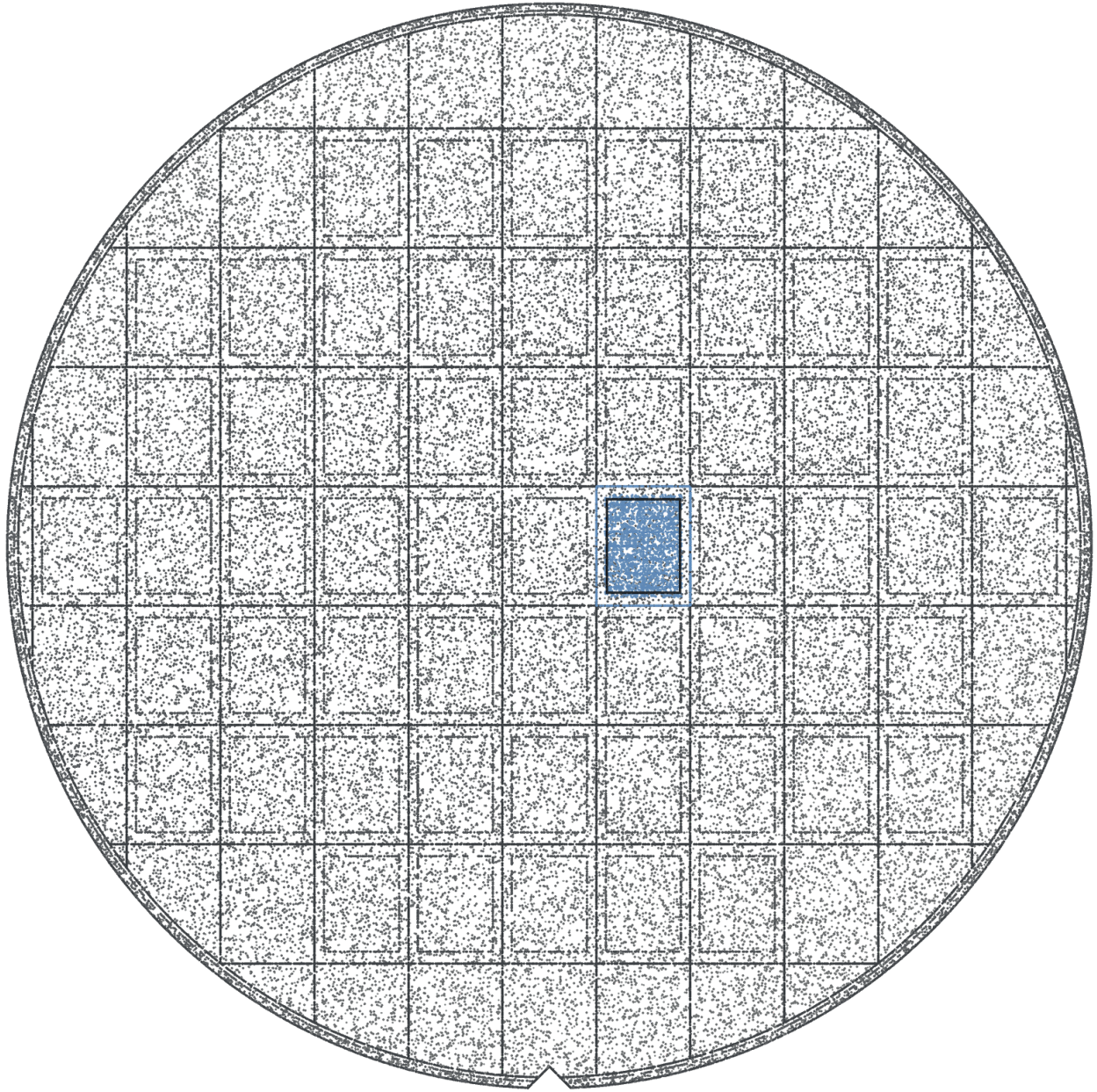




CHIP SUPPLY CHAIN

How AI chips are made

Every stage of the supply chain, and who controls it.

Yashvardhan Sharma with Claude

The Chain: seventeen chapters.

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HOW TO READ A CHAPTER

Each of the fifteen stage chapters opens with a chokepoint card.

Concentration. How many firms credibly supply this stage: Extreme, High, Moderate or Low.

Substitutability. How hard it would be for a well-funded state or firm to build an alternative: Easy, Moderate, Hard or Very hard, rated against four tests.

Price or market size. What one unit costs, or what the stage earns in a year.

The card also gives where China and the United States stand. The chapters run in process order.

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Chip Design, EDA and IP

A small market by revenue and one of the most concentrated. Three software firms sell the tools used to design every leading-edge AI accelerator.

IN PLAIN TERMS

Chip design turns an idea for a new chip into a complete blueprint. A chip holds billions of transistors, tiny electrical switches, and the blueprint fixes where each one sits and how it is wired to the others. The chip works in ticks, and a signal has to cross those wires within one tick, less than a billionth of a second. Software from three companies, Synopsys, Cadence and Siemens, lays out a plan like that, checks it and signs it off, and a chip factory accepts only designs that have passed those tools. The factory prints each layer of the design onto silicon through a stencil, and changing the plan after that takes new stencils and a few months. Withhold the software and no leading-edge chip can be finished.

IN SHORT

In October 2025 CSIS found that only Cadence, Synopsys and Siemens make design software that covers the entire chip design flow, and that Chinese tools were still far from replacing the full range of their advanced capabilities, especially for 5 nm and 3 nm chip design ²⁰. The US government can cut that software off with a letter, and in 2025 it did so for China from late May to 2 July ¹. A narrower US license requirement, agreed through the Wassenaar Arrangement, has covered software made for chips with gate-all-around transistors since October 2022 ¹⁷. In May 2026 SemiAnalysis reported that every advanced chip is designed with software from Synopsys, Cadence and Siemens EDA, and that local design-software companies in China were winning share at mature nodes ³.

²⁰ The Double-Edged Sword of Semiconductor Export Controls: Electronic Design Automation. Center for Strategic and International Studies · 6 October 2025 [\[A\]](https://www.csis.org/analysis/double-edged-sword-semiconductor-export-controls-electronic-design-autom...) [csis.org/analysis/double-edged-sword-semiconductor-export-controls-electronic-design-autom...](https://www.csis.org/analysis/double-edged-sword-semiconductor-export-controls-electronic-design-autom...)

¹ CADENCE DESIGN SYSTEMS INC, Form 8-K current report for the period ended 2025-07-02 (8-K). U.S. Securities and Exchange Commission (filing by CADENCE DESIGN SYSTEMS INC) · 3 July 2025 [\[A\]](https://www.sec.gov/Archives/edgar/data/813672/000081367225000093/cdns-20250702.htm) [sec.gov/Archives/edgar/data/813672/000081367225000093/cdns-20250702.htm](https://www.sec.gov/Archives/edgar/data/813672/000081367225000093/cdns-20250702.htm)

¹⁷ Implementation of Certain 2021 Wassenaar Arrangement Decisions on Four Section 1758 Technologies. Federal Register (Commerce Department; Industry and Security Bureau) · 15 August 2022 [\[A\]](https://www.federalregister.gov/documents/2022/08/15/2022-17125/implementation-of-certain-2021-wassena...) [federalregister.gov/documents/2022/08/15/2022-17125/implementation-of-certain-2021-wassena...](https://www.federalregister.gov/documents/2022/08/15/2022-17125/implementation-of-certain-2021-wassena...)

³ EDA Market Primer. SemiAnalysis · 21 May 2026 [\[B\]](https://www.semianalysis.com/p/eda-market-primer) [newsletter.semianalysis.com/p/eda-market-primer](https://www.semianalysis.com/p/eda-market-primer)

CHOKEPOINT CARD		EXTREME CONCENTRATION	HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY		PRICE OR MARKET SIZE
Extreme	Hard Only three complete sets of chip design software exist, and a fourth would have to be written from nothing and approved by a foundry.		SemiAnalysis put a leading-edge photomask set at \$40M in May 2026 in 2022 it reported startups designing and taping out chips on TSMC 7 nm, then a leading-edge process, for \$50-75M
WHO LEADS	US Synopsys \$7.054B revenue in the fiscal year ended 31 October 2025, Ansys included from July; 90%+ of the timing-signoff market US Cadence \$5.30B revenue in calendar 2025; 55-60% of the hardware emulator market DE Siemens EDA An estimated \$2.2-2.5B revenue in 2025; 85%+ of physical verification, the final layout check GB Arm About 50% of processor compute at the top cloud firms, fiscal 2026 US Broadcom \$16.7B of AI semiconductor revenue in the third quarter of fiscal 2026, custom accelerators and networking combined		
WHERE IT IS MADE	US United States Synopsys, Cadence, Broadcom, Marvell, Nvidia, AMD; Siemens EDA's main sites GB United Kingdom Arm processor and interconnect designs licensed from Cambridge, and since 2026 its own server chip TW Taiwan Alchip, Global Unichip and MediaTek: design services that carry a chip to the factory IL Israel Annapurna Labs, the AWS design house behind Trainium and Graviton IN India Nearly 20% of the world's chip design engineers, on the Indian government's count		
WHY SUBSTITUTION IS SLOW	Three complete sets of chip design software exist today. Changing one tool, such as the synthesis tool, means re-running the later steps of the design, and the foundry that makes the chip specifies which signoff tools its customers must use. A newcomer would have to write a fourth set from nothing and win that foundry approval. CSET at Georgetown University found in 2021, from 2019 data, that Chinese design tools largely did not support processes at 14 nm and below. Industry experts interviewed by CSIS in August 2024 judged China unlikely to develop leading design tools for at least another decade, and able in the short to medium term to replace only specific design steps.		
WHERE CHINA STANDS			
China designs its own AI accelerators, but Huawei's best, the Ascend 950, delivers about half the computing performance of Nvidia's H100 from 2022, on Epoch AI's			

estimate. CSET at Georgetown University found in 2021, from 2019 data, that Chinese design software largely did not support processes at 14 nm and below. In October 2025 CSIS found Chinese design tools still far from replacing the full range of advanced capabilities US firms offer, especially for 5 nm and 3 nm chip design. The US government required a license for design-software sales to China from late May to 2 July 2025, then lifted that requirement. A narrower license requirement on software made for chips with gate-all-around transistors has applied since October 2022.	WHERE THE US STANDS The United States has the two largest design-software vendors and the leading custom-chip design houses. Siemens EDA is German-owned, but the American technology inside it still needs US export licenses.
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Design is the only stage in this chain without a factory, and one the US government has already restricted by letter. In late May 2025 the US government required a license to sell chip design software to anyone in China, and Cadence cut off its Chinese customers until the rule was lifted on 2 July ¹.

How it works

Design runs in five stages, each one's output the next one's input, all of it in software.

- **Architecture.** Engineers fix the shape of the chip: how wide the block that multiplies numbers is, how much fast on-chip memory sits beside it, how many high-bandwidth memory stacks line the edges. The output is a plan.
- **RTL.** Engineers write the plan as register-transfer-level code, RTL, in the hardware language SystemVerilog. A register is a small store on the chip that holds one number, and the clock is the tick that moves every register forward together. The code says what every register holds on every tick, and the output is a text description of the whole chip.
- **Verification.** A large team checks that the code does what the plan says. They run it in simulation, prove parts of it correct with mathematics, and load it into emulators, cabinets of reprogrammable chips that behave like the design, so the chip's own software can boot before any silicon exists.
- **Physical design.** Software swaps each piece of the code for a logic cell, a small ready-made circuit the foundry has already proved it can make, then places the cells on the chip, wires them together and proves that every signal arrives in time.

¹ CADENCE DESIGN SYSTEMS INC, Form 8-K current report for the period ended 2025-07-02 (8-K). U.S. Securities and Exchange Commission (filing by CADENCE DESIGN SYSTEMS INC) · 3 July 2025 [A](https://www.sec.gov/Archives/edgar/data/813672/000081367225000093/cdns-20250702.htm)
sec.gov/Archives/edgar/data/813672/000081367225000093/cdns-20250702.htm

- **Tape-out.** The handover. Software turns the placed layout into pattern files for the mask shop. First it pre-distorts each shape so that it prints as drawn, which is optical proximity correction; then it cuts the layout into the files a mask writer reads, which is mask data preparation.

All that checking exists because each revision after tape-out needs at least some new masks ². In 2022 SemiAnalysis put a full set at more than \$1 million at 28 nm and more than \$10 million at 7 nm, and expected 3 nm sets to push into the \$40 million range ². Its May 2026 primer still puts a leading-edge mask set at \$40 million, and a single respin, a revision after tape-out, at leading-edge nodes at \$50 million to \$100 million ³. In 2022 SemiAnalysis also reported that startups had taken chips on TSMC 7 nm, then a leading-edge process, from design to tape-out for \$50 million to \$75 million, everything included ². In September 2026 CSIS put a different measure, the cost of developing a leading-edge 2 nm chip, at about \$725 million, against \$48 million to develop a 28 nm design in the late 2000s ⁴. The nanometer labels name generations of the process, each finer than the last, and no longer measure anything.

What one photomask set costs, by node, 2022 (\$M). The 28 nm and 7 nm figures are minimums \$M



Source: SemiAnalysis, The Dark Side of the Semiconductor Design Renaissance, July 2022. The 3 nm figure was a 2022 forecast. SemiAnalysis's May 2026 EDA Market Primer puts a leading-edge mask set at \$40M

Variants and trade-offs

Merchant GPU versus custom ASIC

Nvidia designs Blackwell once and sells it to everyone, so the buyer gets mature software and a resale market. A custom accelerator, an ASIC built for one company's own workload, is narrower and tuned to that one workload. Google's seventh-generation tensor processing unit, Ironwood, carries 192 GB of memory per chip, six times its predecessor's, and delivers twice the performance per watt ⁵.

² The Dark Side Of The Semiconductor Design Renaissance – Fixed Costs Soaring Due To Photomask Sets, Verification, and Validation. SemiAnalysis · 24 July 2022 [\[B\]](https://newsletter.semianalysis.com/p/the-dark-side-of-the-semiconductor) newsletter.semianalysis.com/p/the-dark-side-of-the-semiconductor

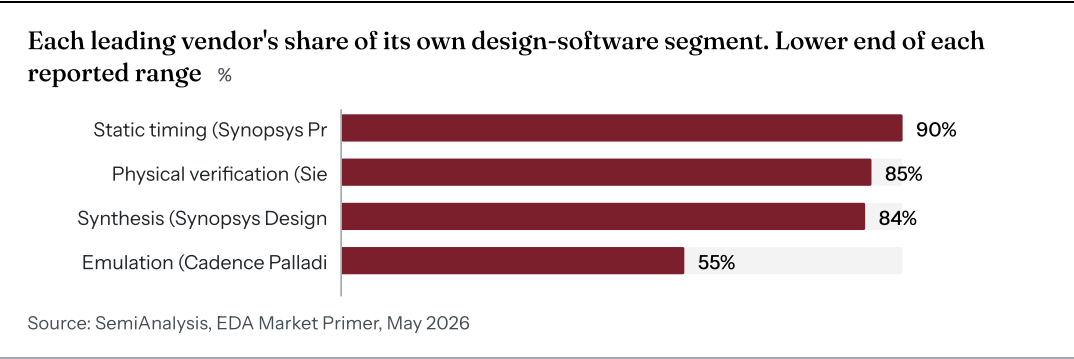
³ EDA Market Primer. SemiAnalysis · 21 May 2026 [\[B\]](https://newsletter.semianalysis.com/p/eda-market-primer) newsletter.semianalysis.com/p/eda-market-primer

⁴ Innovation Lightbulb: The Billion-Dollar Chip: Who Can Afford to Design the Future?. Center for Strategic and International Studies · 11 September 2026 [\[A\]](https://csis.org/analysis/billion-dollar-chip-who-can-afford-design-future) csis.org/analysis/billion-dollar-chip-who-can-afford-design-future

⁵ Ironwood: The first Google TPU for the age of inference. Google · 9 April 2025 [\[A\]](https://blog.google/innovation-and-ai/infrastructure-and-cloud/google-cloud/ironwood-tpu-age-of-in...) blog.google/innovation-and-ai/infrastructure-and-cloud/google-cloud/ironwood-tpu-age-of-in...

The EDA flow

Three complete flows exist, and a change of synthesis tool means re-running place-and-route, signoff and physical verification ³. Foundries also specify which signoff tools their customers must use for tape-out ³. Synopsys alone holds more than 90 percent of static timing analysis, the check that proves a chip will run at its rated speed ³, so inside some steps of the flow one vendor holds most of the market.



Buy the IP or build it

Design houses license the processor cores, the interface controllers and the blocks that drive high-bandwidth memory. Arm licenses processor designs, and in fiscal 2026 it reported \$4.92 billion of revenue, \$2.61 billion of it royalties, and said it held about 50 percent of processor compute at the top cloud firms ⁶. In 2026 Arm also launched the Arm AGI CPU, its first production silicon product, and by May 2026 servers built on it could be ordered from ASRock, Lenovo, Quanta and Supermicro ⁶. The memory interface is a demanding block, because it has to hold its timing across thousands of microscopic solder bumps into a stacked memory die. RISC-V, the open instruction set that needs no license, handles the small control tasks on the chip, and Nvidia now uses it in every GPU ⁷.

Chiplets

The reticle limit, the largest area a scanner can print in one exposure, limits how large a single die can grow ⁸. Many large accelerators are built from chiplets, several smaller dies wired together, and UCIE is an open industry standard for the links between them inside a package ⁹. Version 3.0 of UCIE adds 48 and 64 GT/s data rates ⁹. Broadcom's 3.5D XDSiP platform packs more than 6,000 mm2 of silicon and 12 high-bandwidth memory stacks into one package ⁸.

3 EDA Market Primer. SemiAnalysis · 21 May 2026 [B](https://newsletter.semianalysis.com/p/eda-market-primer) newsletter.semianalysis.com/p/eda-market-primer

6 Arm delivers record-breaking quarter and full-year results. Arm · 6 May 2026 [A](https://newsroom.arm.com/news/arm-q4-fye26-results) newsroom.arm.com/news/arm-q4-fye26-results

7 Behind The Scenes of SHD Group's 2026 RISC-V Market Forecast. RISC-V International · 19 June 2026 [A](https://riscv.org/blog/shd-forecast-2026) riscv.org/blog/shd-forecast-2026

8 3.5D XDSiP Platform Technology. Broadcom · 4 December 2024 [A](https://docs.broadcom.com/doc/3-5d-xdsip-platform-technology) docs.broadcom.com/doc/3-5d-xdsip-platform-technology

9 Specifications | UCIE Consortium. UCIE Consortium [A](https://uciexpress.org/specifications) uciexpress.org/specifications

Who makes it

Design software and licensed blocks were an \$18 billion market in 2025, and Synopsys, Cadence and Siemens EDA took more than 85 percent of it, counting Ansys as part of Synopsys, with no other vendor above 5 percent in any core category ³.

Synopsys is the largest. Its own results put revenue at \$7.054 billion for the fiscal year to 31 October 2025, with Ansys, bought that July, contributing \$756.6 million ¹⁰. Cadence, whose year ends in December, took \$5.297 billion in calendar 2025 ¹¹. The two fiscal years do not line up, so any total for this market depends on which twelve months are counted and on how much of Ansys it includes. SemiAnalysis counts Synopsys at \$8 billion for calendar 2025 with Ansys included, and it puts 31 percent of Ansys's business in semiconductors and high technology, 22 percent in aerospace and 18 percent in automotive ³.

Design software and licensed-block revenue share, 2025. Synopsys includes Ansys %



Source: SemiAnalysis, EDA Market Primer, May 2026. Shares calculated from its calendar 2025 revenue figures, with Synopsys at \$8B including Ansys and Siemens EDA at the middle of its \$2.2-2.5B estimate

Some chip firms also build custom accelerators to a customer's design and sell the finished chips. Broadcom booked \$16.7 billion of AI semiconductor revenue in the third quarter of fiscal 2026, up 221 percent year over year, a figure that covers both its custom AI accelerators and its AI networking chips ¹².

In October 2025 OpenAI and Broadcom said they would deploy 10 gigawatts of OpenAI-designed accelerators, with Broadcom turning the design into silicon and supplying the Ethernet networking around it ¹³. In April 2026 Broadcom extended its Meta partnership to multiple gigawatts of MTIA, Meta's in-house chip, and the first 2 nm AI accelerator ¹⁴.

Below Broadcom and Marvell sit the Taiwanese design-service houses that carry a customer's circuit list all the way to a finished mask set on TSMC's newest nodes; Alchip reported \$992 million of revenue in 2025 ¹⁵. The engineers are spread

³ EDA Market Primer. SemiAnalysis · 21 May 2026 [\[B\]](https://newsletter.semianalysis.com/p/eda-market-primer) newsletter.semianalysis.com/p/eda-market-primer

¹⁰ SYNOPSYS INC, Form 8-K current report for the period ended 2025-12-10 (8-K). U.S. Securities and Exchange Commission (filing by SYNOPSYS INC) · 10 December 2025 [\[A\]](https://sec.gov/Archives/edgar/data/883241/000119312525314200/d29055dex991.htm) sec.gov/Archives/edgar/data/883241/000119312525314200/d29055dex991.htm

¹¹ CADENCE DESIGN SYSTEMS INC, Form 10-K annual report for the period ended 2025-12-31 (financial statement R115). U.S. Securities and Exchange Commission (filing by CADENCE DESIGN SYSTEMS INC) · 19 February 2026 [\[A\]](https://sec.gov/Archives/edgar/data/813672/000081367226000016/R115.htm) sec.gov/Archives/edgar/data/813672/000081367226000016/R115.htm

¹² Broadcom Inc., Form 8-K current report for the period ended 2026-09-02 (8-K). U.S. Securities and Exchange Commission (filing by Broadcom Inc.) · 2 September 2026 [\[A\]](https://sec.gov/Archives/edgar/data/0001730168/000173016826000076/avgo-08022026x8kxex99.htm) sec.gov/Archives/edgar/data/0001730168/000173016826000076/avgo-08022026x8kxex99.htm

¹³ OpenAI and Broadcom announce strategic collaboration to deploy 10 gigawatts of OpenAI-designed AI accelerators. Broadcom [\[A\]](https://investors.broadcom.com/news-releases/news-release-details/openai-and-broadcom-announce-str...) investors.broadcom.com/news-releases/news-release-details/openai-and-broadcom-announce-str...

¹⁴ Broadcom Announces Extended Partnership with Meta to Deploy Technology to Support Multi-Gigawatts of Meta's Custom Silicon, MTIA. Broadcom · 14 April 2026 [\[A\]](https://investors.broadcom.com/news-releases/news-release-details/broadcom-announces-extended-part...) investors.broadcom.com/news-releases/news-release-details/broadcom-announces-extended-part...

¹⁵ Financials - Alchip. Alchip Technologies [\[A\]](https://alchip.com/en/Investors/financials) alchip.com/en/Investors/financials

across more countries than the firms, and India alone holds nearly 20 percent of the world's chip designers ¹⁶.

The chokepoint

A narrower control came first. Since 14 October 2022, design software specially made for chips with gate-all-around transistors, a design the rule calls key to processes at 3 nm and below, has needed a US export license for national-security reasons ¹⁷. That license requirement covers exports to China ¹⁸. The control carried out a December 2021 decision of the Wassenaar Arrangement, the multilateral export-control group ¹⁷.

In late May 2025 the US Bureau of Industry and Security, the agency that writes export licenses, told the design-software vendors that sales to China now needed a license ¹. Cadence got its letter on 23 May: exporting design software classified 3D991 and 3E991 to any party in China, or to a Chinese military end user anywhere, now needed a license ¹. Synopsys got its letter on 29 May and a rescinding letter on 2 July ¹⁹.

Washington imposed the 2025 requirement alone, and at once. Synopsys's China revenue fell from 16 percent of its total in fiscal 2024 to 12 percent in fiscal 2025 ³. SemiAnalysis links the decline to tighter export restrictions and to local design-software companies winning share at mature nodes ³. SemiAnalysis also quoted Synopsys's management saying that the companies it cannot sell to look for alternatives, typically local design-software and licensed-block companies ³.

¹⁶ India's Semiconductor Vision Gathers Momentum with 3nm Chip Design and Large-Scale Talent Development Initiatives. Press Information Bureau, Government of India [A](https://pib.gov.in/PressReleasePage.aspx) pib.gov.in/PressReleasePage.aspx

¹⁷ Implementation of Certain 2021 Wassenaar Arrangement Decisions on Four Section 1758 Technologies. Federal Register (Commerce Department; Industry and Security Bureau) · 15 August 2022 [A](https://www.federalregister.gov/documents/2022/08/15/2022-17125/implementation-of-certain-2021-wassena...) [federalregister.gov/documents/2022/08/15/2022-17125/implementation-of-certain-2021-wassena...](https://www.federalregister.gov/documents/2022/08/15/2022-17125/implementation-of-certain-2021-wassena...)

¹⁸ Supplement No. 1 to Part 738, Title 15 -- Commerce Country Chart. Electronic Code of Federal Regulations [A](https://www.ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-738/appendix-Supplement...) [ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-738/appendix-Supplement...](https://www.ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-738/appendix-Supplement...)

¹ CADENCE DESIGN SYSTEMS INC, Form 8-K current report for the period ended 2025-07-02 (8-K). U.S. Securities and Exchange Commission (filing by CADENCE DESIGN SYSTEMS INC) · 3 July 2025 [A](https://www.sec.gov/Archives/edgar/data/813672/000081367225000093/cdns-20250702.htm) [sec.gov/Archives/edgar/data/813672/000081367225000093/cdns-20250702.htm](https://www.sec.gov/Archives/edgar/data/813672/000081367225000093/cdns-20250702.htm)

¹⁹ SYNOPSYS INC, Form 8-K current report for the period ended 2025-07-02 (8-K). U.S. Securities and Exchange Commission (filing by SYNOPSYS INC) · 3 July 2025 [A](https://www.sec.gov/Archives/edgar/data/883241/000119312525155294/d80081d8k.htm) [sec.gov/Archives/edgar/data/883241/000119312525155294/d80081d8k.htm](https://www.sec.gov/Archives/edgar/data/883241/000119312525155294/d80081d8k.htm)

³ EDA Market Primer. SemiAnalysis · 21 May 2026 [B](https://www.semianalysis.com/p/eda-market-primer) [newsletter.semianalysis.com/p/eda-market-primer](https://www.semianalysis.com/p/eda-market-primer)

In October 2025 CSIS found that only a few companies, Cadence, Synopsys and Siemens, make design software that supports the entire chip design flow of more than 40 steps ²⁰. In a January 2021 report built on 2019 market data, CSET at Georgetown University found that one Chinese firm, Empyrean, could reportedly run a complete design flow only for certain analog and mixed-signal chips, which combine analog and digital circuits ²¹. Outside that niche, Chinese designers then relied on US tools for all chip designs ²¹. The report found that other Chinese tools covered only narrow parts of the design flow or supplemented US tools, and largely did not support processes at 14 nm and below ²¹. In its 2025 annual report, filed in April 2026, Empyrean says it now has complete design flows for analog, memory, radio-frequency and flat-panel display circuits, and that its digital tools cover 80 percent of the main tools for digital design ²². The same report lists foundry certifications for its circuit simulator at 8, 5 and 4 nm and for its physical verification tool, the final layout check, at 28 nm ²². CSIS found that as of 2025 Chinese design tools were still far from replacing the full range of advanced capabilities US firms offer, especially for 5 nm and 3 nm chip design ²⁰.

China can design an accelerator. It cannot finish one at the leading edge without foreign tools, or build what it designs without foreign equipment. In June 2024 CSET found that SMIC's limited 7 nm capacity forced Huawei to choose between making its most advanced phone chips and its AI chips ²³.

On Epoch AI's estimates, Huawei's flagship chip for 2026, the Ascend 950, delivers about half the computing performance of Nvidia's H100, which began shipping in 2022, and Nvidia's B300 has 6.75 times the 950's theoretical peak performance ²⁴. Epoch's median estimate is that Huawei will make about 1.5 million Ascend chips in 2026, against 5.9 million for Nvidia ²⁴. On those estimates, Huawei's 2026 output would carry less than 4 percent of the computing power Nvidia ships that year ²⁴. Epoch puts Huawei's chips three to four years behind Nvidia's until at least 2030, for three reasons. SMIC, which makes Huawei's chips, cannot pack transistors as densely as TSMC, which makes Nvidia's. Chinese memory makers are only starting to produce high-bandwidth memory. And Huawei's software for programming its chips is far less mature than Nvidia's ²⁴.

20 The Double-Edged Sword of Semiconductor Export Controls: Electronic Design Automation. Center for Strategic and International Studies · 6 October 2025 [\[A\]](https://www.csis.org/analysis/double-edged-sword-semiconductor-export-controls-electronic-design-autom...) [csis.org/analysis/double-edged-sword-semiconductor-export-controls-electronic-design-autom...](https://www.csis.org/analysis/double-edged-sword-semiconductor-export-controls-electronic-design-autom...)

21 The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology (CSET) · 21 January 2021 [\[A\]](https://www.cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf) [cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf](https://www.cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf)

22 北京华大九天科技股份有限公司2025 年年度报告全文 北京华大九天科技股份有限公司. Cninfo · 27 April 2026 [\[A\]](https://static.cninfo.com.cn/finalpage/2026-04-28/1225217315.PDF) static.cninfo.com.cn/finalpage/2026-04-28/1225217315.PDF

23 Pushing the Limits: Huawei's AI Chip Tests U.S. Export Controls. Center for Security and Emerging Technology (CSET) · 17 June 2024 [\[A\]](https://www.cset.georgetown.edu/publication/pushing-the-limits-huaweis-ai-chip-tests-u-s-export-controls) [cset.georgetown.edu/publication/pushing-the-limits-huaweis-ai-chip-tests-u-s-export-controls](https://www.cset.georgetown.edu/publication/pushing-the-limits-huaweis-ai-chip-tests-u-s-export-controls)

24 Will Huawei catch up to Nvidia by 2030?. Epoch AI · 24 September 2026 [\[A\]](https://epoch.ai/publications/huaweis-roadmap-to-2031) epoch.ai/publications/huaweis-roadmap-to-2031

Key evaluation criteria

- **Flow completeness.** How many steps one vendor covers, from the first line of code to final signoff.
- **Foundry certification.** Whether the foundry has validated that exact tool version against its reference flow and process design kit, the file set describing what the factory can print. Without that, the foundry refuses signoff.
- **Verification throughput.** Simulation cycles and emulator capacity per day, which set the schedule more than anything else.
- **IP availability at node.** Whether the licensed blocks, the processor cores, the high-speed serial links, PCIe and the memory interface, have been proven in silicon on that process.
- **Design services depth.** Whether a partner can carry a customer's circuit list to a finished mask set on the newest node.
- **Legal exposure.** How much of the flow is US-origin technology, and so subject to export licensing.

FIVE THINGS TO REMEMBER

- Chip design turns an idea into a blueprint, and a factory builds only designs checked in approved software.
- Synopsys, Cadence and Siemens EDA sell the software used to design every leading-edge chip.
- A new vendor would have to write a complete set of tools and win a foundry's approval.
- China designs its own AI chips, but in October 2025 CSIS found its design software still far from replacing US tools, especially for 5 nm and 3 nm chips.
- Huawei's best AI chip trails Nvidia's by three to four years, on Epoch AI's estimate.

Silicon and Wafers

China makes almost all of the world's polysilicon. Firms headquartered in Japan, Taiwan, Germany and South Korea make most of the 300 mm wafers that advanced chips start on. Chinese firms held under 1 percent of that market in 2019, but China's largest 300 mm wafer maker, Eswin, says it shipped about 7.7 percent in the first half of 2026.

IN PLAIN TERMS

Every chip is built on a wafer, a thin round slice of silicon about 30 centimeters across that carries hundreds of chips at once. Making one starts with sand, which is silicon bound to oxygen. The silicon is refined until metal impurities are no more than a few parts per billion. The silicon is melted, a small seed crystal is lowered to the surface and drawn slowly back up, and the melt freezes onto it as one long cylinder, a single crystal with its atoms in one unbroken orderly pattern from end to end. Saws cut the cylinder into discs, and each disc is polished to a mirror finish and made extremely flat across its whole face. In 2025 the top five wafer makers served around 75 percent of the world market, and none of them is American or Chinese.

IN SHORT

In 2024, five companies based in Japan, Taiwan, Germany and South Korea shipped about 79 percent of the world's 300 mm wafers, the polished discs that advanced chips start from, by Eswin's estimate from SEMI data ⁸. China made about 93 percent of the world's polysilicon, the raw material, in 2023 ¹⁴. None of the five major suppliers of electronic-grade silicon that Siltronic named for 2025 is Chinese ⁴. Chinese firms held under 1 percent of the world market for 300 mm wafers as of 2019 ⁷. In the first half of 2026, Eswin, China's largest 300 mm wafer maker, had about 7.7 percent of global 300 mm shipments by its own count ²⁰.

⁸ 688783 20251022 UYMD. Sse [\[A\]](https://static.sse.com.cn/disclosure/listedinfo/announcement/c/new/2025-10-22/688783_20251022_UYMD...)

¹⁴ The Mineral Industry of China in 2020-2021. U.S. Geological Survey · 17 February 2026 [\[A\]](https://pubs.usgs.gov/myb/vol3/2023/myb3-2023-china.pdf)

⁴ FOUNDATION OF DIGITAL LIFE Investor Presentation. Siltronic · 29 April 2026 [\[A\]](https://siltronic.com/fileadmin/investorrelations/2026/Q1/20260429_Siltronic_InvestorPresentation_...)

⁷ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology (CSET) · 21 January 2021 [\[A\]](https://cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf)

²⁰ 西安奕斯伟材料科技股份有限公司2026年半年度报告 1 / 208. Cninfo · 25 August 2026 [\[A\]](https://static.cninfo.com.cn/finalpage/2026-08-26/1225503057.PDF)

CHOKEPOINT CARD		HIGH CONCENTRATION
		MODERATELY HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY	PRICE OR MARKET SIZE
High	Moderate Several firms already make 300 mm wafers that fabs have approved, but customers have to qualify a new wafer plant before they buy from it.	The world wafer market was \$11.4bn in 2025, on 12,973 million square inches shipped
WHO LEADS	JP Shin-Etsu Handotai Wafer sales are not broken out in its parent's results. The parent's electronics materials segment, which also sells rare earth magnets, encapsulants, photoresists and photomask blanks, had ¥1,015.7bn of sales in the year to March 2026 JP SUMCO ¥409.7bn of 2025 net sales, but an ¥11.8bn loss TW GlobalWafers NT\$60.6bn revenue in 2025 KR SK Siltron One of the top five wafer makers, which served around 75 percent of the market in 2025 DE Siltronic €1,346.7m revenue in 2025	
WHERE IT IS MADE	JP Japan Shin-Etsu and SUMCO crystal growth and polishing TW Taiwan GlobalWafers headquarters and plants DE Germany Siltronic Burghausen and Freiberg; Wacker semiconductor-grade polysilicon KR South Korea SK Siltron US United States Hemlock polysilicon in Michigan; GlobalWafers Sherman, Texas and St Peters, Missouri	
WHY SUBSTITUTION IS POSSIBLE	Firms headquartered in Japan, Taiwan, Germany and South Korea make state-of-the-art 300 mm wafers, and the top five served around 75 percent of the market in 2025, so losing one leaves four. A new wafer plant can still be built: GlobalWafers of Taiwan spent \$3.5 billion on a plant in Texas, the first wafer production line of its kind in the United States in over twenty years. The slow part is approval. Customers have to qualify a new plant before they buy from it, and Siltronic completed key customer qualifications at its new Singapore fab in July 2025. Siltronic also sells under long-term agreements.	
WHERE CHINA STANDS		
China made about 93 percent of the world's polysilicon in 2023, an estimated 98 percent of it solar grade and 2 percent electronic grade, a split close to the world's. None of the five major suppliers of silicon for electronics that Siltronic names is Chinese. Chinese firms held under 1 percent of the 300 mm wafer market as of 2019, and as of 2018 Chinese producers made only 12 percent of the wafers for Chinese-headquartered 300 mm fabs. Eswin, China's largest 300 mm		

wafer maker, says it shipped about 7.7 percent of the world's 300 mm wafers in the first half of 2026, up from about 6 percent in 2024.	WHERE THE US STANDS No major US-headquartered firm makes wafers. Hemlock makes polysilicon in Michigan, and GlobalWafers of Taiwan took CHIPS awards of up to \$406 million for wafer plants in Texas and Missouri. Its \$3.5 billion Texas plant opened in May 2025. Proclamation 11052, signed August 6, 2026, sets a minimum import price of \$100 per kilogram for polysilicon ingots and wafers and an extra 15 percent duty on imported ingots and other listed products made from polysilicon, both from December 4, 2026. Firms with approved plans to build US polysilicon, ingot, wafer or cell plants can import equipment and some of those products without the new duties.
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The whole world market for silicon wafers came to \$11.4 billion of revenue on 12,973 million square inches in 2025 ¹. That is a small fraction of Nvidia's data center revenue, which reached \$193.7 billion in the fiscal year to January 25, 2026 ².

How it works

Silicon starts as quartzite, a rock that is silicon bound to oxygen. An arc furnace melts it with carbon, and the carbon takes the oxygen away as gas, leaving rough silicon metal. Refiners turn the metal into a gas, trichlorosilane, and distill it, because the impurities boil at other temperatures and stay behind. The clean gas then flows over silicon filaments heated inside a bell jar. On the hot surface the gas breaks apart, its silicon settles onto the filaments, and over days the filaments thicken into gray rods of polysilicon, the Siemens process. Everything downstream is made from those rods. Polysilicon comes in two ultra-high-purity grades, one for semiconductors and one for solar cells, and chips use the semiconductor grade ⁵.

A grower melts the polysilicon at about 1,420 degrees Celsius, hotter than lava, and pulls a single crystal out of it by the Czochralski method ³. The grower lowers a small seed crystal on the end of a rod to the surface of the melt and draws it back up, slowly turning. Silicon freezes onto the seed in the seed's own atomic pattern, and a cylinder grows beneath it, the ingot. The pull starts with a thin neck so that the flaws formed where the seed first touched the melt end in the neck and never reach the ingot. Boron or phosphorus stirred into the melt, a step called doping, sets how readily the wafer conducts and whether the current in it is carried by negative charges or positive ones.

1 SEMI Reports 2025 Annual Worldwide Silicon Wafer Shipments and Revenue Results. PR Newswire · 10 February 2026

prnewswire.com/news-releases/semi-reports-2025-annual-worldwide-silicon-wafer-shipments-an...

2 NVIDIA Announces Financial Results for Fourth Quarter and Fiscal 2026. Nvidia · 25 February 2026

nvidianews.nvidia.com/news/nvidia-announces-financial-results-for-fourth-quarter-and-fisca...

5 Mineral Commodity Summaries 2026. U.S. Geological Survey · 5 February 2026

pubs.usgs.gov/periodicals/mcs2026/mcs2026-silicon.pdf

3 SUMCO, production processes page. SUMCO

sumcosi.com/english/products/process

A wire saw, a web of fine wire running through abrasive, slices the ingot into discs. The maker then laps each disc, grinding both faces flat between rotating plates, chemically etches off the damaged surface, and polishes it to a mirror with colloidal silica, a slurry of silica particles far too small to see. Epitaxial wafers get one more layer of near-perfect silicon grown on top at about 1,200 degrees Celsius³, still hot enough to glow orange, and almost every step throws material away.

Variants and trade-offs

Polished versus epitaxial

A polished wafer is a doped single crystal polished to a mirror finish³. An epitaxial wafer is a polished wafer with a thin layer of single-crystal silicon grown on top at about 1,200 degrees Celsius³. The transistors live in that layer, so its quality sets the lowest leakage the chip can reach and its risk of latch-up, a parasitic short between power and ground. SEMI, the industry association, credits the 2025 rise in shipments to AI-driven demand for advanced epitaxial wafers in logic and polished wafers for high-bandwidth memory¹.

Silicon on insulator

A buried layer of oxide, which is glass, separates a thin working layer of silicon from the bulk beneath, and Soitec's Smart Cut process makes nearly all of it⁶. Soitec's SOI product lines include RF-SOI for radio chips and FD-SOI, and its markets run from mobile communications to cloud AI⁶. SEMI tied the AI-driven growth in logic to advanced epitaxial wafers¹.

Who makes it

In a January 2021 brief, CSET at Georgetown named Shin-Etsu, SUMCO, GlobalWafers, Siltronic and SK Siltron, headquartered in Japan, Taiwan, Germany and South Korea, as key wafer firms⁷. It also listed nine Chinese-owned producers, among them Zhonghuan, Simgui, ZingSEMI and Finland's Okmetic, but said they generated little revenue in comparison⁷. As of 2018, five Chinese firms were making or planning 300 mm wafers⁷. Eswin's October 2025 listing prospectus counts seven Chinese firms, Eswin included, making 300 mm wafers at scale, with a combined capacity of 2.94 million wafers a month at the end of 2024⁸.

³ SUMCO, production processes page. SUMCO [\[A\]](https://sumcosi.com/english/products/process) sumcosi.com/english/products/process

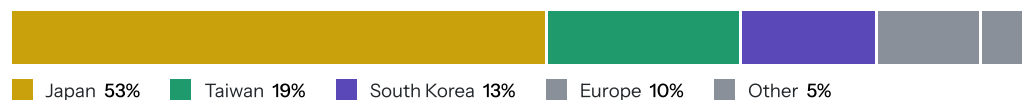
¹ SEMI Reports 2025 Annual Worldwide Silicon Wafer Shipments and Revenue Results. PR Newswire · 10 February 2026 [\[A\]](https://prnewswire.com/news-releases/semi-reports-2025-annual-worldwide-silicon-wafer-shipments-an...) prnewswire.com/news-releases/semi-reports-2025-annual-worldwide-silicon-wafer-shipments-an...

⁶ Soitec | Key figures. Soitec [\[A\]](https://soitec.com/home/group) soitec.com/home/group

⁷ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology (CSET) · 21 January 2021 [\[A\]](https://cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf) cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf

⁸ 688783 20251022 UYMD. Sse [\[A\]](https://static.sse.com.cn/disclosure/listedinfo/announcement/c/new/2025-10-22/688783_20251022_UYMD...) static.sse.com.cn/disclosure/listedinfo/announcement/c/new/2025-10-22/688783_20251022_UYMD...

Silicon wafer sales by supplier headquarters, 2023. Japan held 53%, and the source shows no separate share for China or the United States %



Source: METI, December 2025, from Fuji Keizai data (2023); Japan's share is printed, the others are read off METI's chart

The chart shows shares of 2023 sales from a survey by Fuji Keizai, a Japanese research firm, relayed in the December 2025 strategy deck of Japan's Ministry of Economy, Trade and Industry ⁹. The deck prints only Japan's 53 percent, so the other shares are read off its chart, which gives no separate share to Chinese or US companies ⁹. Siltronic's April 2026 investor presentation says the top five wafer makers serve around 75 percent of the market, based on revenue in the first three quarters of 2025 ⁴.

Their 2025 results split between an AI boom and a slump in the older, mature nodes.

- **Shin-Etsu.** Its parent's electronics materials segment sold ¥1,015.7 billion in the year to March 2026, up 9 percent, as AI-related demand stayed strong and demand in other sectors began to rise, lifting sales of silicon wafers, photoresist and photomask blanks ¹⁰. The segment also sells rare earth magnets and other materials, and the results release does not break out wafer sales, so the figure cannot be compared with the wafer revenue of the other firms here ¹⁰.
- **SUMCO.** Sold ¥409.7 billion and still lost ¥11.8 billion, as operating profit fell from ¥36.9 billion to ¥1.3 billion while it added leading-edge 300 mm capacity and reorganized production of 200 mm and smaller wafers, where demand stayed weak ¹¹.
- **Siltronic.** Lost €77.9 million on €1,346.7 million of sales while investing €369.1 million, with its new Singapore fab as the focus ¹².
- **GlobalWafers.** NT\$60.6 billion of revenue, down 3.24 percent in local currency ¹³.

⁹ METI, Semiconductor and digital industry strategy: future direction (半導体・デジタル産業戦略の今後の方向性), 23 December 2025. Ministry of Economy, Trade and Industry (Japan) · 23 December 2025 [A](https://meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/0014/handaji14-4.pdf)
meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/0014/handaji14-4.pdf

⁴ FOUNDATION OF DIGITAL LIFE Investor Presentation. Siltronic · 29 April 2026 [A](https://siltronic.com/fileadmin/investorrelations/2026/Q1/20260429_Siltronic_InvestorPresentation_...)
siltronic.com/fileadmin/investorrelations/2026/Q1/20260429_Siltronic_InvestorPresentation_...

¹⁰ Consolidated Financial Results for the Fiscal Year Ended March 31, 2026. Shin-Etsu Chemical · 27 April 2026 [A](https://shinetsu.co.jp/wp-content/uploads/2025/07/20260428_con_E.pdf)
shinetsu.co.jp/wp-content/uploads/2025/07/20260428_con_E.pdf

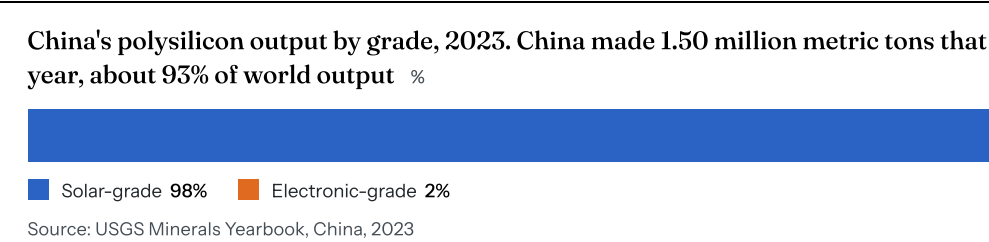
¹¹ Note: This document has been translated from the Japanese original for reference purposes only. In the event of any. SUMCO · 3 March 2026 [A](https://sumcosi.com/english/pdf/ir/library/shareholders/27/pdf/nc_e_27.pdf)
sumcosi.com/english/pdf/ir/library/shareholders/27/pdf/nc_e_27.pdf

¹² Siltronic AG: Robust business performance in 2025 demonstrates resilience despite challenging conditions. Siltronic · 27 August 2026 [A](https://siltronic.com/en/press/press-releases/siltronic-ag-robust-business-performance-in-2025-dem...)
siltronic.com/en/press/press-releases/siltronic-ag-robust-business-performance-in-2025-dem...

¹³ GlobalWafers Reports Full Year 2025 Results - GlobalWafers Co., Ltd. All rights reserved.. GlobalWafers · 3 March 2026 [A](https://globalwafers.com/en/gwc_news_en_20260303) sas-
globalwafers.com/en/gwc_news_en_20260303

Area shipped rose 5.8 percent in 2025 while revenue fell 1.2 percent ¹. SEMI attributes the softer revenue mostly to traditional chip applications, where demand and pricing had yet to improve ¹.

China made 1.50 million metric tons of polysilicon, the raw material, in 2023, about 93 percent of world output ¹⁴. Solar-grade material was an estimated 98 percent of that output and electronic-grade 2 percent ¹⁴. The Commerce Department found in 2026 that semiconductor-grade polysilicon makes up only 2.4 percent of global production, a split close to China's ¹⁵. The share alone does not show whether Chinese polysilicon goes into chips.



Siltronic put the 2025 market for electronic-grade silicon at \$1.4 billion, with five major suppliers, none of them Chinese: Wacker, Hemlock, OCI, Tokuyama and Mitsubishi ⁴.

The leading wafer makers are headquartered in Japan, Taiwan, Germany and South Korea, and Siltronic of Germany describes itself as the only Western-based maker among the top five, based on revenue in the first three quarters of 2025 ⁴. GlobalWafers opened a \$3.5 billion plant in Sherman, Texas in May 2025, the first production line of its kind built in the United States in over twenty years, and announced another \$4 billion for phases three and four the same day ¹⁶. Washington had awarded it up to \$406 million under the CHIPS incentives program for wafer plants in Texas and Missouri ¹⁷.

¹ SEMI Reports 2025 Annual Worldwide Silicon Wafer Shipments and Revenue Results. PR Newswire · 10 February 2026 [\[A\]](#)
prnewswire.com/news-releases/semi-reports-2025-annual-worldwide-silicon-wafer-shipments-an...

¹⁴ The Mineral Industry of China in 2020-2021. U.S. Geological Survey · 17 February 2026 [\[A\]](#) pubs.usgs.gov/myb/vol3/2023/myb3-2023-china.pdf

¹⁵ Adjusting Imports of Polysilicon and Its Derivatives Into the United States. Federal Register (Executive Office of the President) · 11 August 2026 [\[A\]](#) federalregister.gov/documents/2026/08/11/2026-16400/adjusting-imports-of-polysilicon-and-i...

⁴ FOUNDATION OF DIGITAL LIFE Investor Presentation. Siltronic · 29 April 2026 [\[A\]](#)
siltronic.com/fileadmin/investorrelations/2026/Q1/20260429_Siltronic_InvestorPresentation_...

¹⁶ GlobalWafers America Officially Opens for Business - GlobalWafers Co., Ltd. All rights reserved.. GlobalWafers · 15 May 2025 [\[A\]](#) sas-globalwafers.com/en/gwc_news_en_20250516

¹⁷ Biden-Harris Administration Announces CHIPS Incentives Awards with GlobalWafers to Support Domestic Production of Silicon Wafers. NIST · 17 December 2024 [\[A\]](#) nist.gov/news-events/news/2024/12/biden-harris-administration-announces-chips-incentives-a...

Presidential Proclamation 11052, signed August 6, 2026, sets a minimum import price of \$100 per kilogram for polysilicon ingots and wafers and an extra 15 percent duty on imported ingots and other listed products made from polysilicon, both from December 4, 2026 ¹⁵. A September 2026 Commerce rule meant to stop stockpiling before the duties start lists tariff code 3818.00.0040 among the products it covers ¹⁸. That code covers round, doped, single-crystal silicon wafers ¹⁹. Commerce may approve plans to build US polysilicon, ingot, wafer or cell plants whose construction starts by January 20, 2029, and firms with approved plans can import equipment and some of those products without the new duties ¹⁵.

The chokepoint

China dominates polysilicon, and in 2019 it had almost no share in wafers. As of 2019 Chinese firms held under 5 percent of the wafer market and under 1 percent of 300 mm ⁷. As of 2018, Chinese producers made 12 percent of the wafers for Chinese-headquartered 300 mm fabs, against 18 percent for 100 to 200 mm fabs ⁷. Eswin, mainland China's largest maker of 300 mm wafers, says it ranked sixth in the world with about 7.7 percent of global 300 mm shipments in the first half of 2026 ²⁰. Its October 2025 Shanghai listing prospectus, drawing on SEMI data, estimates that the five largest makers shipped about 79 percent of 300 mm wafers in 2024, Eswin about 6 percent and all other makers about 15 percent ⁸.

Making the smoothest, high-purity 300 mm wafers takes considerable know-how that is hard to write down, and 300 mm carried 99.7 percent of world fab capacity at 45 nm and below in SEMI figures from November 2020 cited by CSET ⁷.

Counting wafers of every size, SEMI estimated that 300 mm wafers made up about 78.8 percent of the wafer area shipped worldwide in 2025, according to Eswin's 2025 annual report summary ²¹. Customers have to qualify a new wafer plant before they buy from it, and Siltronic completed key customer qualifications at its new Singapore fab in July 2025 ⁴.

15 Adjusting Imports of Polysilicon and Its Derivatives Into the United States. Federal Register (Executive Office of the President) · 11 August 2026 [\[A\] federalregister.gov/documents/2026/08/11/2026-16400/adjusting-imports-of-polysilicon-and-i...](https://www.federalregister.gov/documents/2026/08/11/2026-16400/adjusting-imports-of-polysilicon-and-i...)

18 Measures To Restrict Stockpiling of Polysilicon and Polysilicon Derivatives Under Proclamation 11052. Federal Register (Commerce Department; Industry and Security Bureau) · 24 September 2026 [\[A\] federalregister.gov/documents/2026/09/24/2026-19537/measures-to-restrict-stockpiling-of-po...](https://www.federalregister.gov/documents/2026/09/24/2026-19537/measures-to-restrict-stockpiling-of-po...)

19 Harmonized Tariff Schedule. Harmonized Tariff Schedule [\[A\] hts.usitc.gov/search](https://hts.usitc.gov/search)

7 The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology (CSET) · 21 January 2021 [\[A\] cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf](https://cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf)

20 西安奕斯伟材料科技股份有限公司2026 年半年度报告 1 / 208. Cninfo · 25 August 2026 [\[A\] static.cninfo.com.cn/finalpage/2026-08-26/1225503057.PDF](https://static.cninfo.com.cn/finalpage/2026-08-26/1225503057.PDF)

8 688783 20251022 UYMD. Sse [\[A\] static.sse.com.cn/disclosure/listedinfo/announcement/c/new/2025-10-22/688783_20251022_UYMD...](https://static.sse.com.cn/disclosure/listedinfo/announcement/c/new/2025-10-22/688783_20251022_UYMD...)

21 688783 20260421 6JVC. Sse [\[A\] static.sse.com.cn/disclosure/listedinfo/announcement/c/new/2026-04-21/688783_20260421_6JVC...](https://static.sse.com.cn/disclosure/listedinfo/announcement/c/new/2026-04-21/688783_20260421_6JVC...)

4 FOUNDATION OF DIGITAL LIFE Investor Presentation. Siltronic · 29 April 2026 [\[A\] siltronic.com/fileadmin/investorrelations/2026/Q1/20260429_Siltronic_InvestorPresentation...](https://siltronic.com/fileadmin/investorrelations/2026/Q1/20260429_Siltronic_InvestorPresentation...)

The last increase in wafer size, to 300 mm, happened in 2002 ⁷. Bigger discs make printing a bigger share of the processing cost, and a 2013 University of Texas lecture cited by CSET put photolithography at half the cost of processing a 300 mm wafer against a quarter of a 150 mm one ⁷. Wafers are still produced in diameters of up to 300 mm ¹.

One fatal defect ruins far more silicon on a GPU die that fills a whole printed field than on a small chip, and extreme-ultraviolet printing stays in focus over only a very small range of heights (see Lithography), so flatness has to hold at every point on the disc.

Key evaluation criteria

- **Grade.** Chips need electronic-grade polysilicon, and none of the five major suppliers of it that Siltronic named for 2025 is Chinese ⁴.
- **Defect density** in the epitaxial layer. A big AI die loses more good silicon per defect than a small chip does, and SEMI's wafer group says the move to sub-3nm processes is raising requirements for wafer quality and consistency ¹.
- **Flatness and nanotopography**, the fine ripple across the surface, because extreme-ultraviolet exposure stays in focus over only a very small range of heights, and that has to hold across a 300 mm wafer.
- **Diameter**, where 300 mm carried 99.7 percent of world fab capacity at 45 nm and below in SEMI figures from November 2020 cited by CSET ⁷. Of all the wafer area shipped worldwide in 2025, 300 mm wafers made up an estimated 78.8 percent ²¹.
- **Contract structure**, since Siltronic expects continued price pressure in 2026 on sales outside its existing long-term agreements ¹².

FOUR THINGS TO REMEMBER

- Every chip starts on a wafer, a polished disc of pure silicon about 30 centimeters across.

⁷ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology (CSET) · 21 January 2021 [\[A\]](https://cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf)
cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf

¹ SEMI Reports 2025 Annual Worldwide Silicon Wafer Shipments and Revenue Results. PR Newswire · 10 February 2026 [\[A\]](https://prnewswire.com/news-releases/semi-reports-2025-annual-worldwide-silicon-wafer-shipments-an...)
prnewswire.com/news-releases/semi-reports-2025-annual-worldwide-silicon-wafer-shipments-an...

⁴ FOUNDATION OF DIGITAL LIFE Investor Presentation. Siltronic · 29 April 2026 [\[A\]](https://siltronic.com/fileadmin/investorrelations/2026/Q1/20260429_Siltronic_InvestorPresentation_...)
siltronic.com/fileadmin/investorrelations/2026/Q1/20260429_Siltronic_InvestorPresentation_...

²¹ 688783 20260421 6JVC. Sse [\[A\]](https://static.sse.com.cn/disclosure/listedinfo/announcement/c/new/2026-04-21/688783_20260421_6JVC...) static.sse.com.cn/disclosure/listedinfo/announcement/c/new/2026-04-21/688783_20260421_6JVC...

¹² Siltronic AG: Robust business performance in 2025 demonstrates resilience despite challenging conditions. Siltronic · 27 August 2026 [\[A\]](https://siltronic.com/en/press/press-releases/siltronic-ag-robust-business-performance-in-2025-dem...) siltronic.com/en/press/press-releases/siltronic-ag-robust-business-performance-in-2025-dem...

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- The top five wafer makers, in Japan, Taiwan, Germany and South Korea, served around 75 percent of the market in 2025.
 - Customers have to qualify a new wafer plant before they buy from it.
 - China makes most of the world's polysilicon, but none of the five major suppliers of the electronic-grade silicon chips need is Chinese.

Chemicals, Gases and Photoresist

A few hundred chemicals separate a blank wafer from a working chip. Japanese companies held 78 percent of world photoresist sales in 2023. Supply has been disrupted three times since 2019. After Japan's 2019 licensing of chemicals for South Korea and the 2022 invasion of Ukraine, buyers turned to stockpiles, other suppliers or local production. The third came from China, whose ban on germanium sales to the United States cut US imports of the metal by 67 percent in 2025.

IN PLAIN TERMS

Photoresist is a coating that changes wherever light hits it. A machine spins a coat of it, thinner than a soap bubble, across the wafer. Light shines through a stencil onto the coat, and a liquid wash then takes away the parts the light reached. What remains is a pattern, and the next machine cuts that pattern into the wafer beneath, a step called etching. A few hundred other gases and liquids lay down layers, strip them off and clean the wafer between steps. All of them have to be clean to about one stray metal atom in every trillion. Each formula is approved for one factory and one product at a time, and a new supplier has to earn that approval from scratch, so a second source takes years. Japanese companies held 78 percent of world photoresist sales in 2023, and no factory can swap it out quickly.

IN SHORT

Photoresist is the light-sensitive coating that carries a chip's pattern onto the wafer, and Japanese companies held 78 percent of world sales of it in 2023 ². When Japan put photoresist and two other chemicals under export licenses for South Korea in 2019, Korea bought more from other countries, and production of the chemicals rose at Korean firms and at Japanese companies' affiliates in South Korea ²². China restricts exports of gallium, a metal used in lasers, LEDs and some specialized chips ³⁰. In November 2025 it suspended its ban on US sales of gallium, germanium and antimony until 27 November 2026 ²⁷.

² METI, Semiconductor and digital industry strategy: future direction (半導体・デジタル産業戦略の今後の方向性), 23 December 2025. Ministry of Economy, Trade and Industry (Japan) · 23 December 2025 [\[A\]](https://meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/O014/handej14-4.pdf) meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/O014/handej14-4.pdf

²² The impact of export controls on international trade: evidence from the Japan–Korea trade dispute in the semiconductor industry. Research Institute of Economy, Trade and Industry (Japan) · 8 May 2023 [\[A\]](https://rieti.go.jp/en/columns/v01_0201.html) rieti.go.jp/en/columns/v01_0201.html

³⁰ Mineral Commodity Summaries 2026. U.S. Geological Survey · 5 February 2026 [\[A\]](https://pubs.usgs.gov/periodicals/mcs2026/mcs2026-gallium.pdf) pubs.usgs.gov/periodicals/mcs2026/mcs2026-gallium.pdf

²⁷ 商务部公告2025年第72号 公布调整实施商务部公告2024年第46号的决定. Ministry of Commerce of the People's Republic of China [\[A\]](https://mofcom.gov.cn/zwgk/zcfb/art/2025/art_5c68985a6b1a46778e2e8dbff1bb1601.html) mofcom.gov.cn/zwgk/zcfb/art/2025/art_5c68985a6b1a46778e2e8dbff1bb1601.html

CHOKEPOINT CARD		HIGH CONCENTRATION	MODERATELY HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY	PRICE OR MARKET SIZE	
High	Moderate Rated on photoresist, the hardest input in this stage, where Japanese companies held 78 percent of world sales in 2023.	Wafer fabrication materials were a \$45.8bn market in 2025 and packaging materials \$27.4bn, \$73.2bn in total	
WHO LEADS	JP JSR Owner of Inpria, a maker of metal-oxide resist for extreme-ultraviolet printing; a Japan Investment Corporation vehicle took 84.36% in an April 2024 tender offer JP Tokyo Ohka Kogyo Resist maker; ¥139,668m of sales in the first half of fiscal 2026 FR Air Liquide €2,465m of electronics revenue in 2025, 9.1% of group sales US Entegris \$3,196.6m of 2025 net sales; makes filters, polishing slurries, gas delivery systems and wafer carriers JP JX Advanced Metals Says it holds about 65% of sputtering targets for semiconductors as of fiscal 2026; the targets supply thin metal films such as the barrier and seed layers for copper wiring		
WHERE IT IS MADE	JP Japan Photoresist, ultra-pure hydrofluoric acid, sputtering targets, polishing slurries US United States Entegris filters, wafer carriers and polishing slurries; Qnity Electronics slurries, pads and resist; Air Products gases FR France Air Liquide electronics gases and precursors KR South Korea SK Materials nitrogen trifluoride, Dongjin resist, on-site gas for memory fabs CN China Gallium, germanium and antimony refining; growing wet chemicals and polishing slurries		
WHY SUBSTITUTION IS POSSIBLE	Photoresist is the light-sensitive coating that holds the printed pattern on the wafer. Each formula is approved for one layer of one product at one fab. A new supplier therefore has to develop its version together with the fab, one layer at a time. Korea shows how buyers respond to a cut. When Japan required individual export licenses for resist and two other chemicals in 2019, Korea imported more from the United States, Taiwan and Belgium, and output of the three chemicals rose at Korean firms and at Japanese companies' affiliates in Korea. Some of the American supply may have been Japanese material shipped by way of the United States. Japanese resist exports to Korea did not fall, possibly in part because Japan allowed three-year bulk licenses for some resist sales in December 2019.		
WHERE CHINA STANDS			
As of January 2021, CSET found that			

China made no photoresist for extreme-ultraviolet printing and was still developing resist for 193 nm printing. At the time it held under 5 percent of the photoresist market. In March 2026 the Chinese resist maker Hubei Dinglong said China had yet to reach large-scale production of advanced resist for 248 nm, 193 nm or extreme-ultraviolet printing. USGS put its share of world production of primary low-purity gallium at 99 percent in February 2026. Since August 2023 it has required licenses to export gallium and germanium. It banned their export to the United States in December 2024 and in November 2025 suspended that ban until 27 November 2026.	WHERE THE US STANDS American firms are strong in filters, containers, polishing slurries and gas delivery: Entegris, Qnity Electronics and Air Products. In photoresist, American companies ranked a distant second to Japanese companies by sales in 2023, and in 2021 JSR of Japan agreed to buy Inpria, an Oregon maker of resist for extreme ultraviolet.
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A modern fab is a chemical plant with lithography attached. Air Liquide alone supplies more than 200 molecules and roughly 50,000 cylinders a year ¹. A shortage of any one of them can stop a fab.

How it works

The resist has to change only where the light lands, and change fast enough that the scanner, the machine that projects the pattern, can expose each patch of the wafer in milliseconds. Since the 1990s the standard resist has been the chemically amplified resist. At 248 nm and 193 nm, a photon absorbed in the film can free an acid molecule, and nothing more happens until the wafer is baked. In the bake, each acid molecule sets off hundreds of reactions around itself that turn the film soluble, so a little light does a lot of chemistry. The wash then takes away the exposed film and leaves the rest. The light comes at 248 nm from a krypton fluoride laser or 193 nm from an argon fluoride laser shining through a layer of water, which sharpens the image.

That chemistry works less well with extreme ultraviolet (see Lithography). An absorbed extreme ultraviolet photon instead knocks electrons loose, and a cascade of lower-energy secondary electrons makes the chemical changes in the resist ³. A 13.5 nm photon carries about fourteen times the energy of a 193 nm one, so the same dose of light arrives as far fewer photons. With fewer photons, where each one happens to land matters, and that randomness shows up as ragged line edges and missing contact holes, the small wells that join one layer of wiring to the next. Resist makers answered with metal-oxide resists, built on clusters with a tin-oxide core, which absorb more of the extreme ultraviolet light than chemically amplified resists ⁴. In 2021 JSR agreed to buy Inpria, an Oregon maker of these resists ⁵.

1 Electronics | Air Liquide. Air Liquide [\[A\]](https://airliquide.com/group/activities/electronics) airliquide.com/group/activities/electronics

3 How Scientists Are Accelerating the Development of Next-Gen Microelectronics. Lawrence Berkeley National Laboratory · 21 August 2023 [\[A\]](https://newscenter.lbl.gov/2023/08/21/how-scientists-are-accelerating-next-gen-microelectronics) newscenter.lbl.gov/2023/08/21/how-scientists-are-accelerating-next-gen-microelectronics

4 INPRIA | A world leader world leader in metal oxide photoresist design, development and manufacturing. Inpria [\[A\]](https://inpria.com) inpria.com

5 JSR Agrees to Acquire EUV Pioneer Inpria Corporation | 2021 | News. JSR Corporation · 17 September 2021 [\[A\]](https://jsr.co.jp/jsr_e/news/2021/20210917.html) jsr.co.jp/jsr_e/news/2021/20210917.html

Everything else puts material on the wafer, takes it off, or keeps it clean. Bulk gases arrive by the metric ton, specialty gases in grams. Silane carries silicon into the chamber for deposition. A plasma tears nitrogen trifluoride into charged fragments, which scrub the chamber walls clean between wafers. Hydrofluoric acid cleans the wafer itself. Polishing slurries grind each new layer flat before the next goes on. Sputtering targets are slabs of pure metal; a plasma knocks atoms off them, and the atoms settle on the wafer as thin metal films, including the barrier and seed layers for copper wiring ⁶. The copper wiring itself is then filled in by electroplating ⁷. Filters and carriers keep contamination out.

Variants and trade-offs

RESIST CLASS	WAVELENGTH	WHERE IT IS USED	LIMIT
i-line novolak	365 nm	Packaging, mature nodes	Resolution
KrF chemically amplified	248 nm	Implant layers, thick films	Resolution
ArF immersion chemically amplified	193 nm	Most critical layers below 28 nm	Needs several exposures per layer
EUV chemically amplified	13.5 nm	Leading-edge single-exposure layers	Shot noise from too few photons
EUV metal-oxide	13.5 nm	High-NA tools, tightest pitches	Cost, defects, outgassing

Each resist class is specific to one kind of lithography, such as EUV, ArF immersion, ArF, KrF or i-line ⁸.

Who makes it

CSET's January 2021 brief, citing a 2019 estimate, gave Japan 90 percent of the semiconductor photoresist market, with the rest largely held by US and South Korean firms ⁸. A separate Fuji Keizai survey, relayed in the December 2025 strategy deck of Japan's Ministry of Economy, Trade and Industry, measures sales by company nationality and puts Japanese companies at 77 percent in 2021 and 78 percent in 2023, with American and South Korean companies next ².

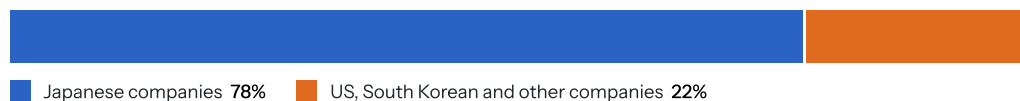
⁶ PVD | Applied Materials. Applied Materials [\[A\]](https://appliedmaterials.com/eu/en/semiconductor/semiconductor-technologies/pvd.html) appliedmaterials.com/eu/en/semiconductor/semiconductor-technologies/pvd.html

⁷ SABRE Product Family - Lam Research. Lam Research · 11 August 2017 [\[A\]](https://lamresearch.com/product/sabre) lamresearch.com/product/sabre

⁸ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology (CSET) · 21 January 2021 [\[A\]](https://cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf) cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf

² METI, Semiconductor and digital industry strategy: future direction (半導体・デジタル産業戦略の今後の方向性), 23 December 2025. Ministry of Economy, Trade and Industry (Japan) · 23 December 2025 [\[A\]](https://meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/0014/handeji14-4.pdf) meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/0014/handeji14-4.pdf

Photoresist sales share by company nationality, 2023 %



Source: METI, December 2025, from Fuji Keizai data

CSET's January 2021 brief lists JSR, Tokyo Ohka Kogyo, Shin-Etsu Chemical, Fujifilm and Sumitomo Chemical of Japan as resist makers, along with Dongjin of South Korea, the American firms DuPont, EMD Performance Materials and Inpria, and four Chinese firms ⁸. Qnity Electronics, the former DuPont electronics business, says in its 2025 annual report that it offers lithography materials for every wavelength, including extreme ultraviolet ⁹. In its 2025 annual report summary, the Chinese firm Hubei Dinglong said China had yet to reach large-scale production of advanced resist for 248 nm, 193 nm or extreme-ultraviolet printing, though three of its own resists for 248 nm and 193 nm printing had moved into stable volume supply ¹⁰.

A vehicle of Japan Investment Corporation, a state-backed fund, took 84.36 percent of JSR's shares at ¥4,350 each in a tender offer that closed on 16 April 2024 ¹¹. JSR's shares were delisted from the Tokyo Stock Exchange on 25 June 2024 ¹².

Tokyo Ohka Kogyo sold ¥139,668 million in the first half of fiscal 2026, up 25.1 percent, as strong demand for AI servers in data centers raised demand for chips ¹³. Fujifilm planned to raise its polishing-slurry capacity at Kumamoto by about 30 percent from January 2025 ¹⁴. It also scheduled new production and quality-evaluation equipment for extreme-ultraviolet resist at Shizuoka and Pyeongtaek to start in October 2025 ¹⁵.

Wafer fabrication materials sold \$45.8 billion in 2025 and packaging materials \$27.4 billion ¹⁶.

In electronic gases, CSET named Merck, Air Products and Air Liquide as the market leaders in January 2021 ⁸. Air Liquide's electronics arm alone sold €2,465 million in 2025, 9.1 percent of group revenue ¹. Smaller firms specialize in single

⁸ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology (CSET) · 21 January 2021 [\[A\]](https://cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf)
cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf

⁹ Qnity Electronics, Inc., Form 10-K annual report for the period ended 2025-12-31 (10-K). U.S. Securities and Exchange Commission (filing by Qnity Electronics, Inc.) · 26 February 2026 [\[A\]](https://sec.gov/Archives/edgar/data/2058873/000205887326000010/q-20251231.htm)
sec.gov/Archives/edgar/data/2058873/000205887326000010/q-20251231.htm

¹⁰ 湖北鼎龙控股股份有限公司2025 年年度报告摘要. Cninfo · 26 March 2026 [\[A\]](https://static.cninfo.com.cn/finalpage/2026-03-27/1225036148.PDF)
static.cninfo.com.cn/finalpage/2026-03-27/1225036148.PDF

¹¹ April 17, 2024 Japan Investment Corporation. Japan Investment Corporation · 17 April 2024 [\[A\]](https://jiccapi.com/en/news/assets/E_20240417_JIC_JICC_PressRelease.pdf)
jiccapi.com/en/news/assets/E_20240417_JIC_JICC_PressRelease.pdf

¹² Announcement of Delisting of Shares of JSR Corporation. JSR Corporation · 19 June 2024 [\[A\]](https://jsr.co.jp/jsr_e/news/assets/pdf/20240624_01_e.pdf)
jsr.co.jp/jsr_e/news/assets/pdf/20240624_01_e.pdf

¹³ Consolidated Financial Results for the Second Quarter (Interim) of the Fiscal Year Ending December 31, 2026 [J-GAAP]. Tokyo Ohka Kogyo · 5 August 2026 [\[A\]](https://tok.co.jp/application/files/7417/8598/0069/q2_2612_en.pdf)
tok.co.jp/application/files/7417/8598/0069/q2_2612_en.pdf

¹⁴ Fujifilm to Enhance its Production Capacity of Advanced Semiconductor Material CMP Slurries at the Kumamoto Site. Fujifilm · 5 December 2024 [\[A\]](https://fujifilm.com/jp/en/news/hq/11942)
fujifilm.com/jp/en/news/hq/11942

¹⁵ Fujifilm Launches EUV Resist and EUV Developer. Fujifilm · 29 October 2024 [\[A\]](https://fujifilm.com/jp/en/news/hq/11842)
fujifilm.com/jp/en/news/hq/11842

¹⁶ Global Semiconductor Materials Market Revenue Reaches Record \$73.2 Billion in 2025, SEMI Reports. PR Newswire · 12 May 2026 [\[A\]](https://prnewswire.com/news-releases/global-semiconductor-materials-market-revenue-reaches-record-...)
prnewswire.com/news-releases/global-semiconductor-materials-market-revenue-reaches-record-...

¹ Electronics | Air Liquide. Air Liquide [\[A\]](https://airliquide.com/group/activities/electronics)
airliquide.com/group/activities/electronics

molecules: SK Materials in nitrogen trifluoride, Kanto Denka in fluorine chemistry, Stella Chemifa and Morita in ultra-high-purity hydrofluoric acid.

CSET's January 2021 brief, drawing on 2019 market reports, put five firms at more than 60 percent of wet chemicals and DuPont and Cabot Microelectronics at about 56 percent of a \$790 million market in polishing slurries ⁸. The same Fuji Keizai survey that METI relayed counts sales by company nationality, and it puts Japanese companies at 51 percent of polishing-slurry sales and 59 percent of high-purity cleaning-liquid sales in 2023, up from 49 percent of each in 2021 ². Cabot Microelectronics renamed itself CMC Materials in October 2020 ¹⁷. Entegris completed its purchase of CMC Materials on 6 July 2022 ¹⁸. DuPont separated its electronics business into an independent company, Qnity Electronics, on 1 November 2025 ¹⁹. Qnity sells polishing slurries and pads ²⁰. In sputtering targets for semiconductors, JX Advanced Metals puts its own share of the world market at about 65 percent as of fiscal 2026 ²¹.

The chokepoint

Supply at this stage has been disrupted three times since 2019, twice by governments and once by a war.

In July 2019 Japan put photoresist, hydrogen fluoride and fluorinated polyimide under individual export licenses for South Korea. It had supplied more than 90 percent of Korean imports of two of the three, and hydrogen fluoride exports fell 87.9 percent ²². Japanese photoresist exports to Korea did not fall, possibly in part because Japan allowed three-year bulk licenses for some resist sales in December 2019 ²². South Korea bought more hydrogen fluoride from the United States and Taiwan and more photoresist from Belgium, and production of all three chemicals rose inside the country ²². The same study found that Japanese hydrogen fluoride exports to the United States rose, which may mean some Japanese supply reached Korea by way of the United States ²². The rise in Korean output came both from Korean firms and from Japanese companies' affiliates in South Korea ²². Japan

⁸ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology (CSET) · 21 January 2021 [\[A\]](https://cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf) cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf

² METI, Semiconductor and digital industry strategy: future direction (半導体・デジタル産業戦略の今後の方向性), 23 December 2025. Ministry of Economy, Trade and Industry (Japan) · 23 December 2025 [\[A\]](https://meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/0014/handeji14-4.pdf) meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/0014/handeji14-4.pdf

¹⁷ CMC Materials, Inc., Form 8-K current report for the period ended 2020-09-28 (8-K). U.S. Securities and Exchange Commission (filing by CMC Materials, Inc.) · 1 October 2020 [\[A\]](https://sec.gov/Archives/edgar/data/1102934/000110293420000048/ccmp-20201001xex991.htm) sec.gov/Archives/edgar/data/1102934/000110293420000048/ccmp-20201001xex991.htm

¹⁸ ENTEGRIS INC, Form 8-K current report for the period ended 2022-07-06. U.S. Securities and Exchange Commission (filing by ENTEGRIS INC) · 6 July 2022 [\[A\]](https://sec.gov/Archives/edgar/data/1101302/000114036122025275/ny20004647x3_ex99-1.htm) sec.gov/Archives/edgar/data/1101302/000114036122025275/ny20004647x3_ex99-1.htm

¹⁹ Default. Dupont [\[A\]](https://investors.dupont.com/news-and-media/press-release-details/2025/DuPont-Completes-Separation...) investors.dupont.com/news-and-media/press-release-details/2025/DuPont-Completes-Separation...

²⁰ Chemical Mechanical Planarization (CMP) Materials for Semiconductor. Qnityelectronics [\[A\]](https://qnityelectronics.com/semiconductor-cmp.html) qnityelectronics.com/semiconductor-cmp.html

²¹ Quick Guide to JX Advanced Metals | Corporate Overview. JX Advanced Metals [\[A\]](https://jx-nmm.com/english/company/glance) jx-nmm.com/english/company/glance

²² The impact of export controls on international trade: evidence from the Japan-Korea trade dispute in the semiconductor industry. Research Institute of Economy, Trade and Industry (Japan) · 8 May 2023 [\[A\]](https://rieti.go.jp/en/columns/v01_0201.html) rieti.go.jp/en/columns/v01_0201.html

ended the individual licenses on 23 March 2023, when it put exports of the three chemicals to South Korea under its bulk export license system ²³.

In 2022 Russia invaded Ukraine, which supplied about 70 percent of the world's neon and 90 percent of the semiconductor-grade neon used by US industry ²⁴. Many chipmakers had added to their gas stockpiles after Russia annexed Crimea in 2014, and Samsung, SK Hynix, Renesas and Rohm reported adequate neon supplies from China ²⁴.

China's export controls fall on the metals. Beijing announced export licenses for gallium and germanium on 3 July 2023, in force from 1 August ²⁵. On 3 December 2024 it said it would in principle grant no licenses to export gallium, germanium, antimony or superhard materials to the United States ²⁶. On 9 November 2025 it suspended that ban until 27 November 2026 ²⁷. Under a trade deal set out by the White House on 1 November 2025, China also agreed to issue general licenses for exports of gallium, germanium and antimony for the benefit of US end users and their suppliers ²⁸.

In the United States, germanium goes mainly into fiber optics, infrared optics, semiconductors and solar cells, and radiation detectors ²⁹. Of the gallium used in the United States, 73 percent went into integrated circuits built on gallium arsenide or gallium nitride, and 26 percent into optoelectronic devices such as LEDs and laser diodes ³⁰. Germanium metal averaged \$4,100 a kilogram in 2025 against \$1,392 in 2023, and US imports of the metal fell 67 percent in 2025 because of China's ban ²⁹. The US Geological Survey estimated that a total Chinese ban on gallium and germanium exports could cut US GDP by \$3.4 billion ³¹.

23 指定されたページまたはファイルは存在しません (METI/経済産業省) . Go [A](https://meti.go.jp/english/press/2023/0323_001.html) meti.go.jp/english/press/2023/0323_001.html

24 Russia's Invasion of Ukraine Impacts Gas Markets Critical to Chip Production | Perspectives on Innovation. Center for Strategic and International Studies [A](https://csis.org/blogs/perspectives-innovation/russias-invasion-ukraine-impacts-gas-markets-critic...) csis.org/blogs/perspectives-innovation/russias-invasion-ukraine-impacts-gas-markets-critic...

25 商务部 海关总署公告2023年第23号 关于对镓、锗相关物项实施出口管制的公告. Ministry of Commerce of the People's Republic of China [A](https://mofcom.gov.cn/zcfb/dwmygl/art/2023/art_52b9a321087f402bb3d310d18b07967e.html) mofcom.gov.cn/zcfb/dwmygl/art/2023/art_52b9a321087f402bb3d310d18b07967e.html

26 商务部公告2024年第46号 关于加强相关两用物项对美国出口管制的公告. Ministry of Commerce of the People's Republic of China [A](https://mofcom.gov.cn/zwgk/zcfb/art/2024/art_3d5e990b43424e60828030f58a547b60.html) mofcom.gov.cn/zwgk/zcfb/art/2024/art_3d5e990b43424e60828030f58a547b60.html

27 商务部公告2025年第72号 公布调整实施商务部公告2024年第46号的决定. Ministry of Commerce of the People's Republic of China [A](https://mofcom.gov.cn/zwgk/zcfb/art/2025/art_5c68985a6b1a46778e2e8dbff1bb1601.html) mofcom.gov.cn/zwgk/zcfb/art/2025/art_5c68985a6b1a46778e2e8dbff1bb1601.html

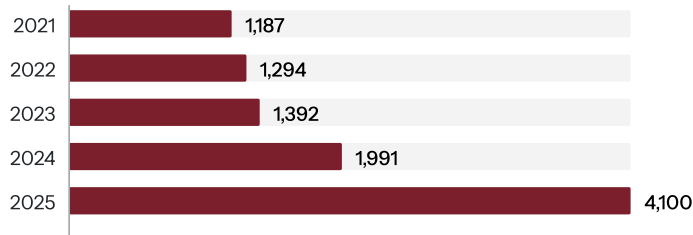
28 Fact Sheet: President Donald J. Trump Strikes Deal on Economic and Trade Relations with China. The White House · 1 November 2025 [A](https://whitehouse.gov/fact-sheets/2025/11/fact-sheet-president-donald-j-trump-strikes-deal-on-eco...) whitehouse.gov/fact-sheets/2025/11/fact-sheet-president-donald-j-trump-strikes-deal-on-eco...

29 Mineral Commodity Summaries 2026. U.S. Geological Survey · 5 February 2026 [A](https://pubs.usgs.gov/periodicals/mcs2026/mcs2026-germanium.pdf) pubs.usgs.gov/periodicals/mcs2026/mcs2026-germanium.pdf

30 Mineral Commodity Summaries 2026. U.S. Geological Survey · 5 February 2026 [A](https://pubs.usgs.gov/periodicals/mcs2026/mcs2026-gallium.pdf) pubs.usgs.gov/periodicals/mcs2026/mcs2026-gallium.pdf

31 USGS Critical Minerals Study: Bans on Gallium and Germanium Exports Could Cost the U.S. Billions. USGS [A](https://usgs.gov/news/national-news-release/usgs-critical-minerals-study-bans-gallium-and-germanium...) usgs.gov/news/national-news-release/usgs-critical-minerals-study-bans-gallium-and-germanium...

Germanium metal, annual average price (\$/kg). China licensed exports from August 2023, banned US shipments in December 2024 and suspended the ban from November 2025 to 27 November 2026 \$/KG



Source: USGS Mineral Commodity Summaries, February 2026 (Argus Media prices)

The slower risk is the European Union's proposed restriction on PFAS, the long-lived fluorinated chemicals. The five national authorities behind it, from Denmark, Germany, the Netherlands, Norway and Sweden, evaluated more than 5,600 comments and updated the proposal, which ECHA, the EU chemicals agency, published on 20 August 2025 ³². In March 2026 ECHA's two scientific committees backed an EU-wide restriction with targeted derogations, one in a final opinion and one in a draft, and their evaluation is due to finish by the end of 2026 ³³. These chemicals are everywhere in a fab: photoacid generators, etch gases, chamber liners, pump seals and filter membranes are all fluorinated. The updated proposal assessed options that would let electronics and semiconductor makers keep using PFAS where the risks can be controlled, and the European Commission will decide in consultation with the member states ³².

Key evaluation criteria

- **Purity, in parts per trillion** of metallic contamination, a million times finer than parts per million, which is the spec that keeps entrants out.
- **Qualification lock-in:** a resist or slurry is approved for one layer of one product at one fab, so switching costs are counted in tape-outs.
- **Photon efficiency** for EUV resists: how much light the resist absorbs sets the dose, the dose sets how many wafers an hour the scanner prints, and too few photons per dose set the defect rate, which is the case for metal-oxide chemistry.
- **Transportability:** bulk gases are often made on site at the fab, while specialty gases travel in cylinders and can be embargoed.
- **Byproduct exposure:** gallium is recovered mostly as a byproduct of processing bauxite ³⁰. Germanium comes from certain zinc ores and coal deposits, so supply of both depends on another industry's economics ²⁹.

32 Echa publishes updated pfas restriction proposal (European Chemicals Agency website). European Chemicals Agency ^A
echa.europa.eu/-/echa-publishes-updated-pfas-restriction-proposal

33 ECHA supports PFAS restriction with targeted derogations. European Chemicals Agency · 26 March 2026 ^A
echa.europa.eu/-/echa-supports-pfas-restriction-with-targeted-derogations

30 Mineral Commodity Summaries 2026. U.S. Geological Survey · 5 February 2026 ^A pubs.usgs.gov/periodicals/mcs2026/mcs2026-gallium.pdf

29 Mineral Commodity Summaries 2026. U.S. Geological Survey · 5 February 2026 ^A pubs.usgs.gov/periodicals/mcs2026/mcs2026-germanium.pdf

FOUR THINGS TO REMEMBER

- Photoresist holds the pattern printed by light so the next step can etch it into the wafer.
- Japanese companies held 77 percent of world photoresist sales in 2021 and 78 percent in 2023.
- Each resist is approved for one layer of one product at one factory, so a new supplier takes years.
- China has required licenses to export gallium and germanium since August 2023.

Lithography

The most concentrated stage in the chain. One firm in the Netherlands builds every extreme ultraviolet scanner in the world, the machine that prints the finest circuit layers. It recognized revenue on 48 of them in 2025 and in July 2026 put its 2026 capacity at around 65 of the standard model, which sells for around \$200 million.

IN PLAIN TERMS

Lithography prints the pattern of a circuit onto the wafer. A machine holds a stencil of one layer of the circuit up to a lamp and projects the image, four times smaller, onto the silicon. The shorter the wavelength of the light, the finer the lines a machine can print. A machine can still print lines several times narrower than its light's wavelength, and ASML says its 193-nanometer argon fluoride light prints features as small as 38 nanometers. Air soaks up the shortest light now in use, so the machine has to print in a vacuum. Only one company makes a machine that prints with it, and it is Dutch. Export controls are government rules on who a company may sell to. Every advanced chip passes through that firm's machines, so a rule aimed at it reaches all advanced chipmaking.

IN SHORT

Only one company, the Dutch firm ASML, has mastered extreme ultraviolet (EUV) lithography at scale, and the most advanced AI chips depend on it ²¹. Export controls block ASML from shipping EUV machines to Chinese chipmakers ²¹. In September 2025 CSIS judged that EUV remained "firmly out of reach" for China despite massive state investment ²¹. A Chinese prototype reported in December 2025 made EUV light but had printed no chip ²⁹. China's share of ASML's system sales fell from 41 percent in 2024 to 33 percent in 2025 ⁷.

²¹ Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements | Strategic Technologies Blog. Center for Strategic and International Studies [\[A\] csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chines...](https://www.csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chines...)

²⁹ How China built its 'Manhattan Project' to rival the West in AI chips. Reuters · 17 December 2025 [\[B\] reuters.com/world/china/how-china-built-its-manhattan-project-rival-west-ai-chips-2025-12-17](https://www.reuters.com/world/china/how-china-built-its-manhattan-project-rival-west-ai-chips-2025-12-17)

⁷ Presentation Investor Relations Q4 2025. ASML · 27 January 2026 [\[A\]](https://www.asml.com/m/3136300aa4999bc1/original/2026_01_28_Presentation-Investor-Relations-Q...)
ourbrand.asml.com/m/3136300aa4999bc1/original/2026_01_28_Presentation-Investor-Relations-Q...

CHOKEPOINT CARD		EXTREME CONCENTRATION	VERY HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY		PRICE OR MARKET SIZE
Extreme	Very hard		About \$200M
	ASML is the only maker of EUV scanners, Zeiss is its sole supplier of their mirrors, and a state-funded Chinese team has made the light but has not printed a chip.		for a standard EUV scanner, \$350-400M for the newer High-NA version and about \$60M for a DUV tool, according to Reuters. ASML does not publish per-system prices
WHO LEADS			
	NL	ASML 100% of EUV (extreme ultraviolet) and above 80% of DUV (deep ultraviolet); EUV was 48% of its own 2025 system revenue and immersion DUV 42%	
	JP	Nikon 22 new chip lithography systems in the year to March 2026, in a 2025 market Nikon estimates at 570 units	
	JP	Canon i-line and krypton fluoride tools for older, coarser layers, plus a nanoimprint system that Canon says was the first commercialized for chipmaking	
WHERE IT IS MADE			
	NL	Netherlands ASML design and final assembly, Veldhoven	
	DE	Germany Zeiss SMT optics, Oberkochen; Trumpf carbon dioxide lasers that drive the light source, Ditzingen	
	US	United States ASML light-source research and manufacturing, San Diego	
	JP	Japan Nikon and Canon deep ultraviolet scanners and steppers	
WHY SUBSTITUTION IS SLOW	Nobody else makes EUV scanners. A newcomer would first have to make mirrors a meter wide, polished smooth to within tens of picometers, a picometer being a trillionth of a meter. It would also need a light source that hits tin droplets with a laser 50,000 times a second. An attempt in China, reported in December 2025, had made extreme-ultraviolet light but had printed no chip. In September 2025, before that report, CSIS judged that EUV remained firmly out of reach for China despite massive state investment.		
WHERE CHINA STANDS	WHERE THE US STANDS		
Export controls block ASML from shipping EUV scanners to Chinese foundries. In September 2025 CSIS judged that EUV remained firmly out of reach for China despite massive state investment. That came before a December 2025 report of a Chinese prototype that made EUV light but had printed no chip. Shanghai Aishengna Electronic Technology Group, a state-owned firm registered in 2023, is reported to have started producing Chinese immersion DUV scanners in 2026. SMEE, the older Chinese supplier, has its largest share in i-line scanners, the coarsest kind, and even there holds about 4 percent of the world market.	No American firm makes scanners. The US government also limits who may buy them, through rules on the American-made parts inside each machine and its entity list of firms that may not be supplied.		

Every transistor in an AI accelerator gets its shape from a machine one company builds. ASML sold 327 lithography systems in 2025, 48 of them extreme ultraviolet¹. Nobody else makes EUV systems².

How it works

The stencil is a photomask, the film is photoresist and the machine is a scanner (see Photomasks and pellicles).

The wafer is coated with photoresist, a film that changes wherever light touches it. The mask holds one layer of the circuit as a pattern of clear and dark areas, drawn four times larger than life. The machine shines light through the mask, shrinks the image four times with a lens, and lands it on the film. A wash then removes the film where the light hit, and the pattern is left standing on the wafer for the next machine to etch in or fill with metal. Then the film is stripped and the next mask goes in. A chip takes dozens of masks, one per layer.

The image from one mask covers a patch about 26 by 33 mm, so the wafer moves under the lens one patch at a time, close to a hundred patches per wafer. ASML's own throughput rating for an EUV scanner assumes 96 of them⁴. Before the wafer is exposed, the machine measures alignment marks printed in earlier layers so the new layer lines up with them, and ASML rates the NXE:3400B's matched-machine overlay at 2 nm⁴.

Finer lines need shorter light. The finest light now in use, at 13.5 nm, is stopped by glass and by air, so an EUV scanner works in a vacuum and uses mirrors instead of lenses, and its masks are mirrors too⁵. The older machines use light more than fourteen times longer³. The immersion type among them gains extra sharpness by filling the gap between lens and wafer with water⁶.

When one exposure cannot draw a pattern finely enough, the layer is printed with two, three or four masks instead. Each extra pass costs a mask, machine time and a chance to misalign, and ASML says one EUV exposure per layer cuts masks and process steps and lowers cost².

Variants and trade-offs

¹ ASML 2025 Annual Report. ASML · 24 February 2026 [\[A\] ourbrand.asml.com/m/419103cb23dfeaa4/original/asml-2025-annual-report-financial-performance...](https://ourbrand.asml.com/m/419103cb23dfeaa4/original/asml-2025-annual-report-financial-performance)

² ASML 2025 Annual Report. ASML · 24 February 2026 [\[A\] ourbrand.asml.com/m/8ab959d4926657b/original/asml-2025-annual-report-strategic-report-sect...](https://ourbrand.asml.com/m/8ab959d4926657b/original/asml-2025-annual-report-strategic-report-sect...)

⁴ TWINSCAN NXE:3400B: EUV lithography systems. ASML [\[A\] asml.com/en/products/euv-lithography-systems/twinscan-nxe3400b](https://asml.com/en/products/euv-lithography-systems/twinscan-nxe3400b)

⁵ ASML EUV lithography systems. ASML [\[A\] asml.com/en/products/euv-lithography-systems](https://asml.com/en/products/euv-lithography-systems)

³ All about light and lasers in lithography. ASML [\[A\] asml.com/en/technology/lithography-principles/light-and-lasers](https://asml.com/en/technology/lithography-principles/light-and-lasers)

⁶ Lenses & mirrors - Lithography principles. ASML [\[A\] asml.com/en/technology/lithography-principles/lenses-and-mirrors](https://asml.com/en/technology/lithography-principles/lenses-and-mirrors)

Deep ultraviolet

Deep ultraviolet (DUV) light comes from gas lasers: 248 nanometers from krypton fluoride (KrF), 193 from argon fluoride (ArF), shone through air or water ³. These tools still dominate by volume. Of ASML's 327 systems in 2025, 131 were ArF immersion, 78 KrF and 16 ArF dry, all deep ultraviolet, and another 54 were older i-line tools ⁷. The i-line tools use 365 nm light from a mercury lamp, and ASML says they print features as small as 220 nm ³. A DUV scanner costs roughly \$60 million. DUV is the one tier with named competitors, Nikon and Canon, and ASML still holds above 80 percent of it ⁸.

Immersion is the contested tier, because without EUV a fab needs NXT:2000i-class scanners and several passes per layer to reach leading-edge logic, and that is the tier Dutch export licensing covers.

Extreme ultraviolet

The 13.5 nm light comes from shooting molten tin droplets from a generator and hitting each droplet twice, with a low-intensity pulse to flatten it and then a more powerful one that vaporizes it into plasma, a process repeated 50,000 times a second ³. Zeiss mirrors carry it to the wafer, and the largest are a meter across, smooth down to tens of picometers, a picometer being a thousandth of a nanometer ⁶.

Brighter light means more wafers an hour, and ASML ran the first 1,000-watt EUV source in April 2025 ². Its TWINSCAN NXE:3800E now ships at its full 220 wafers an hour, 37 percent better than the NXE:3600D ².

High-NA EUV

High numerical aperture (High-NA) raises the aperture from 0.33 to 0.55 and cuts the smallest printable feature from 13 nm to 8 nm ⁹. Its optics shrink the mask image four times in one direction and eight in the other, halving the patch of wafer one exposure covers and doubling the exposures per wafer ⁹. The second-generation TWINSCAN EXE:5200B runs at 175 wafers an hour, 60 percent above the EXE:5000 ².

Reuters puts a standard EUV tool at around \$200 million and a High-NA machine at \$350 to \$400 million, prices ASML does not publish ⁸.

³ All about light and lasers in lithography. ASML [\[A\]](https://www.asml.com/en/technology/lithography-principles/light-and-lasers) asml.com/en/technology/lithography-principles/light-and-lasers

⁷ Presentation Investor Relations Q4 2025. ASML · 27 January 2026 [\[A\]](https://ourbrand.asml.com/m/3136300aa4999bc1/original/2026_01_28_Presentation-Investor-Relations-Q4-2025) ourbrand.asml.com/m/3136300aa4999bc1/original/2026_01_28_Presentation-Investor-Relations-Q...

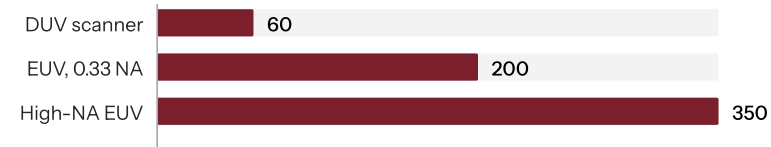
⁸ Explainer: The \$400 million ASML 'printers' key for the AI chip boom. Reuters · 28 January 2026 [\[B\]](https://www.reuters.com/world/asia-pacific/250-million-asml-printer-behind-nvidias-chips-2026-07-28) reuters.com/world/asia-pacific/250-million-asml-printer-behind-nvidias-chips-2026-07-28

⁶ Lenses & mirrors - Lithography principles. ASML [\[A\]](https://www.asml.com/en/technology/lithography-principles/lenses-and-mirrors) asml.com/en/technology/lithography-principles/lenses-and-mirrors

² ASML 2025 Annual Report. ASML · 24 February 2026 [\[A\]](https://ourbrand.asml.com/m/8ab959d4926657b/original/asml-2025-annual-report-strategic-report-sect...) ourbrand.asml.com/m/8ab959d4926657b/original/asml-2025-annual-report-strategic-report-sect...

⁹ 5 things you should know about High NA in EUV. ASML · 25 January 2024 [\[A\]](https://www.asml.com/en/company/stories/2024/5-things-high-na-euv) asml.com/en/company/stories/2024/5-things-high-na-euv

What one lithography system costs. The High-NA figure is quoted as a \$350-400M range; the bar shows the low end \$M



Source: Reuters explainer on ASML's lithography machines, 28 July 2026

Intel and TSMC have chosen differently on High-NA:

- **Intel Foundry** says it uses High-NA in volume production for select layers of some Intel 18A products ¹⁰. It installed the first EXE:5200B ¹¹. By September 2026 it had run more than one million wafers on High-NA tools, a count that includes tool testing and research as well as volume production ¹⁰.
- **TSMC** waited, and now says it will use High-NA in high-volume manufacturing from 2030 ¹².

ASML recognized four EXE systems in sales in 2025 against two in 2024 ¹. In its 2025 annual report, filed in February 2026, ASML said it expected the platform to start supporting high-volume manufacturing in 2027 ¹³. On 8 September 2026 it announced with TSMC a move to 12-inch photomasks to remove stitching constraints, aiming for a pilot mask line by 2031 and 12-inch High-NA systems in production by 2033 ¹².

EUV systems ASML recognized in sales each year TOOLS



Source: ASML 2025 annual report (2024 and 2025); 2023 from ASML's Q4 2023 investor presentation

10 Intel Foundry and ASML Accelerate Industry Readiness for High-NA EUV. Intel · 7 September 2026 [A](https://www.intel.com/content/www/us/en/newsroom/news/intel-foundry/intel-foundry-asml-accelerate-indu...)
[intel.com/content/www/us/en/newsroom/news/intel-foundry/intel-foundry-asml-accelerate-indu...](https://www.intel.com/content/www/us/en/newsroom/news/intel-foundry/intel-foundry-asml-accelerate-indu...)

11 High NA EUV reaches new readiness milestone with first high-volume Logic product. ASML · 15 July 2026 [A](https://www.asml.com/en/news/press-releases/2026/high-na-euv-reaches-new-readiness-milestone)
[asml.com/en/news/press-releases/2026/high-na-euv-reaches-new-readiness-milestone](https://www.asml.com/en/news/press-releases/2026/high-na-euv-reaches-new-readiness-milestone)

12 ASML and TSMC Announce Initiative to Pioneer Industry Transition to Large-Format Photomasks for High NA EUV. TSMC · 8 September 2026 [A](https://www.pr.tsmc.com/english/news/3338)
[pr.tsmc.com/english/news/3338](https://www.pr.tsmc.com/english/news/3338)

1 ASML 2025 Annual Report. ASML · 24 February 2026 [A](https://ourbrand.asml.com/m/419103cb23dfeaa4/original/asml-2025-annual-report-financial-performanc...)
ourbrand.asml.com/m/419103cb23dfeaa4/original/asml-2025-annual-report-financial-performanc...

13 ASML HOLDING NV, Form 6-K report of foreign private issuer for the period ended 2025-12-31 (6-K). U.S. Securities and Exchange Commission (filing by ASML HOLDING NV) · 25 February 2026 [A](https://www.sec.gov/Archives/edgar/data/937966/000162828026011377/asml-2025xannualxreportx.htm)
[sec.gov/Archives/edgar/data/937966/000162828026011377/asml-2025xannualxreportx.htm](https://www.sec.gov/Archives/edgar/data/937966/000162828026011377/asml-2025xannualxreportx.htm)

Who makes it

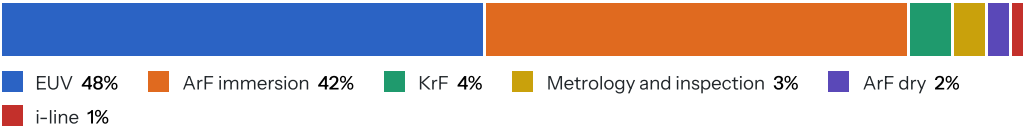
ASML took EUR 32.7 billion in net sales in 2025 at a 52.8 percent gross margin ¹, and in July 2026 raised its 2026 forecast to EUR 43 to 45 billion at 54 to 56 percent ¹⁴. It assembles more than it makes, listing 5,100 suppliers ¹³. Four of them make the main parts of the EUV machine:

- **Zeiss SMT**, Oberkochen, makes the illumination system and the six-mirror projection optics ¹⁵.
- **Trumpf**, Ditzingen, makes the carbon dioxide drive laser, which amplifies a few watts to 40 kilowatts ¹⁶.
- **ASML San Diego**, which includes the light-source maker Cymer that ASML bought in 2013, designs the source where the laser turns tin into plasma, and builds the droplet generator ¹⁷.
- **VDL ETG** builds the frames that suspend and position the mirrors ¹⁸.

ASML says the production capacity of Zeiss, its sole supplier of optics, limits how many lithography systems it can build ¹³.

Nikon and Canon are specialists now. Nikon sold 22 new chip lithography systems in the year to March 2026, into a market it sizes at 570 units for 2025, and its Precision Equipment business made an operating loss ¹⁹. Canon's alternative is nanoimprint, where the FPA-1200NZ2C stamps the pattern instead of projecting it, down to a 14 nm linewidth ²⁰. Canon delivered one in 2024 to the Texas Institute for Electronics, to be used for research and prototypes ²⁰.

ASML net system sales by technology, 2025 %



Source: ASML Q4 2025 investor presentation

1 ASML 2025 Annual Report. ASML · 24 February 2026 ourbrand.asml.com/m/419103cb23dfeaa4/original/asml-2025-annual-report-financial-performance...

14 Press Release Financial Results Q2 2026. ASML · 14 July 2026 ourbrand.asml.com/asset/c8dbf3fc-4c5e-4406-83f6-27694b138245/Press-Release-Financial-Resul...

13 ASML HOLDING NV, Form 6-K report of foreign private issuer for the period ended 2025-12-31 (6-K). U.S. Securities and Exchange Commission (filing by ASML HOLDING NV) · 25 February 2026 sec.gov/Archives/edgar/data/937966/000162828026011377/asml-2025xannualreportx.htm

15 EUV lithography and technology. Carl Zeiss zeiss.com/semiconductor-manufacturing-technology/inspiring-technology/euv-lithography.html

16 Good things come in ever-smaller packages. TRUMPF trumpf.com/en_US/products/lasers/euv-drive-laser

17 Explore ASML San Diego. ASML asml.com/en/company/about-asml/locations/san-diego

18 Vdl etg builds complex frames for zeiss. Archive web.archive.org/web/20240726075938/https://www.vdlgroep.com/en/news/vdl-etg-builds-complex...

19 FINANCIAL RESULTS The Year Ended March 31,2026. Nikon · 21 May 2026 nikon.com/content/dam/web-assets/nikoncom/company/local/global/en/ir/ir_library/result/pdf...

20 Canon delivers FPA -1200NZ2C nanoimprint lithography system for semiconductor manufacturing to the Texas Institute for Electronics. Canon · 26 September 2024 global.canon/en/news/2024/20240926.html

Controls and China's answer

Export controls bar EUV from Chinese foundries ²¹. In September 2025, before the Chinese prototype described below was reported, CSIS judged that EUV remained "firmly out of reach" for China despite massive state investment ²¹. Below EUV, the restrictions arrived in this order:

- **Dutch national licensing** of advanced DUV took effect on 1 September 2023 ²².
- **A US rule** published on 25 October 2023 put certain immersion scanners bound for advanced chipmaking under US export rules if they held any American content at all, unless the country they were first exported from already controlled them ²³.
- **A partial license revocation** disclosed on 1 January 2024 stopped NXT:2050i and NXT:2100i shipments to a few Chinese customers ²⁴.
- **The Netherlands widened its licensing** from 7 September 2024 ²². On 15 January 2025 it announced that from 1 April 2025 the license requirement would also cover a very limited number of further goods, among them specific measuring and inspection equipment ²⁵.
- **The BIS Affiliates Rule** extended entity-list controls to affiliates owned 50 percent or more by listed entities from 29 September 2025 ²⁶, then BIS suspended it to 9 November 2026 ²⁷.
- **The EU** added certain Dutch controls to the EU Control List in November 2025, and ASML says this changed nothing for its immersion tools because they already needed a Dutch license ¹³.

China fell from 41 percent of ASML's net system sales in 2024 to 33 percent in 2025 ⁷.

21 Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements | Strategic Technologies Blog. Center for Strategic and International Studies [A] csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chines...

22 The Netherlands expands export control measure for advanced semiconductor manufacturing equipment. Government of the Netherlands · 6 September 2024 [A] government.nl/latest/news/2024/09/06/the-netherlands-expands-export-control-measure-advanc...

23 Export Controls on Semiconductor Manufacturing Items. Federal Register (Commerce Department; Industry and Security Bureau) · 25 October 2023 [A] federalregister.gov/documents/2023/10/25/2023-23049/export-controls-on-semiconductor-manuf...

24 Statement regarding partial revocation export license. ASML · 1 January 2024 [A] asml.com/en/news/press-releases/2023/statement-regarding-partial-revocation-export-license

25 Klever: export controls on advanced semiconductor manufacturing equipment to be tightened. Government of the Netherlands · 15 January 2025 [A] government.nl/latest/news/2025/01/15/klever-export-controls-on-advanced-semiconductor-manu...

26 Expansion of End-User Controls To Cover Affiliates of Certain Listed Entities. Federal Register (Commerce Department; Industry and Security Bureau) · 30 September 2025 [A] federalregister.gov/documents/2025/09/30/2025-19001/expansion-of-end-user-controls-to-cove...

27 One Year Suspension of Expansion of End-User Controls for Affiliates of Certain Listed Entities. Federal Register (Commerce Department; Industry and Security Bureau) · 12 November 2025 [A] federalregister.gov/documents/2025/11/12/2025-19846/one-year-suspension-of-expansion-of-en...

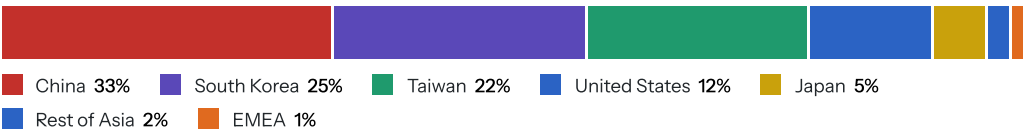
13 ASML HOLDING NV, Form 6-K report of foreign private issuer for the period ended 2025-12-31 (6-K). U.S. Securities and Exchange Commission (filing by ASML HOLDING NV) · 25 February 2026 [A] sec.gov/Archives/edgar/data/937966/000162828026011377/asml-2025xannualreportx.htm

7 Presentation Investor Relations Q4 2025. ASML · 27 January 2026 [A] ourbrand.asml.com/m/3136300aa4999bc1/original/2026_01_28_Presentation-Investor-Relations-Q...

On DUV, Reuters reported in July 2026, on one unnamed source, that Shanghai Aishengna Electronic Technology Group has started producing home-grown immersion DUV tools. The firm was registered in August 2023 with 7 billion yuan of capital and two state shareholders, Shanghai Electric Holding and a Shanghai International Trust subsidiary. It has no website, and has taken in teams from SMEE and the startup Yuliangsheng ²⁸. SMEE, the incumbent, is strongest in i-line and even there holds about four percent of the world market ²¹.

On EUV there is less evidence, and claims of Huawei mass production in 2026 remain unverified. Reuters reported in December 2025 that a Shenzhen team of former ASML engineers had built a prototype that makes extreme ultraviolet light but no chip ²⁹. Between that light and a printed chip sit the mirrors, and ASML's sole supplier of them is Zeiss ¹³.

ASML net system sales by the region tools shipped to, 2025 %



Source: ASML Q4 2025 investor presentation

The chokepoint

If ASML stopped shipping, no fab anywhere could add EUV scanners. Tools already in fabs would keep printing for as long as they were serviced. In its 2025 annual report ASML said about 95 percent of the systems it had sold in the previous 30 years were still in use ¹³. It guarantees service and spare parts for each platform until at least a committed date, subject to export controls ¹³. Even ASML could not rebuild itself quickly, since Zeiss makes its optics and Trumpf its drive laser.

In July 2026 ASML put its 2026 capacity at around 65 standard (low-NA) EUV scanners and said it plans to add 30 percent for 2027 ¹⁴.

For AI accelerators, EUV is the point of control. It prints the finest layers, the ones that set how densely transistors and wires pack, and TSMC expects the number of

28 China starts production of home-grown immersion DUV chipmaking tools, source says. Reuters · 28 July 2026 ^[B]
[reuters.com/world/china/china-starts-production-home-grown-immersion-duv-chipmaking-tools-...](https://www.reuters.com/world/china/china-starts-production-home-grown-immersion-duv-chipmaking-tools-...)

21 Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements | Strategic Technologies Blog. Center for Strategic and International Studies ^[A] csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chines...

29 How China built its 'Manhattan Project' to rival the West in AI chips. Reuters · 17 December 2025 ^[B] [reuters.com/world/china/how-china-built-its-manhattan-project-rival-west-ai-chips-2025-12-17](https://www.reuters.com/world/china/how-china-built-its-manhattan-project-rival-west-ai-chips-2025-12-17)

13 ASML HOLDING NV, Form 6-K report of foreign private issuer for the period ended 2025-12-31 (6-K). U.S. Securities and Exchange Commission (filing by ASML HOLDING NV) · 25 February 2026 ^[A]
sec.gov/Archives/edgar/data/937966/000162828026011377/asml-2025xannualreportx.htm

14 Press Release Financial Results Q2 2026. ASML · 14 July 2026 ^[A] ourbrand.asml.com/asset/c8dbf3fc-4c5e-4406-83f6-27694b138245/Press-Release-Financial-Resul...

layers needing High-NA to rise as AI designs grow more complex ¹². Every added layer is more time on a tool nobody else builds.

Key evaluation criteria

- **Resolution.** Set by the Rayleigh criterion, which puts the smallest printable feature at k_1 times the wavelength divided by the numerical aperture ³⁰. The factor k_1 depends on the chipmaking process and has a physical limit of 0.25 ³⁰. 13 nm at 0.33 NA, 8 nm at 0.55 NA ⁹.
- **Throughput.** Wafers an hour at a stated dose. 220 on the NXE:3800E, 175 on the EXE:5200B ².
- **Overlay.** How precisely one layer lands on the one below; ASML says the EXE:5200B's improved projection optics, developed with Zeiss, maximize imaging and overlay ².
- **Field size.** The patch of wafer one exposure covers. High-NA halves it ⁹. ASML and TSMC plan 12-inch masks to remove stitching constraints ¹².
- **Source power.** Brighter light, more wafers an hour, which is why the 1,000-watt demonstration matters ².

FOUR THINGS TO REMEMBER

- Lithography prints each layer of a chip's circuit onto the wafer.
- The finest layers need extreme-ultraviolet light, which works only in a vacuum and with mirrors.
- ASML of the Netherlands is the only maker of EUV machines, and Zeiss is its sole supplier of their mirrors.
- Export controls block EUV sales to Chinese chipmakers, and a Chinese prototype reported in December 2025 had printed no chip.

¹² ASML and TSMC Announce Initiative to Pioneer Industry Transition to Large-Format Photomasks for High NA EUV. TSMC · 8 September 2026 [\[A\] pr.tsmc.com/english/news/3338](https://pr.tsmc.com/english/news/3338)

³⁰ What is the Rayleigh criterion?. ASML [\[A\] asml.com/en/technology/lithography-principles/rayleigh-criterion](https://asml.com/en/technology/lithography-principles/rayleigh-criterion)

⁹ 5 things you should know about High NA in EUV. ASML · 25 January 2024 [\[A\] asml.com/en/company/stories/2024/5-things-high-na-euv](https://asml.com/en/company/stories/2024/5-things-high-na-euv)

² ASML 2025 Annual Report. ASML · 24 February 2026 [\[A\] ourbrand.asml.com/m/8ab959d4926657b/original/asml-2025-annual-report-strategic-report-sect...](https://ourbrand.asml.com/m/8ab959d4926657b/original/asml-2025-annual-report-strategic-report-sect...)

Photomasks and Pellicles

The finest layers of leading-edge chips are printed from masks built on blank plates that only three firms in the world make. Japan's AGC and Hoya are two of them, Japan's Lasertec built the first tool that inspects finished masks in EUV light, and a membrane 13 nanometers thick catches the dust that would otherwise land on the mask.

IN PLAIN TERMS

A photomask is the stencil that lithography prints from, one for each layer of a chip. The same plate prints its layer on wafer after wafer, so one plate shapes millions of chips. The most complicated layers are printed with extreme ultraviolet light, and the rest can often be printed with deep ultraviolet light shone through a quartz plate. No glass lets extreme ultraviolet light pass through, so for those layers the plate is a mirror, built up from about forty pairs of very thin layers, and the light bounces off it. A dark pattern drawn on top of the mirror soaks up the light wherever no line should print. Any speck of dust on the plate repeats on every wafer it prints. Japan's AGC and Hoya are two of the three firms that make those mirrors. A business almost nobody has heard of can hold up every advanced chip in the world.

IN SHORT

AGC says it is one of only three companies in the world that make the blank glass plates for EUV photomasks, the stencils used to print a chip's finest layers ¹. Hoya, another Japanese maker of these blanks, says its share of the market is exceptionally high ¹⁰. In May 2026 SemiAnalysis put a full set of masks for a leading-edge chip at \$40 million, a fixed cost that only chips sold in large numbers can repay ²⁷.

¹ The Japanese glass behind next-generation chips. AGC [\[A\]](https://www.agc.com/en/hub/pr/the-japanese-glass-behind-next-generation-chips.html) [agc.com/en/hub/pr/the-japanese-glass-behind-next-generation-chips.html](https://www.agc.com/en/hub/pr/the-japanese-glass-behind-next-generation-chips.html)

¹⁰ Information Technology Business | Review of Operations | HOYA REPORT 2025. HOYA [\[A\]](https://www.hoya.com/ir/2025/en/review/it.html) [hoya.com/ir/2025/en/review/it.html](https://www.hoya.com/ir/2025/en/review/it.html)

²⁷ EDA Market Primer. SemiAnalysis · 21 May 2026 [\[B\]](https://newsletter.semianalysis.com/p/eda-market-primer) newsletter.semianalysis.com/p/eda-market-primer

CHOKEPOINT CARD		EXTREME CONCENTRATION	HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY		PRICE OR MARKET SIZE
Extreme	Hard		SemiAnalysis put a leading-edge mask set at \$40M in May 2026
	AGC says only three firms supply the blank plates for EUV masks, and Lasertec was the first to sell a tool that checks a finished mask in EUV light.		in July 2022 it put a 7 nm set above \$10M
WHO LEADS	JP AGC Ranks itself No.2 worldwide in EUV mask blanks on its own fiscal 2026 estimates and counts three suppliers in all; said in June 2026 that its EUV blank sales reached ¥40bn in 2024, fell in 2025 and were recovering in 2026 JP Hoya Says its share of mask blanks is exceptionally high, and aims to keep its leading share even if customers gradually move to multi-sourcing EUV blanks JP Lasertec Launched the world's first patterned EUV mask inspection tool that works at the scanner's own wavelength, in 2019, and the faster ACTIS A200HiT series in October 2025; JPY 230,485 million of net sales in the year to June 2026 AT IMS Nanofabrication In 2023 Intel called it the established industry leader in multi-beam mask writers, the machines that draw the pattern onto the mask; CSET puts its share of all electron-beam mask writer sales at 46.6% in 2025, a \$994M market, ahead of NuFlare (39.2%) and JEOL (14.2%) US Photronics Calls itself one of the world's leading photomask makers; \$849.3M revenue in fiscal 2025		
WHERE IT IS MADE	JP Japan Mask blanks (AGC, Hoya), DUV blanks (Shin-Etsu), inspection (Lasertec), writers (NuFlare), pellicles (Mitsui Chemicals) AT Austria IMS Nanofabrication multi-beam mask writers, Brunn am Gebirge and Vienna DE Germany Zeiss mask checking in EUV light (AIMS EUV) and mask repair (MeRiT) US United States Photronics merchant mask shops, KLA inspection TW Taiwan TSMC's in-house mask shop, and a 10% stake in IMS at the end of 2024		
WHY SUBSTITUTION IS SLOW	An EUV mask starts as a blank plate coated with forty pairs of layers. AGC says it invested more than a decade in meeting the blank's requirements, and mass production only began in 2017. Three firms have now done it and the structure of the plate is published, so a newcomer knows what to build. The harder part is inspection, where Lasertec launched the world's first tool that checks a patterned mask in the same EUV light the scanner uses, in 2019. Germany's Zeiss calls its AIMS the only system that tests how a mask will print under conditions equivalent to the scanner's.		
WHERE CHINA STANDS	SMIC runs two mask shops of its own in		

Shanghai, for g-line, i-line, DUV and ArF steppers and scanners. Photronics names Shenzhen Qingyi Photomask and Shenzhen Newway Photomask among its competitors, and since 2019 has itself run two mask plants in China, in Hefei and Xiamen; its Xiamen chip mask business is a joint venture with DNP. No Chinese firm makes an EUV mask blank, a tool that checks a mask in EUV light, or a multi-beam writer, the machine that draws the finest patterns onto a mask.	WHERE THE US STANDS Photronics calls itself one of the world's leading photomask makers, and KLA makes mask inspection tools, but no American firm makes an EUV mask blank or a tool that checks a mask in EUV light.
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Every EUV layer on an AI accelerator needs a flawless mask, built on a blank plate from one of only three suppliers worldwide, two of which are Japan's AGC and Hoya ¹. AGC says it is the only company in the world that takes an EUV blank all the way from the glass to the finished coating ².

How it works

ASML says a chip's most complicated layers are made on EUV machines, while the rest can often be printed on older deep ultraviolet machines ³. A mask starts as a blank, a polished plate with nothing on it yet. For deep ultraviolet the blank is a window of quartz carrying a light-blocking film such as molybdenum silicide, and Shin-Etsu supplies those blanks ⁴. For EUV the blank is a mirror of about 40 molybdenum and silicon layer pairs, 7 nm to a pair, laid on glass, with a dark tantalum film on top, the absorber, that will carry the pattern ⁵.

The mask shop coats the blank with resist, and a mask writer draws the design into the coating with electrons. A single-beam writer flashes one shape at a time, while NuFlare's multi-beam writer for the most advanced masks controls 260,000 beams at once ⁶. A wash removes the drawn resist, an etch removes the blocking film or absorber wherever the resist is gone, and the rest of the resist is stripped. The plate now passes light, or reflects it, in the exact shape of one layer of the chip. On standard scanners it is drawn four times larger than it will print. An inspection tool compares the plate to the design, and a repair tool fixes the stray defects it finds.

Making the plate a mirror creates its own problems:

- **Mask 3D effects.** Light strikes the mirror at a slant, and the absorber has height, so its edges throw small shadows that distort the printed shape; software has to correct for it in advance.
- **Write precision.** Every edge of the absorber has to sit within a few nanometers of where the design says.

¹ The Japanese glass behind next-generation chips. AGC [\[A\]](https://www.agc.com/en/hub/pr/the-japanese-glass-behind-next-generation-chips.html) agc.com/en/hub/pr/the-japanese-glass-behind-next-generation-chips.html

² AGC to Boost Production Capacity of EUVL Photomask Blanks. AGC · 27 April 2023 [\[A\]](https://www.agc.com/en/news/detail/1203819_2814.html) agc.com/en/news/detail/1203819_2814.html

³ See ASML's DUV lithography systems. ASML [\[A\]](https://www.asml.com/en/products/duv-lithography-systems) asml.com/en/products/duv-lithography-systems

⁴ Photomask blanks - Shin-Etsu Chemical Co., Ltd.. Shin-Etsu Chemical · 3 April 2019 [\[A\]](https://www.shinetsu.co.jp/en/products/electronics-materials/photomask-blanks) shinetsu.co.jp/en/products/electronics-materials/photomask-blanks

⁵ The refined EUV mask model I.A. MAKHOTKIN¹*, M. WU¹, V. SOLTWISCH², F. SCHOLZE², V. PHILIPSEN¹. arXiv · 19 December 2019 [\[A\]](https://arxiv.org/pdf/1912.09075) arxiv.org/pdf/1912.09075

⁶ EB Mask Writer | Product Information. NuFlare Technology [\[A\]](https://www.nuflare.co.jp/english/products/beam) nuflare.co.jp/english/products/beam

- **Particles.** Anything on the reflector prints on every wafer until someone finds it.

High-NA scanners, the newest EUV machines, print finer lines with larger mirrors. To keep masks at their usual size, their mirrors shrink the pattern four times in one direction and eight times in the other, so each exposure covers half the patch of wafer and a wafer takes twice as many exposures ⁷. On 8 September 2026 ASML and TSMC announced an initiative to move from today's 6-inch masks to 12-inch masks, which they expect to raise fab productivity, lower chipmaking costs and remove stitching constraints ⁸. They aim to set up a 12-inch mask pilot line by 2031, so that High-NA scanners using 12-inch masks can enter advanced chip production by 2033 ⁸.

Variants and trade-offs

Blanks

AGC says it invested more than a decade in meeting the blank's requirements, which include near-zero thermal expansion, perfectly smooth and flat surfaces and no particle contamination, and mass production only began in 2017 ¹. AGC publishes no share figure for EUV blanks, but it counts the suppliers. It says it is one of three companies worldwide that supply EUV blanks, and the only one that handles every material and process itself ¹. Its own data book ranks AGC No.2 worldwide in EUV lithography photomask blanks, based on AGC's fiscal 2026 estimates ⁹.

Hoya says its share of the mask blank market is exceptionally high, and that customers may gradually move toward multi-sourcing EUV blanks ¹⁰. In April 2023 AGC said its EUV blank capacity would grow by about 30 percent in 2025, on a line in Fukushima selected under a METI supply-chain program, and that it was aiming for more than ¥40 billion of sales in the business by 2025 ². In December 2024 AGC said its EUV blank sales had grown 50 percent in 2023 ¹. The sales reached ¥40 billion in 2024, a year ahead of the 2025 target, AGC reported in February 2025 ¹¹. In June 2026 AGC said they had declined in 2025 and were on a

⁷ 5 things you should know about High NA in EUV. ASML · 25 January 2024 [\[A\] asml.com/en/company/stories/2024/5-things-high-na-euv](https://www.asml.com/en/company/stories/2024/5-things-high-na-euv)

⁸ ASML and TSMC Announce Initiative to Pioneer Industry Transition to Large-Format Photomasks for High NA EUV. TSMC · 8 September 2026 [\[A\] pr.tsmc.com/english/news/3338](https://pr.tsmc.com/english/news/3338)

¹ The Japanese glass behind next-generation chips. AGC [\[A\] agc.com/en/hub/pr/the-japanese-glass-behind-next-generation-chips.html](https://www.agc.com/en/hub/pr/the-japanese-glass-behind-next-generation-chips.html)

⁹ AGC Data Book. AGC Inc. · 29 May 2026 [\[A\] agc.com/en/ir/library/outline/pdf/reference.pdf](https://www.agc.com/en/ir/library/outline/pdf/reference.pdf)

¹⁰ Information Technology Business | Review of Operations | HOYA REPORT 2025. HOYA [\[A\] hoya.com/ir/2025/en/review/it.html](https://www.hoya.com/ir/2025/en/review/it.html)

² AGC to Boost Production Capacity of EUVL Photomask Blanks. AGC · 27 April 2023 [\[A\] agc.com/en/news/detail/1203819_2814.html](https://www.agc.com/en/news/detail/1203819_2814.html)

¹¹ Financial Results for FY2024. AGC Inc. · 7 February 2025 [\[A\] agc.com/en/ir/library/briefing/pdf/2025_0207e_1.pdf](https://www.agc.com/en/ir/library/briefing/pdf/2025_0207e_1.pdf)

recovery track in 2026 ¹². In August 2026 AGC planned capacity expansions of 20 to 50 percent across EUV blanks, polishing slurry and lens materials for lithography tools, with no separate figure for the blanks, and mass production on the added capacity to begin in 2028 ¹³.

Writers

An electron-beam writer cuts the pattern into a sensitive coating on the blank. Multi-beam writers fire many beams at once, and Japan's NuFlare sells them for 3 nm node design rules ⁶. In September 2023 Intel called Austria's IMS Nanofabrication the established industry leader in the multi-beam mask writing tools that advanced EUV requires, and agreed to sell roughly 10 percent of it to TSMC at a valuation of about \$4.3 billion ¹⁴. TSMC's subsidiary TSMC Development held that 10 percent at the end of 2024, at a fair value of \$432.8 million in TSMC's accounts ¹⁵. Intel sold a combined 32 percent of IMS in 2023 and still held the other 68 percent on 27 December 2025 ¹⁶. Counting all electron-beam mask writers, CSET put IMS's share of a \$994 million world market at 46.6 percent in 2025, ahead of NuFlare at 39.2 percent and JEOL at 14.2 percent ¹⁷.

Inspection and repair

A mask defect costs yield on every wafer that mask prints, so fabs check masks three times: as blanks, after patterning and again in production. Actinic inspection uses 13.5 nm light, the wavelength of EUV lithography, and Lasertec launched the world's first actinic EUV patterned mask inspection system, the ACTIS A150, in 2019 ¹⁸. In October 2025 it launched the ACTIS A200HiT series, which it says triples the A150's inspection speed ¹⁸. Lasertec reported net sales of JPY 230,485 million in the year to June 2026 ¹⁹. KLA sells optical reticle inspection tools for both EUV and optical masks ²⁰. Zeiss makes AIMS EUV, which checks a mask in EUV light under the scanner's own imaging conditions to judge how a defect will affect printing, and says it can be extended to ASML's High-NA scanner, the EXE:5000 ²¹. Zeiss also sells electron-beam repair tools that work on EUV masks ²².

12 AGC Inc.. AGC Inc. · 10 June 2026 [\[A\] agc.com/en/ir/library/bizbriefing/pdf/2026_0602semiconductor_transcript.pdf](https://agc.com/en/ir/library/bizbriefing/pdf/2026_0602semiconductor_transcript.pdf)

13 Company Overview. AGC Inc. · 25 September 2026 [\[A\] agc.com/en/ir/library/outline/pdf/c_overview.pdf](https://agc.com/en/ir/library/outline/pdf/c_overview.pdf)

6 EB Mask Writer | Product Information. NuFlare Technology [\[A\] nuflare.co.jp/english/products/beam](https://nuflare.co.jp/english/products/beam)

14 Intel to Sell Minority Stake in IMS Nanofabrication Business to TSMC. Intel · 12 September 2023 [\[A\] intc.com/news-events/press-releases/detail/1645/intel-to-sell-minority-stake-in-ims-nanofa...](https://intc.com/news-events/press-releases/detail/1645/intel-to-sell-minority-stake-in-ims-nanofa...)

15 TAIWAN SEMICONDUCTOR MANUFACTURING CO LTD, Form 6-K report of foreign private issuer for the period ended 2024-12-31 (6-K). U.S. Securities and Exchange Commission (filing by TAIWAN SEMICONDUCTOR MANUFACTURING CO LTD) · 27 February 2025 [\[A\] sec.gov/Archives/edgar/data/1046179/000104617925000019/tsmc2024q4consolidatedfina.htm](https://sec.gov/Archives/edgar/data/1046179/000104617925000019/tsmc2024q4consolidatedfina.htm)

16 INTEL CORP, Form 10-K annual report for the period ended 2025-12-27 (10-K). U.S. Securities and Exchange Commission (filing by INTEL CORP) · 23 January 2026 [\[A\] sec.gov/Archives/edgar/data/50863/000005086326000011/intc-20251227.htm](https://sec.gov/Archives/edgar/data/50863/000005086326000011/intc-20251227.htm)

17 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\] chipexplorer.eto.tech](https://chipexplorer.eto.tech)

18 Lasertec Releases ACTIS A200HiT Series Actinic EUV Patterned Mask Inspection System. Lasertec [\[A\] lasertec.co.jp/en/news/2025/20251031_3912.html](https://lasertec.co.jp/en/news/2025/20251031_3912.html)

19 Business Report | Lasertec Corporation. Lasertec [\[A\] lasertec.co.jp/en/ir/plan/message.html](https://lasertec.co.jp/en/ir/plan/message.html)

20 KLA-Tencor Introduces Five Patterning Control Systems for Sub-7nm IC Manufacturing. KLA Corporation · 11 September 2017 [\[A\] ir.kla.com/news-events/press-releases/detail/95/kla-tencor-introduces-five-patterning-cont...](https://ir.kla.com/news-events/press-releases/detail/95/kla-tencor-introduces-five-patterning-cont...)

21 Mask Qualification Solutions by ZEISS SMT. Carl Zeiss [\[A\] zeiss.com/semiconductor-manufacturing-technology/products/photomask-solutions/mask-qualifi...](https://zeiss.com/semiconductor-manufacturing-technology/products/photomask-solutions/mask-qualifi...)

22 Mask Repair Solutions by ZEISS SMT. Carl Zeiss [\[A\] zeiss.com/semiconductor-manufacturing-technology/products/photomask-solutions/mask-repair...](https://zeiss.com/semiconductor-manufacturing-technology/products/photomask-solutions/mask-repair...)

Pellicles

A pellicle is a thin membrane on a frame above the mask. Particles land on it, too far out of focus to print, and the pattern below stays clean.

ASML's EUV membrane is 13 nanometers thick, has to hold together at 500 degrees Celsius in vacuum, and every photon it absorbs is light that never reaches the wafer ²³. ASML released its first EUV pellicles in 2016 and calls the pellicle one of the breakthroughs that brought EUV lithography to high-volume manufacturing ²³. The light crosses it twice, on the way in and on the way back off the mirror, so absorption counts double.

Carbon nanotube membranes are the next step, aimed at next-generation High-NA, high-output EUV scanners ²⁴. In 2020 imec mounted them on reticles and exposed them in an NXE:3300 scanner, measuring single-pass transmission up to 97 percent and finding the effect on imaging low and correctable ²⁵. Mitsui Chemicals, which began commercial production of silicon-based EUV pellicles under an ASML license in 2021, said in 2024 it would build a plant at Iwakuni-Ohtake, tentatively due to finish in December 2025, for carbon nanotube membranes with 92 percent or higher transmittance that withstand exposure power above 1 kW ²⁴.

Cost and design economics

In July 2022 SemiAnalysis put mask sets beyond \$1 million at 28 nm and beyond \$10 million at 7 nm, and expected 3 nm mask sets to push into the \$40 million range ²⁶. Its May 2026 primer still puts a leading-edge mask set at \$40 million, and a single respin, remaking a chip after a design flaw, at leading-edge nodes at \$50 million to \$100 million ²⁷.

That cost decides who can use a node at all. SemiAnalysis wrote that falling cost per transistor at 5 nm and 3 nm is limited to firms with large wafer volume, and that more companies will lack the volume to spread the fixed cost of mask sets ²⁶. It expected failed chip designs to show up first among AI chip startups, which work on much tighter budgets ²⁶.

²³ Indistinguishable from magic: the EUV pellicle. ASML · 14 September 2022 [A] asml.com/en/news/stories/2022/the-euv-pellicle-indistinguishable-from-magic

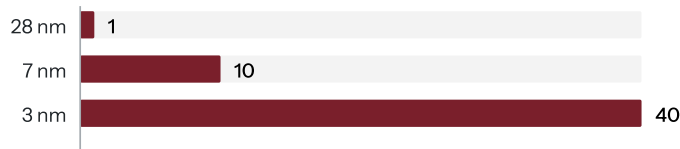
²⁴ Mitsui Chemicals Sets up Production Facilities for CNT Pellicles to Be Used in Next-Gen EUV Lithography. Mitsui Chemicals [A] jp.mitsuichemicals.com/en/release/2024/2024_0528_1/index.htm

²⁵ Imec demonstrates CNT pellicle utilization on EUV scanner. imec · 6 October 2020 [A] imec-int.com/en/press/imec-demonstrates-cnt-pellicle-utilization-euv-scanner

²⁶ The Dark Side Of The Semiconductor Design Renaissance – Fixed Costs Soaring Due To Photomask Sets, Verification, and Validation. SemiAnalysis · 24 July 2022 [B] newsletter.semianalysis.com/p/the-dark-side-of-the-semiconductor

²⁷ EDA Market Primer. SemiAnalysis · 21 May 2026 [B] newsletter.semianalysis.com/p/eda-market-primer

What one mask set costs, by node, 2022 (\$M). The 28 nm and 7 nm figures are minimums and 3 nm was a projection \$M



Source: SemiAnalysis, The Dark Side of the Semiconductor Design Renaissance, July 2022. SemiAnalysis's May 2026 EDA Market Primer puts a leading-edge mask set at \$40M

Who makes it

Mask making splits between chipmakers that make masks for their own use and independent merchant firms that sell to them and others ²⁸. Photronics says the market was majority captive-supplied for a period, and that production has more recently tended to move toward the independents ²⁸. Photronics, a leading worldwide maker of IC and flat panel display masks, had \$849.3 million of fiscal 2025 revenue, of which \$615.1 million was IC masks ²⁹. Its named competitors in chip and display masks include Dai Nippon Printing, Hoya, Tekscend Photomask and two Chinese firms, Shenzhen Newway Photomask and Shenzhen Qingyi Photomask, and it also competes with chipmakers' own mask shops ²⁸.

SMIC runs two in-house mask shops in Shanghai, for g-line, i-line, DUV and ArF steppers and scanners ³⁰. Photronics began operating two mask plants in China, in Hefei and Xiamen, in 2019, and its chip mask business in Xiamen is a joint venture in which DNP holds 49.99 percent ²⁸. There is no Chinese EUV blank, no Chinese actinic inspection tool and no Chinese multi-beam writer.

The chokepoint

Mask blanks are a small, highly concentrated business. Three firms supply EUV blanks worldwide, AGC says, and AGC spent more than a decade meeting the blank's requirements before mass production began in 2017 ¹. AGC said in June

28 PHOTRONICS INC, Form 10-K annual report for the period ended 2025-10-31 (10-K). U.S. Securities and Exchange Commission (filing by PHOTRONICS INC) · 17 December 2025 [A](https://sec.gov/Archives/edgar/data/810136/000114036125045801/ef20057458_10k.htm)

29 Photronics Reports Full Year and Fourth Quarter Fiscal 2025 Results. GlobeNewswire (release by Photronics) · 10 December 2025 [A](https://globenewswire.com/news-release/2025/12/10/3203040/0/en/Photronics-Reports-Full-Year-and-Fo...)

30 Mask Service. SMIC [A](https://smics.com/en/site/mask)

1 The Japanese glass behind next-generation chips. AGC [A](https://agc.com/en/hub/pr/the-japanese-glass-behind-next-generation-chips.html)

2026 that its EUV blank sales reached ¥40 billion in 2024, declined in 2025 and were recovering in 2026 ¹². Lasertec launched the first tool that inspects patterned EUV masks in EUV light, in 2019 ¹⁸.

Pellicles already work in high-volume EUV manufacturing, but ASML says no material is completely transparent to EUV light, so any pellicle in the light's path costs customers productivity ²³. In 2024 Mitsui Chemicals said it would set up production of carbon nanotube membranes for next-generation High-NA, high-output EUV scanners ²⁴.

Key evaluation criteria

- **Blank defectivity.** Particles buried in the multilayer cannot be repaired, so blank yield sets mask yield.
- **Write time and placement.** Intel said in 2023 that advanced EUV requires multi-beam mask writing tools, and called IMS the established industry leader in them ¹⁴. In 2025 IMS held 46.6 percent of the market for all electron-beam mask writers, on CSET's count ¹⁷.
- **Actinic inspectability.** A 13.5 nm inspection uses the same wavelength as EUV lithography, and Lasertec launched the first one for patterned masks in 2019 ¹⁸.
- **Pellicle transmission and lifetime.** Transmission counts twice, and imec measured carbon nanotube membranes passing up to 97 percent in a single crossing in 2020 ²⁵.
- **Mask-set cost per node.** In July 2022 SemiAnalysis put a set above \$10M at 7 nm, a cost that decides which designs can use a node ²⁶. In May 2026 it put a leading-edge set at \$40M ²⁷.

FOUR THINGS TO REMEMBER

- A photomask is the stencil for one layer of a chip, and any flaw on it repeats on every wafer.

12 AGC Inc.. AGC Inc. · 10 June 2026 [\[A\]](#) agc.com/en/ir/library/bizbriefing/pdf/2026_0602semiconductor_transcript.pdf

18 Lasertec Releases ACTIS A200HiT Series Actinic EUV Patterned Mask Inspection System. Lasertec [\[A\]](#) lasertec.co.jp/en/news/2025/20251031_3912.html

23 Indistinguishable from magic: the EUV pellicle. ASML · 14 September 2022 [\[A\]](#) asml.com/en/news/stories/2022/the-euv-pellicle-indistinguishable-from-magic

24 Mitsui Chemicals Sets up Production Facilities for CNT Pellicles to Be Used in Next-Gen EUV Lithography. Mitsui Chemicals [\[A\]](#) jp.mitsuichemicals.com/en/release/2024/2024_0528_1/index.htm

14 Intel to Sell Minority Stake in IMS Nanofabrication Business to TSMC. Intel · 12 September 2023 [\[A\]](#) intc.com/news-events/press-releases/detail/1645/intel-to-sell-minority-stake-in-ims-nanofa...

17 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](#) chipexplorer.eto.tech

25 Imec demonstrates CNT pellicle utilization on EUV scanner. imec · 6 October 2020 [\[A\]](#) imec-int.com/en/press/imec-demonstrates-cnt-pellicle-utilization-euv-scanner

26 The Dark Side Of The Semiconductor Design Renaissance – Fixed Costs Soaring Due To Photomask Sets, Verification, and Validation. SemiAnalysis · 24 July 2022 [\[B\]](#) newsletter.semianalysis.com/p/the-dark-side-of-the-semiconductor

27 EDA Market Primer. SemiAnalysis · 21 May 2026 [\[B\]](#) newsletter.semianalysis.com/p/eda-market-primer

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- Three firms make EUV mask blanks, and Lasertec launched the first tool that checks finished masks in EUV light.
 - AGC spent more than a decade learning to make EUV blanks before mass production began in 2017.
 - China makes masks only for older machines, in SMIC's own mask shops and at merchant firms such as Shenzhen Qingyi and Shenzhen Newway.

Deposition and Etch

Lithography prints the pattern; deposition and etch lay down and carve away the layers, and they are among the tools where Chinese makers gained the most share between 2019 and 2024.

IN PLAIN TERMS

Deposition and etch build the chip itself, one layer at a time. Deposition lays down a film a few atoms thick. Lithography prints a pattern on it. Etch then eats away everything the pattern does not protect, and the next film goes down on top. Making one chip takes 1,000 to 1,500 steps, the Semiconductor Industry Association estimated in 2025. Some of the holes the etch cuts are more than 50 times deeper than they are wide, like a finger-wide shaft about a meter deep, and the film has to coat them right to the bottom. The etch has to eat one material and leave the one beside it untouched. Four firms in America, Japan and the Netherlands make most of these machines, and Chinese makers have gained share in both kinds of tool since 2019.

IN SHORT

Deposition tools lay thin films on a wafer and etch tools carve patterns into them. American companies held 60.3 percent of the world market for deposition tools in 2025 and Japanese companies 14.0 percent ⁸. In etch and cleaning tools the American share was 52.6 percent and the Japanese 32.6 percent that year ²⁶. Chinese toolmakers have gained ground in these tools, reaching 10.1 percent of the world market for etch and cleaning tools in 2025 ²⁶. In atomic layer deposition, the most advanced deposition tool, they held only 2.6 percent in 2025, most of it from Piotech ¹³. US export rules call this tool a critical enabler of today's most advanced chips ⁷.

⁸ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\] chipexplorer.eto.tech](https://chipexplorer.eto.tech)

²⁶ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\] chipexplorer.eto.tech](https://chipexplorer.eto.tech)

¹³ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\] chipexplorer.eto.tech](https://chipexplorer.eto.tech)

⁷ Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 25 October 2023 [\[A\] govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf](https://www.govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf)

CHOKEPOINT CARD		HIGH CONCENTRATION
		MODERATELY HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY	PRICE OR MARKET SIZE
High	Moderate Most deposition and etch steps have three or four established tool makers, and atomic layer deposition has at least five; China's own makers held 2.6 percent of atomic layer deposition in 2025.	Tool makers publish no list prices World sales of chipmaking equipment were \$135.1B in 2025, with wafer processing tools up 12%.
WHO LEADS	US Applied Materials \$28.4B revenue, fiscal 2025; leader in physical and chemical vapor deposition and in epitaxy US Lam Research \$23.2B revenue, fiscal 2026; leader in dry etch and in metal atomic layer deposition JP Tokyo Electron 23% of dry etch and 38% of tube and low-pressure CVD, 2025 NL ASM International €3.2B revenue, 2025; leader in atomic layer deposition CN Naura 14.7% of PVD and 5.9% of dry etch, 2025; China's largest toolmaker	
WHERE IT IS MADE	US United States Applied Materials (Santa Clara), Lam Research (Fremont) JP Japan Tokyo Electron, Kokusai Electric, Hitachi High-Tech NL Netherlands ASM International, Almere; ALD and epitaxy KR South Korea Large buyer; Jusung, Wonik IPS and Eugene in atomic layer deposition and PSK in dry strip, 2025; Semes in wet processing CN China Naura, AMEC, Piotech; largest equipment market at \$49.3B in 2025	
WHY SUBSTITUTION IS POSSIBLE	For most of the deposition and etch steps inside a fab, the tool can already be bought from three or four makers: Applied Materials, Lam, Tokyo Electron and ASM International. Switching from one maker to another means testing the new tool on the fab's own line until it matches. Atomic layer deposition, the most advanced kind of deposition, lays down a film a fraction of a layer of atoms at a time, and at least five makers sell it, led by ASM International with 54.5 percent in 2025. China's own toolmakers held 2.6 percent of it in 2025, against 12.4 percent of dry etch.	
WHERE CHINA STANDS		
Deposition and etch are among the tools where Chinese makers gained the most share between 2019 and 2024. Chinese suppliers held 12.4 percent of dry etch, 9.8 percent of deposition and 2.6 percent of atomic layer deposition in 2025, on CSET's analysis of TechInsights data. CSET's earlier analysis had them under 1		

percent of atomic layer deposition in 2024.	WHERE THE US STANDS Two of the three largest deposition and etch tool makers are American. The US government lists some dry etch, atomic layer deposition and deep-hole deposition tools as controlled exports. Its December 2024 foreign direct product rule reaches some tools built abroad with American technology, but largely exempts those exported by companies in Japan, the Netherlands and 31 other countries that the rule lists.
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Applied Materials and Lam Research, the two largest deposition and etch suppliers, booked \$28.4 billion and \$23.2 billion of revenue in their latest fiscal years ^{1 2}.

How it works

Most etch steps, and many deposition steps, happen in a vacuum chamber that holds one wafer at a time. A pump empties the chamber of air, a measured flow of gas comes in, and an electric field that reverses millions of times a second, a radio-frequency field, turns the gas into a plasma. The field splits the gas into charged ions and into neutral fragments called radicals, which are more reactive than whole molecules ⁵. Batch furnaces such as Tokyo Electron's TELINDY PLUS instead heat as many as 125 wafers at once, usually without plasma, for oxidation, low-pressure chemical vapor deposition and some atomic layer deposition ⁶.

For deposition the gas carries the material wanted. The molecules, or the radicals a plasma splits from them, land on the wafer and stick, and the film builds from the bottom up, a few atoms at a time. To coat the floor of a deep hole as thickly as its rim, the machine can work in cycles: let one gas settle in a single layer on every surface, pump it out, admit a second gas that reacts with that layer and nothing else, pump again. Each cycle adds a fraction of a layer of atoms wherever the gas reached, so the film builds up as evenly on the walls and floor of a hole as on its rim ⁷.

For etch the gas attacks one material and leaves the one beside it. Wherever the photoresist pattern covers the wafer, nothing happens. Wherever it does not, the radicals react with the surface and turn it into a gas, which the pump carries away. A second field pulls the ions straight down at the wafer, so the etch cuts

1 Revenue from Contract with Customer, Excluding Assessed Tax (us-gaap:RevenueFromContractWithCustomerExcludingAssessedTax) reported by APPLIED MATERIALS INC /DE, XBRL company concept data. U.S. Securities and Exchange Commission (XBRL data for APPLIED MATERIALS INC /DE) [A](https://data.sec.gov/api/xbrl/companyconcept/CIK0000006951/us-gaap/RevenueFromContractWithCustomer...)

2 LAM RESEARCH CORP, Form 8-K current report for the period ended 2026-07-29 (8-K). U.S. Securities and Exchange Commission (filing by LAM RESEARCH CORP) · 29 July 2026 [A](https://sec.gov/Archives/edgar/data/707549/000070754926000033/lrcx_exhibitx991xq4x2026.htm)

5 Etch Essentials: The Building Blocks of AI Era Microchips (Semi 101). Lam Research [A](https://newsroom.lamresearch.com/etch-essentials-semiconductor-manufacturing)

6 Deposition TELINDY™ Series | Products and Service(products). Tokyo Electron [A](https://tel.com/product/telindy.html)

7 Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 25 October 2023 [A](https://govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf)

vertically and a narrow hole keeps its width as it deepens ⁵. When the etch reaches the material underneath, which the gas was chosen not to touch, it slows almost to a stop, and the tool ends the step.

Deposition and etch chambers are separate products built from similar vacuum, gas and radio-frequency parts, and the export controls describe each tool by the process it is designed to run ⁷.

A part-finished chip can cross international borders 70 or more times on its way to the end customer, a 2020 estimate by Accenture and the Global Semiconductor Alliance that the Semiconductor Industry Association repeated in 2025 ³.

Variants and trade-offs

Deposition families

The market sizes and leading shares below are CSET's for 2025, which it builds from TechInsights data, on a \$26.2 billion deposition tool market ⁸ and a \$21.9 billion dry etch market ⁹.

- **Physical vapor deposition** knocks atoms off a solid target and lands them on the wafer, \$4.9 billion in 2025 ¹⁰.
- **Chemical vapor deposition** reacts gases at the wafer surface to grow a film; the plasma-enhanced version runs cooler and is most of the \$11.2 billion CVD market, \$7.5 billion in 2025 ^{11 12}.
- **Atomic layer deposition** lays down less than one atomic layer at a time, so it coats vertical walls as evenly as horizontal floors. US regulators call it a 3D scaling enabler in 3D DRAM, 3D NAND, and FinFET and gate-all-around logic ⁷; ASM International leads it with 54.5 percent of a \$4.1 billion market in 2025 ¹³.
- **Epitaxy** grows layers that line up with the crystal beneath them, using high-temperature CVD tools ¹⁴. **Electroplating** deposits the copper used for wiring across the wafer ¹⁵.

Etch families

- **Conductor etch** cuts gates, metals and silicon, \$12.2 billion in 2025, led by Lam at 51.2 percent ¹⁶.

5 Etch Essentials: The Building Blocks of AI Era Microchips (Semi 101). Lam Research [\[A\]](https://newsroom.lamresearch.com/etch-essentials-semiconductor-manufacturing) newsroom.lamresearch.com/etch-essentials-semiconductor-manufacturing

7 Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 25 October 2023 [\[A\]](https://govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf) govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf

3 Testimony of David Isaacs, Vice President of Government Affairs. Senate · 12 May 2025 [\[A\]](https://finance.senate.gov/download/051425-isaacs-testimony&download=1) finance.senate.gov/download/051425-isaacs-testimony&download=1

8 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](https://chipexplorer.eto.tech) chipexplorer.eto.tech

9 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](https://chipexplorer.eto.tech) chipexplorer.eto.tech

10 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](https://chipexplorer.eto.tech) chipexplorer.eto.tech

11 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](https://chipexplorer.eto.tech) chipexplorer.eto.tech

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13 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](https://chipexplorer.eto.tech) chipexplorer.eto.tech

14 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](https://chipexplorer.eto.tech) chipexplorer.eto.tech

15 The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology (CSET) · 21 January 2021 [\[A\]](https://cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf) cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf

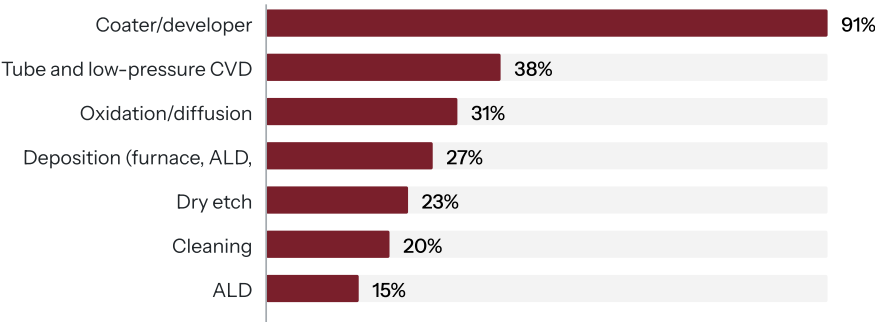
16 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](https://chipexplorer.eto.tech) chipexplorer.eto.tech

- **Dielectric etch** cuts the insulating oxides and nitrides between them, \$8.7 billion in 2025, led by Tokyo Electron at 55.9 percent ¹⁷.
- **High-aspect-ratio etch** cuts the deep, narrow channels that let 3D NAND stack layers of memory cells, and Lam says slight deviations from the target profile can hurt yield ⁴. Lam runs the etch well below 0 degrees Celsius and says Cryo 3.0 holds critical-dimension deviation under 0.1 percent down channels up to 10 microns deep ⁴.

AI hardware asks for sideways cuts, deeper holes and a second metal stack on the wafer's back.

- **Gate-all-around** needs highly selective isotropic etch, which cuts sideways, and BIS controls isotropic dry etch tools with a silicon-germanium-to-silicon selectivity of 100:1 or more ⁷.
- **HBM** needs holes etched straight through the silicon so chips can be stacked and wired, which BIS controls at 10:1 or deeper above 7 microns a minute ¹⁸.
- **Backside power delivery** moves power routing to the back of the wafer ¹⁹. Applied Materials expects it to add another \$1 billion per 100,000 wafer starts a month to the wiring market it serves ²⁰.

Tokyo Electron world market share by tool type, 2025 %



Source: Tokyo Electron FY2026 Q4 results presentation

Who makes it

SEMI put global equipment billings at \$135.1 billion in 2025, up 15 percent from \$117.1 billion, with wafer processing equipment up 12 percent ²².

17 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) ^[A] chipexplorer.eto.tech

4 Lam Research Introduces Lam Cryo™ 3.0 Cryogenic Etch Technology to Accelerate Scaling of 3D NAND for the AI Era. Lam Research · 31 July 2024 ^[A] newsroom.lamresearch.com/2024-07-31-Lam-Research-Introduces-Lam-Cryo-TM-3-0-Cryogenic-Etch...

7 Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 25 October 2023 ^[A] govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf

18 Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 5 December 2024 ^[A] govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf

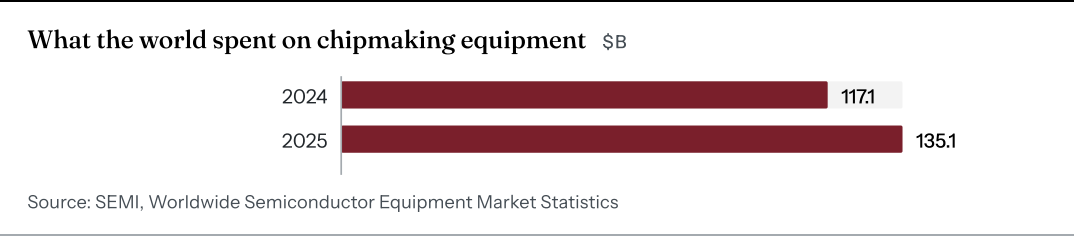
19 PowerVia Test Shows Industry-Leading Performance. Intel · 31 January 2025 ^[A] download.intel.com/newsroom/archive/2025/en-us-2023-06-05-powervia-test-shows-industrylead...

20 Applied Materials Unveils Chip Wiring Innovations for More Energy-Efficient Computing. GlobeNewswire (release by Applied Materials) · 8 July 2024 ^[A] globenewswire.com/news-release/2024/07/08/2909540/0/en/applied-materials-unveils-chip-wiri...

22 SEMI Reports Global Semiconductor Equipment Billings Reached \$135 Billion in 2025, Up 15% Year-on-Year. SEMI · 7 April 2026 ^[A] semi.org/en/SEMI-Reports-Global-Semiconductor-Equipment-Billings-Reached-135-Billion-in-2025

Within deposition and etch no one firm dominates as ASML does in lithography. The share chart in Tokyo Electron's own results presentation puts it at 23 percent of dry etch, 27 percent of deposition systems (furnace, ALD and low-pressure CVD tools) and 15 percent of ALD in 2025, against 91 percent of coater/developer ²¹.

ASM International, the atomic layer deposition specialist, reached a record EUR 3.2 billion of revenue in 2025 as customers built 2 nm gate-all-around capacity, with molybdenum ALD entering volume production ²³.



China and the controls

China is the tool vendors' largest market, and Chinese toolmakers have gained share since 2019 ²⁴. It bought \$49.3 billion of equipment in 2025, still the biggest single market, though its spending fell half a percent while Taiwan's rose 90 percent to \$31.5 billion ²². China still takes a large share of every major vendor's sales.

- **Tokyo Electron:** 34.1 percent of sales in the year to March 2026, down from 41.7 percent ²¹.
- **Lam Research:** 26 percent in the June 2026 quarter, behind Taiwan at 27 percent ².
- **Applied Materials:** 28 percent in the third fiscal quarter of 2026, down from 35 percent ²⁵.
- **ASM International:** more than 30 percent of 2025 revenue ²³.

21 Investor Relations / April 30, 2026. Tokyo Electron · 30 April 2026 [A](https://tel.com/ir/library/report/pjuomj00000000tf-att/fy26q4transcript-e.pdf) tel.com/ir/library/report/pjuomj00000000tf-att/fy26q4transcript-e.pdf

23 Press Release Q4, 2025 text. ASM International · 3 March 2026 [A](https://asm.com/media/yvxbavwe/20260303-asm-reports-q4-and-full-year-2025-results.pdf) asm.com/media/yvxbavwe/20260303-asm-reports-q4-and-full-year-2025-results.pdf

24 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology (CSET) · 14 July 2025 [A](https://cset.georgetown.edu/article/inside-beijings-chipmaking-offensive) cset.georgetown.edu/article/inside-beijings-chipmaking-offensive

22 SEMI Reports Global Semiconductor Equipment Billings Reached \$135 Billion in 2025, Up 15% Year-on-Year. SEMI · 7 April 2026 [A](https://semi.org/en/SEMI-Reports-Global-Semiconductor-Equipment-Billings-Reached-135-Billion-in-2025) semi.org/en/SEMI-Reports-Global-Semiconductor-Equipment-Billings-Reached-135-Billion-in-2025

2 LAM RESEARCH CORP, Form 8-K current report for the period ended 2026-07-29 (8-K). U.S. Securities and Exchange Commission (filing by LAM RESEARCH CORP) · 29 July 2026 [A](https://sec.gov/Archives/edgar/data/707549/000070754926000033/lrcx_exhibitx991xq4x2026.htm) sec.gov/Archives/edgar/data/707549/000070754926000033/lrcx_exhibitx991xq4x2026.htm

25 Applied Materials Announces Third Quarter 2026 Results. GlobeNewswire (release by Applied Materials) · 13 August 2026 [A](https://globenewswire.com/news-release/2026/08/13/3344890/0/en/applied-materials-announces-third-q...) globenewswire.com/news-release/2026/08/13/3344890/0/en/applied-materials-announces-third-q...

Between 2019 and 2024 China-based suppliers went from 2 to 7 percent of deposition and from under 3 to almost 9 percent of etch and clean, and in ALD they gained no share and held less than 1 percent in 2024 ²⁴. CSET's newer analysis of TechInsights data published in July 2026 puts them at 9.8 percent of deposition in 2025 ⁸. They held 10.1 percent of etch and clean that year ²⁶. In dry etch alone their share was 12.4 percent ⁹. In ALD they held 2.6 percent in 2025, most of it from Piotech ¹³. AMEC by itself held 12.4 percent of dielectric etch in 2025 ¹⁷. AMEC turned over RMB 12.385 billion in 2025, up 36.6 percent, and spent RMB 3.744 billion on research, 30.2 percent of sales ²⁷.

Washington tightened these rules at least five times between 2022 and 2025.

- **October 2022.** The 7 October interim final rule put certain chipmaking equipment and some US person support under license and widened foreign-produced item rules for 28 listed Chinese entities ²⁸.
- **October 2023.** The rule effective 17 November rewrote the equipment entries, adding isotropic and anisotropic dry etch (ECCN 3B001.c.1), spatial ALD (3B001.d.9), low-fluorine tungsten ALD and CVD (3B001.d.10) and carbon hard mask PECVD (3B001.d.5) ⁷.
- **December 2024.** BIS controlled 24 more types of equipment and three types of software, added 140 entities and wrote a foreign direct product rule that reaches some tools built outside the United States ²⁹. The new entries take in TSV etch and deposition into features with aspect ratios above 200:1 ¹⁸. The rule largely exempts foreign-made tools exported by firms located in Japan, the Netherlands and the 31 other countries it lists, whose governments can control these tools themselves ¹⁸. Japan added advanced chipmaking equipment to its control list on 23 July 2023 ¹⁸.

24 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology (CSET) · 14 July 2025 [\[A\]](https://cset.georgetown.edu/article/inside-beijings-chipmaking-offensive)
cset.georgetown.edu/article/inside-beijings-chipmaking-offensive

8 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](https://chipexplorer.eto.tech) chipexplorer.eto.tech

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17 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](https://chipexplorer.eto.tech) chipexplorer.eto.tech

27 AMEC holds its 2025 annual results briefing (中微公司成功举办2025年度业绩说明会). Advanced Micro-Fabrication Equipment (AMEC) · 1 April 2026 [\[A\]](https://amec-inc.com/news/708.html) amec-inc.com/news/708.html

28 Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification. U.S. Government Publishing Office (Federal Register) · 13 October 2022 [\[A\]](https://govinfo.gov/content/pkg/FR-2022-10-13/pdf/2022-21658.pdf) govinfo.gov/content/pkg/FR-2022-10-13/pdf/2022-21658.pdf

7 Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 25 October 2023 [\[A\]](https://govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf) govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf

29 Commerce Strengthens Export Controls to Restrict China's Capability to Produce Advanced Semiconductors for Military Applications. U.S. Bureau of Industry and Security · 2 December 2024 [\[A\]](https://bis.gov/press-release/commerce-strengthens-export-controls-restrict-chinas-capability-prod...) bis.gov/press-release/commerce-strengthens-export-controls-restrict-chinas-capability-prod...

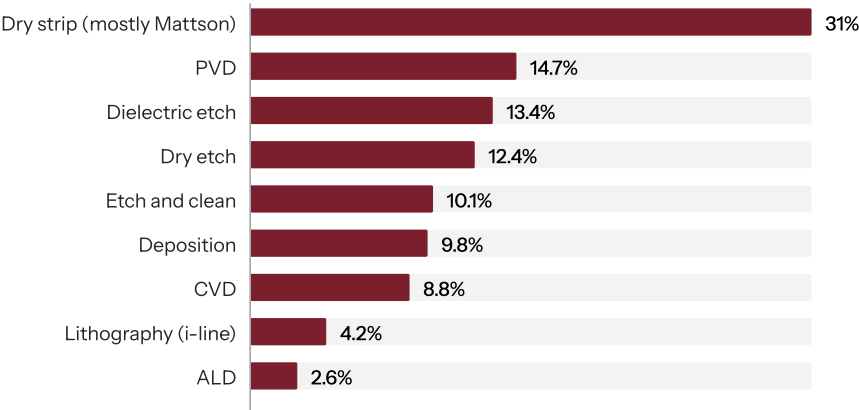
18 Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 5 December 2024 [\[A\]](https://govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf) govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf

- **September 2025.** BIS removed the Chinese units of Samsung and SK hynix, and Intel Semiconductor (Dalian), from the Validated End-User program, effective 31 December 2025, so US tools bound for them now need a license ³⁰. BIS estimated that the change would add 1,000 license applications a year ³⁰.
- **September 2025.** The Affiliates Rule extended Entity List restrictions to any company at least 50 percent owned by a listed entity ³¹; BIS then stayed it to 9 November 2026 ³².

Applied Materials took a \$253 million charge to settle an export controls compliance matter with BIS, so the rules reach the vendors as well as their customers ²⁵.

Of the tools in the chart below, China's share is largest in dry stripping, a \$314.6 million market in 2025, where Mattson Technology held 22.6 percent and Naura 8.3 percent ³³. Mattson is a US-based firm that Beijing E-Town bought in 2016 ²⁴.

China-based suppliers' share of global tool segments, 2025 %



Source: CSET analysis of TechInsights data (published July 2026), ETO Chip Explorer

The chokepoint

The chokepoint is real but weaker than lithography's. Three or four credible vendors exist for most deposition and etch steps, and atomic layer deposition has at least five, led by ASM International at 54.5 percent in 2025 ¹³. China's own toolmakers held only 2.6 percent of atomic layer deposition in 2025 ¹³. The

30 Federal Register, Volume 90 Issue 167 (Tuesday, September 2, 2025). U.S. Government Publishing Office [\[A\]](#)
govinfo.gov/content/pkg/FR-2025-09-02/html/2025-16735.htm

31 Expansion of End-User Controls To Cover Affiliates of Certain Listed Entities. U.S. Government Publishing Office (Federal Register) · 30 September 2025 [\[A\]](#) govinfo.gov/content/pkg/FR-2025-09-30/pdf/2025-19001.pdf

32 One Year Suspension of Expansion of End-User Controls for Affiliates of Certain Listed Entities. U.S. Government Publishing Office (Federal Register) · 12 November 2025 [\[A\]](#) govinfo.gov/content/pkg/FR-2025-11-12/pdf/2025-19846.pdf

25 Applied Materials Announces Third Quarter 2026 Results. GlobeNewswire (release by Applied Materials) · 13 August 2026 [\[A\]](#) globenewswire.com/news-release/2026/08/13/3344890/0/en/applied-materials-announces-third-q...

33 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](#) chipexplorer.eto.tech

24 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology (CSET) · 14 July 2025 [\[A\]](#)
cset.georgetown.edu/article/inside-beijings-chipmaking-offensive

13 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](#) chipexplorer.eto.tech

December 2024 rule targets advanced atomic layer deposition tools and the extremely deep, narrow holes that HBM and 3D memory need ¹⁸.

Key evaluation criteria

- **Selectivity.** How hard the process attacks one material and spares another. BIS controls wet processing at a silicon-germanium-to-silicon ratio of 100:1 ⁷.
- **Conformality and aspect ratio.** Whether a film reaches the bottom of a hole, and how deep that hole is against its width. Controls start at 10:1 for TSV etch and 200:1 for 3D DRAM deposition ¹⁸.
- **Uniformity.** Variation across a 300 mm wafer, with the TSV etch control set at within-wafer etch depth nonuniformity of 2 percent or less ¹⁸.
- **Throughput.** Wafers per hour, which sets cost per layer and decides how many lots a fab can run.
- **Particles and chamber matching.** How large a share of the defects a fab can tolerate comes from these tools, and whether one chamber behaves like the next, which metrology and inspection measure (see Metrology and inspection).

FOUR THINGS TO REMEMBER

- Deposition lays down thin films and etch cuts them into patterns, and making one chip takes 1,000 to 1,500 steps, by a 2025 industry estimate.
- Four American, Japanese and Dutch firms make most of these tools, and none dominates.
- Chinese makers held 12.4 percent of dry etch and 9.8 percent of deposition in 2025, on CSET's count.
- Chinese makers held 2.6 percent of atomic layer deposition in 2025, most of it from Piotech.

¹⁸ Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 5 December 2024 [A govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf](https://www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf)

⁷ Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 25 October 2023 [A govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf](https://www.govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf)

Metrology and Inspection

No fab is planned around measuring and inspecting wafers, and no fab works without it. One American firm, KLA, held 56.8 percent of the market for those tools in 2025 by CSET's count, about five times its nearest rival, and its share is still growing.

IN PLAIN TERMS

Metrology and inspection are the factory's quality control. Between the steps that build a chip, another machine looks the wafer over. It checks whether the lines are the right width, whether this layer landed squarely on the last one, and whether a speck of dirt has killed a circuit. An AI accelerator is the part built to run AI, and its main chip, the one that does the calculating, is one of the largest cut from a wafer. A bigger chip is a bigger target for a speck. On a chip that size, halving the stray specks lifts the share of flawless chips from about half to about seven in ten. One American firm held about five times the market share of its nearest rival in 2025, so a chip factory, or fab, cut off from it would find fewer of the faults that make its chips fail.

IN SHORT

Chipmakers use inspection and measurement tools to find defects and raise the share of chips that work, and KLA, the world's leading supplier, sells to every major chipmaker ². CSET's count puts KLA at 56.8 percent of this market in 2025, about five times Applied Materials, the next largest supplier ¹. Since October 2022, US rules have required a license for any US tool, inspection tools included, bound for China's most advanced fabs ²⁰. In December 2024 they also listed specific inspection and metrology tools, including those that find defects 21 nm across or smaller, a size the rule calls critical for advanced chips ²¹.

² Letter to Shareholders Q4 Fiscal 2026. KLA Corporation · 27 July 2026 [\[A\]](#)
d1io3yogOoux5.cloudfront.net/_b9ee755a5f60dd0fb3f9e27967aed6af/klatencor/db/1117/10668/let...

¹ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](#) [chipexplorer.eto.tech](#)

²⁰ Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification. U.S. Government Publishing Office (Federal Register) · 13 October 2022 [\[A\]](#) [govinfo.gov/content/pkg/FR-2022-10-13/pdf/2022-21658.pdf](#)

²¹ Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 5 December 2024 [\[A\]](#) [govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf](#)

CHOKEPOINT CARD		HIGH CONCENTRATION
		MODERATELY HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY	PRICE OR MARKET SIZE
High	Moderate KLA is the largest maker of measuring and inspecting tools, but every kind has a second maker, so losing KLA would slow a fab without stopping it.	A \$15.7B process control tool market in 2025, about \$8.9B of it KLA's (56.8%) KLA's total fiscal 2026 revenue of \$13.579B also includes services, 22 percent of revenue in the June 2026 quarter, plus PCB and component inspection and specialty semiconductor process tools. KLA puts the 2025 wafer equipment market at about \$120B.
WHO LEADS	US KLA 56.8% of process control tools in 2025 by CSET's count, about 5 times Applied Materials; Gartner put KLA at 56.5% in 2024; \$13.579B total revenue, fiscal 2026 US Applied Materials 11.2% of process control tools in 2025: electron-beam defect review, line-width measurement and electron-beam metrology JP Lasertec 6.4% of process control tools in 2025, almost all of it mask inspection JP Hitachi High-Tech 6.2% of process control tools in 2025, most of it CD-SEM line-width measurement, where it holds 71.9% NL ASML 5.9% of process control tools in 2025: YieldStar layer alignment and HMI electron-beam metrology IL Nova 4.3% of process control tools in 2025; \$880.6M revenue, 2025 US Onto Innovation 2.6% of process control tools in 2025; \$1,005.3M revenue, 2025	
WHERE IT IS MADE	US United States KLA (Milpitas), Onto Innovation (Wilmington, MA), Applied Materials NL Netherlands ASML YieldStar and HMI e-beam, Veldhoven and San Jose JP Japan Hitachi High-Tech CD-SEM; Lasertec mask inspection; Rigaku X-ray IL Israel Nova (Rehovot) and Camtek (Migdal Haemek) CN China Skyverse (Shenzhen), RSIC and other domestic makers; 0.7% of the market in 2025 by CSET's count, though Skyverse's own 2025 revenue came to about 1.8%	
WHY SUBSTITUTION IS POSSIBLE	Metrology and inspection tools measure and inspect wafers so a fab can find and fix faults in its process. KLA is the biggest maker, but eight other firms each hold more than 1 percent of the market, and Applied Materials and Hitachi each lead at least one kind of tool. A fab that loses KLA and buys from the others keeps running. It finds fewer flaws and fixes them more slowly. A country that is not allowed to buy from any of them	

has to rely on its own makers, and Chinese firms held 0.7 percent of the market for these tools in 2025 by CSET's count.

WHERE CHINA STANDS

Chinese makers are still small in metrology and inspection, but one of them is growing fast. CSET's count, built on TechInsights data, puts all Chinese firms at 0.7 percent of the market for these tools in 2025, against 0.2 percent of lithography tools. Skyverse, a Shenzhen maker of inspection and metrology tools, reported 2.05 billion yuan of revenue in 2025, about \$285 million and up 48.75 percent on 2024. That alone is about 1.8 percent of CSET's market, so the CSET count may miss some domestic sales. In its 2025 annual report Skyverse says Chinese makers still hold a low share of China's own market for these tools, where KLA holds the largest share. CSET's July 2025 survey of Chinese share gains from 2019 to 2024 covers deposition, etch, polishing, lithography, packaging and test, and does not cover measurement and inspection.

WHERE THE US STANDS

KLA is the largest maker of metrology and inspection tools in the world. CSET's Supply Chain Explorer puts it at 56.8 percent of the 2025 market, about five times Applied Materials. Citing Gartner, KLA puts its 2024 share at 56.5 percent, or 6.5 times its nearest rival. In 2025 American firms held 71.7 percent of this market and Japanese firms 14.1 percent. Since October 2022 a US license has been needed for any US tool bound for China's most advanced fabs. A December 2024 US rule added defect inspection tools that find defects 21 nm across or smaller, high-accuracy overlay and wafer shape metrology, and film and line-width metrology for non-planar transistors to the controlled list.

Process control tools were a \$15.7 billion market in 2025 ¹. KLA puts the whole wafer equipment market, including advanced packaging, at about \$120 billion that year ². CSET's count for 2025, built on TechInsights data, puts KLA at 56.8 percent, about five times Applied Materials' 11.2 percent ¹. At its March 2026 investor day KLA cited Gartner's figures for 2024, which put its share at 56.5 percent, 6.5 times its nearest competitor ³. In April 2026 KLA said its 2025 share was about 7 times the nearest competitor's ⁴. The figures rest on different data and years, so the multiple runs from about 5 to about 7.

How it works

An inspection tool sweeps a beam of light across the wafer, photographs it, and compares the image of each chip with the image of its neighbors. The chips on a wafer are meant to be identical, so anything that shows in one and not the others is a defect, and the tool records where it is. For faults too small for light to show, a

1 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](#) chipexplorer.eto.tech

2 Letter to Shareholders Q4 Fiscal 2026. KLA Corporation · 27 July 2026 [\[A\]](#)
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3 Compounding Sustainable Outperformance. KLA Corporation · 13 March 2026 [\[A\]](#)
d1io3yogOoux5.cloudfront.net/_7791115a123b86b3f10b1a5eb5210224/klatencor/db/1166/10653/fil...

4 Letter to Shareholders Q3 Fiscal 2026. KLA Corporation · 29 April 2026 [\[A\]](#)
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second tool scans a beam of electrons across a small patch and builds a picture from the electrons that bounce back.

A metrology tool measures known shapes. It shines light on a test pattern printed beside the circuits and works out from the scatter how wide the lines are and how thick the film is, and it reads marks printed in this layer and the last to measure how far the two are out of line, which is overlay.

The fab pays for all this to protect yield, the share of chips on a wafer that work. A wafer loses value two ways: whole regions ruined by mishandling, misalignment or over-etching, and single circuits killed by stray material or an airborne particle⁵.

A bigger chip is a bigger target for the second kind, and the loss grows faster than the area. In the standard formula, die yield is $(1 + D0A/a)$ to the power minus a , where $D0$ is defects per square centimeter, A is die area and a is a clustering constant of 3 to 4, which says how much defects bunch together. At a defect density of 0.8 per square centimeter, with a set to 3, a 1 square centimeter die yields 49.2 percent and a 2 by 2 centimeter die 11.3 percent, so the bigger die, which also fits fewer times on a wafer, costs 20.1 times as much⁵.

Run that equation with a clustering constant of 3 for an 8 square centimeter die, about as much as one exposure can print, and it yields about 49 percent at a defect density of 0.10 and about 69 percent at 0.05⁵. Getting from one to the other is yield learning, which means finding the process step that is losing dies and fixing it.

Those percentages are the share of dies with no killer defect. A chip built from many identical blocks can carry spares and switch off a faulty block⁵. Nvidia's full H100 design has 144 of its main computing blocks, called streaming multiprocessors, and the SXM5 version it ships has 132 turned on⁶. So the share of dies that can be sold is higher than the formula gives. What the formula shows is how fast flawless dies get scarce as chips grow.

Variants and trade-offs

The tools trade sensitivity against speed. All the market sizes and shares below are CSET's, for 2025¹.

- **Defect inspection** scans a whole wafer with light or electrons and compares each die against its neighbors. It is by far the largest family, \$6.7 billion, and the one KLA dominates, at 85.9 percent. ASML's HMI eScan 1100 runs 25 electron beams at once, up to 15 times the throughput of single-beam inspection tools, and finds patterning defects down to 7 nm⁷.

⁵ Behrooz Parhami, Dependable Computing: A Multilevel Approach, part 2. University of California, Santa Barbara · 11 October 2020 [A] web.ece.ucsb.edu/~parhami/docs_folder/f33-book-dep-comp-pt2.pdf

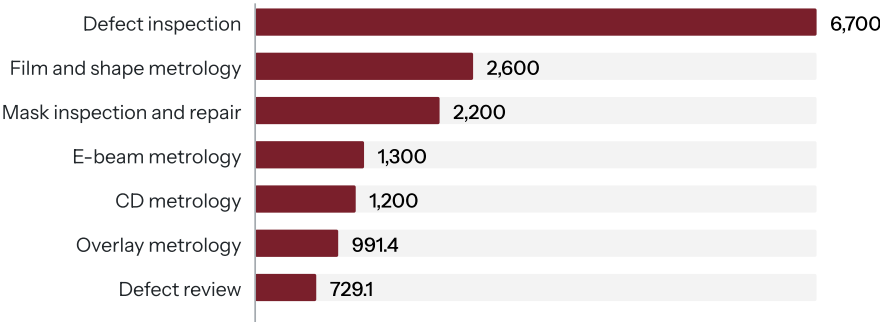
⁶ NVIDIA Hopper Architecture In-Depth. Nvidia · 22 March 2022 [A] developer.nvidia.com/blog/nvidia-hopper-architecture-in-depth

¹ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [A] chipexplorer.eto.tech

⁷ The HMI eScan 1100. ASML [A] asml.com/en/products/metrology-and-inspection-systems/hmi-escan-1100

- **Film and shape metrology** measures how thick each film is and how flat the wafer sits, without cutting it open: \$2.6 billion, with KLA at 45.6 percent, Nova at 24.6 and Onto Innovation at 10.9. Onto paid about \$720 million in August 2026 for 27 percent of Japan's X-ray maker Rigaku ⁸.
- **Mask inspection and repair** gets its own tools, because a defect on a mask repeats on every die: \$2.2 billion, and one of two families where KLA has a close rival, 45.9 percent against Lasertec's 42 and Zeiss's 10.1. Lasertec also makes actinic inspection tools, which check EUV masks with the same 13.5 nm light that prints them, and it calls its ACTIS A150 the world's first EUV patterned mask inspection system ⁹. KLA's own actinic mask inspection tool was still at an early demo stage at its March 2026 investor day ³.
- **Overlay metrology** measures whether this layer sits on the one below: \$991.4 million, split almost evenly between KLA at 51.5 percent and ASML at 47.9.
- **Critical dimension metrology** measures how wide a printed feature actually came out: \$1.2 billion, and the one family Japan leads, with Hitachi at 71.9 percent and Applied Materials at 27.5.
- **Electron-beam metrology** resolves detail too fine for light: \$1.3 billion, led by Applied Materials at 45.1 percent with ASML at 35.6 and KLA at 18.8.

Process control market by tool family, 2025 \$M



Source: ETO Supply Chain Explorer, CSET

Who makes it

KLA held 56.8 percent of a \$15.7 billion market in 2025 ¹. KLA says its share grew 3.6 percentage points from 2021 to 2025 ⁴. Its fiscal 2026 revenue was \$13.579 billion, after \$12.156 billion in fiscal 2025 ¹⁰, and it says it gained share again in 2025 across mask, optical wafer and e-beam inspection ⁴.

8 Onto Innovation Completes Strategic Investment in Rigaku Holdings Corporation. Onto Innovation · 10 August 2026 [\[A\]](#)
investors.ontoinnovation.com/news/news-details/2026/Onto-Innovation-Completes-Strategic-In...

9 ACTIS A150 | Lasertec Corporation. Lasertec · 12 September 2019 [\[A\]](#) [lasertec.co.jp/en/products/semiconductor/actis_a150.html](#)

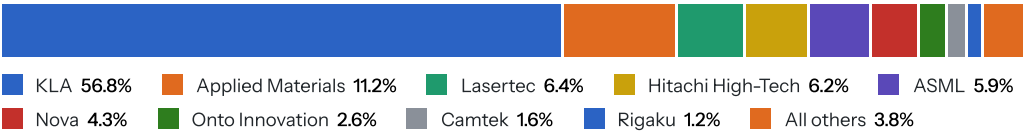
3 Compounding Sustainable Outperformance. KLA Corporation · 13 March 2026 [\[A\]](#)
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1 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](#) [chipexplorer.eto.tech](#)

4 Letter to Shareholders Q3 Fiscal 2026. KLA Corporation · 29 April 2026 [\[A\]](#)
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10 Revenue from Contract with Customer, Excluding Assessed Tax (us-gaap:RevenueFromContractWithCustomerExcludingAssessedTax) reported by KLA CORP, XBRL company concept data. U.S. Securities and Exchange Commission (XBRL data for KLA CORP) [\[A\]](#) [data.sec.gov/api/xbrl/companyconcept/CIK0000319201/us-gaap/RevenueFromContractWithCustomer...](#)

Process control tool revenue share, 2025 %



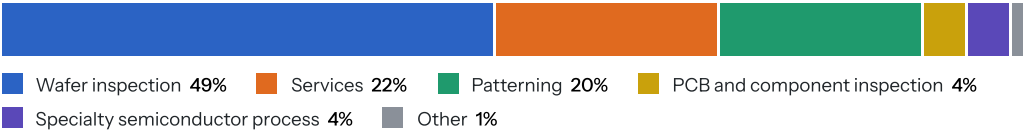
Source: ETO Supply Chain Explorer, CSET

The rest are specialists, and none holds more than 11.2 percent, by CSET's count for 2025 ¹.

- **Applied Materials** is the largest of them at 11.2 percent, selling e-beam defect review, CD-SEM line-width tools and e-beam metrology next to the deposition and etch tools that create the defects.
- **Lasertec** holds 6.4 percent, almost all of it mask inspection; **Hitachi High-Tech** 6.2 percent, most of it CD-SEM; **ASML** 5.9 percent through YieldStar overlay and HMI e-beam metrology.
- **Nova** holds 4.3 percent, through film metrology, and took \$880.6 million of revenue in 2025 ¹¹.
- **Onto Innovation** holds 2.6 percent on \$1,005.3 million of 2025 revenue ¹² and **Camtek** 1.6 percent on \$496.1 million ¹³.

Patterning, which includes metrology products and reticle inspection, grew 61 percent year on year in the June 2026 quarter, when Taiwan took 31 percent of KLA's revenue and China 26 percent ².

KLA revenue by product line, June 2026 quarter %



Source: KLA letter to shareholders, Q4 FY2026

Process control's share of fab spending is still rising, and in memory KLA credits higher performance specifications, less redundancy and more logic content in devices built for high-performance computing ⁴.

KLA's systems also apply AI-driven analytics and noise suppression, and KLA says it has added AI capabilities across its entire product portfolio over the past five years ⁴.

1 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [A](#) chipexplorer.eto.tech

11 Revenues (us-gaap:Revenues) reported by NOVA LTD., XBRL company concept data. U.S. Securities and Exchange Commission (XBRL data for NOVA LTD.) [A](#) data.sec.gov/api/xbrl/companyconcept/CIK0001109345/us-gaap/Revenues.json

12 Onto Innovation Reports 2025 Fourth Quarter and Full Year Results. Onto Innovation · 19 February 2026 [A](#) investors.ontoinnovation.com/news/news-details/2026/Onto-Innovation-Reports-2025-Fourth-Qu...

13 CAMTEK LTD, Form 6-K report of foreign private issuer for the period ended 2026-02-18 (6-K). U.S. Securities and Exchange Commission (filing by CAMTEK LTD) · 18 February 2026 [A](#) sec.gov/Archives/edgar/data/1109138/000117891326000549/zk2634405.htm

2 Letter to Shareholders Q4 Fiscal 2026. KLA Corporation · 27 July 2026 [A](#) d1io3yogOoux5.cloudfront.net/_b9ee755a5f60dd0fb3f9e27967aed6af/klatencor/db/1117/10668/let...

4 Letter to Shareholders Q3 Fiscal 2026. KLA Corporation · 29 April 2026 [A](#) d1io3yogOoux5.cloudfront.net/_a357bfc9113388e37f3bfc2ea2f0b64/klatencor/db/1117/10655/let...

Packaging, AI and China

The AI build-out is increasing the importance of advanced packaging and of the process control it needs ². KLA took the number one position in advanced wafer-level packaging process control in 2025, adding 14 points ⁴, and expects about \$1.1 billion of packaging process control revenue in 2026, more than 70 percent growth ². Onto signed a volume purchase agreement estimated at over \$240 million with an HBM maker for 2D inspection and 3D bump metrology through 2027 ¹².

Chinese makers are still small in process control, but one of them is growing fast. CSET's count, built on TechInsights data, puts all Chinese firms at 0.7 percent of a \$15.7 billion market in 2025 ¹. Skyverse (Shenzhen Zhongke Feice), which makes wafer inspection and metrology tools, reported 2.05 billion yuan of revenue in 2025, about \$285 million, up 48.75 percent on 2024 and more than double its 2023 revenue ¹⁴. That alone is about 1.8 percent of CSET's market, more than twice CSET's figure for all Chinese firms, so the CSET count may miss some domestic sales ¹. In its 2025 annual report Skyverse says Chinese makers still hold a low share of China's market for these tools and that KLA holds the largest share of it ¹⁴. By CSET's 2025 count, Chinese firms held 0.6 percent of defect inspection tools ¹⁵. They held 0.4 percent of line-width measurement in 2025 ¹⁶. In film and shape

² Letter to Shareholders Q4 Fiscal 2026. KLA Corporation · 27 July 2026 [\[A\]](#)
d1io3yog0oux5.cloudfront.net/_b9ee755a5f60dd0fb3f9e27967aed6af/klatencor/db/1117/10668/let...

⁴ Letter to Shareholders Q3 Fiscal 2026. KLA Corporation · 29 April 2026 [\[A\]](#)
d1io3yog0oux5.cloudfront.net/_a357bfc9113388e37f3bfc2ea2f0b64/klatencor/db/1117/10655/let...

¹² Onto Innovation Reports 2025 Fourth Quarter and Full Year Results. Onto Innovation · 19 February 2026 [\[A\]](#)
investors.ontoinnovation.com/news/news-details/2026/Onto-Innovation-Reports-2025-Fourth-Qu...

¹ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](#) chipexplorer.eto.tech

¹⁴ 深圳中科飞测科技股份有限公司2025 年年度报告摘要 公司代码: 688361. Cninfo · 24 April 2026 [\[A\]](#) static.cninfo.com.cn/finalpage/2026-04-25/1225182755.PDF

¹⁵ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](#) chipexplorer.eto.tech

¹⁶ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](#) chipexplorer.eto.tech

metrology they held 2 percent in 2025, all of it from Raintree Scientific Instruments, or RSIC ¹⁷. They held no share of photomask inspection and repair tools in 2025 ¹⁸. Nor did they hold any share that year of the tools that inspect wafers during advanced packaging ¹⁹.

In October 2022 the US began requiring a license for any US-made item, process control tools included, bound for a Chinese fab that made logic chips at 16/14 nm or below, NAND memory with 128 or more layers or DRAM at 18 nm half-pitch or below ²⁰. The December 2024 rule added specific process control tools to the export lists. It controls defect inspection and measurement of patterned 300 mm wafers where the tool can find defects of 21 nm or smaller using light below 400 nm, or an electron beam resolving 1.65 nm, or a cold field emission source, or two or more beams ²¹. The same rule controls overlay metrology accurate to 0.5 nm or better that is built into the track, the machine that coats and develops the light-sensitive resist, or that can switch wavelengths quickly, and stand-alone wafer shape metrology that feeds corrections to immersion or EUV scanners ²¹. A separate new entry, 3B994, covers optical film and line-width metrology for 300 mm wafers with software for measuring non-planar transistors ²¹. BIS placed these tools in new entries for items it says also have legitimate uses in older chipmaking, so they carry narrower license requirements than tools built only for advanced chips ²¹. A new foreign direct product rule extends US jurisdiction to specified foreign-made chipmaking tools bound for Macau or for a Country Group D:5 destination such as China ²².

The chokepoint

Process control is a chokepoint of concentration. Several firms can build a good film metrology tool, but one firm leads most kinds of process control tool, and its share is still growing. A fab that can buy scanners and etchers but not sensitive inspection tools finds fewer of the defects that lower its yield, so its yield rises more slowly.

17 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) chipexplorer.eto.tech

18 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) chipexplorer.eto.tech

19 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) chipexplorer.eto.tech

20 Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification. U.S. Government Publishing Office (Federal Register) · 13 October 2022 [govinfo.gov/content/pkg/FR-2022-10-13/pdf/2022-21658.pdf](https://www.govinfo.gov/content/pkg/FR-2022-10-13/pdf/2022-21658.pdf)

21 Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 5 December 2024 [govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf](https://www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf)

22 Commerce Strengthens Export Controls to Restrict China's Capability to Produce Advanced Semiconductors for Military Applications. U.S. Bureau of Industry and Security · 2 December 2024 [bis.gov/press-release/commerce-strengthens-export-controls-restrict-chinas-capability-prod...](https://www.bis.gov/press-release/commerce-strengthens-export-controls-restrict-chinas-capability-prod...)

Key evaluation criteria

- **Sensitivity.** The smallest killer defect a tool can find. ASML's multibeam system is specified to 7 nm patterning defects ⁷.
- **Throughput.** Wafers per hour, which decides how many lots a fab can afford to look at; multibeam gives up to 15 times the throughput of single-beam tools ⁷.
- **Nuisance rate.** The share of flagged events that turn out not to be real defects, which is what AI classification is meant to reduce.
- **Sampling plan.** How many wafers and sites per lot, a cost decision as much as a physics one, which sets what process control costs the fab.
- **Time to result.** How fast a measurement reaches the process engineer, which sets the speed of yield learning.

FOUR THINGS TO REMEMBER

- Metrology and inspection tools check each wafer between steps and tell a fab why its chips fail.
- AI chips are among the largest made, so finding defects matters most for them.
- CSET's count puts KLA of the United States at 56.8 percent of this tool market in 2025, about five times its nearest rival.
- Chinese makers held 0.7 percent of this tool market in 2025 on CSET's count, though Skyverse's own revenue came to about 1.8 percent.

⁷ The HMI eScan 1100. ASML  [asml.com/en/products/metrology-and-inspection-systems/hmi-escan-1100](https://www.asml.com/en/products/metrology-and-inspection-systems/hmi-escan-1100)

Transistors and the Front End

Three companies make 2 nm-class transistors in volume, and TSMC promises 1.2 times the logic density for N2P over N3E and more than that for A14 over N2.

IN PLAIN TERMS

The front end of a chip factory is the part that builds the transistors, the billions of tiny switches in every chip. Each switch is a valve. Current runs along a narrow strip of silicon called the channel, and a small voltage on a gate above the strip opens or shuts the flow. Shorter strips switch faster and more of them fit on a chip, but make the strip short enough and the valve stops sealing: current leaks through even when the gate is off, and the chip burns power doing nothing. The fix is to wrap the gate around all four sides of the strip, so it can squeeze the flow shut from every side, and that takes a long sequence of steps that have to run in exact order. Only three companies, TSMC, Intel and Samsung, make these switches in volume. In 2024 the United States put a worldwide license requirement on the know-how for building them, with an exception for countries that impose matching controls. In July 2025 Rapidus in Japan said it had started making 2 nm prototypes at its new plant in Hokkaido.

IN SHORT

TSMC's N2 process, which it calls the industry's most advanced, entered volume production in late 2025 with its first nanosheet transistors ⁴. TSMC's own figures give N2P 1.2 times the logic density of N3E, and A16, which adds backside power, up to 1.10 times the chip density of N2P ⁵. TSMC says its A14 process, planned for production in 2028, will raise logic density by more than 20 percent over N2 ²³. China made its most advanced chips, at 7 nm, with older deep ultraviolet machines stockpiled before export controls took effect, and in September 2025 CSIS judged that EUV remained firmly out of China's reach ²².

4 2nm Technology. TSMC [\[A\]](https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_2nm) [tsmc.com/english/dedicatedFoundry/technology/logic/l_2nm](https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_2nm)

5 HPC Platform – Advanced Technologies. TSMC [\[A\]](https://www.tsmc.com/english/dedicatedFoundry/technology/platform_HPC_tech_advancedTech) [tsmc.com/english/dedicatedFoundry/technology/platform_HPC_tech_advancedTech](https://www.tsmc.com/english/dedicatedFoundry/technology/platform_HPC_tech_advancedTech)

23 TSMC Unveils Next-Generation A14 Process at North America Technology Symposium. TSMC · 24 April 2025 [\[A\]](https://www.pr.tsmc.com/english/news/3228) [pr.tsmc.com/english/news/3228](https://www.pr.tsmc.com/english/news/3228)

22 Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements | Strategic Technologies Blog. Center for Strategic and International Studies [\[A\]](https://www.csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chines...) [csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chines...](https://www.csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chines...)

CHOKEPOINT CARD		EXTREME CONCENTRATION	HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY		PRICE OR MARKET SIZE
Extreme	Hard Three firms make gate-all-around transistors, the newest kind, in volume, and none sells its process recipe.		No foundry publishes prices for its newest wafers, so cost per transistor cannot be worked out from public figures TSMC publishes 1.2 times the logic density for N2P over N3E and a gain of more than 20 percent for A14 over N2.
WHO LEADS	TW TSMC N2 in volume production since 4Q25, TSMC's first nanosheet node US Intel 18A in high-volume manufacturing; 18A-P adds 9% performance at the same power KR Samsung Foundry First into production with gate-all-around nanosheets, starting initial 3 nm output in June 2022; SF2 family, with SF2Z adding backside power CN SMIC N+2 and N+3, printed in several passes on older deep-ultraviolet tools, no EUV JP Rapidus State-backed 2 nm entrant targeting mass production in 2027		
WHERE IT IS MADE	TW Taiwan TSMC N2 at Fab 20 Hsinchu and Fab 22 Kaohsiung US United States Intel 18A at Fab 52, Arizona; TSMC Arizona on N4, with N3 targeted for the second half of 2027 KR South Korea Samsung Hwaseong and Pyeongtaek JP Japan Rapidus Chitose, Hokkaido CN China SMIC Shanghai and Beijing 300 mm lines		
WHY SUBSTITUTION IS SLOW	The scarce thing is the process recipe: which steps, in which order, on which tools. Three firms have written one, so a newcomer knows it can be done but has to work out its own. Rapidus in Japan, backed by the state, is now finding out what it costs to go from prototypes to volume production, with 424.95 billion yen in equity as of June 2026, state research subsidies and a 2027 target. China cannot buy extreme-ultraviolet scanners. It made its 7 nm chips on older deep-ultraviolet machines stockpiled before export controls took effect, and that keeps it behind the newest chips.		
WHERE CHINA STANDS		WHERE THE US STANDS	
SMIC ships a process it calls N+3, measured at 113.4 million transistors per square millimeter. It prints its tightest layers in two or four passes because it cannot buy an extreme-ultraviolet scanner. Its narrowest wires sit closer together than Intel 18A's, a comparison SemiAnalysis calls an incomplete, cherry-picked metric.		Intel runs the only American-owned line that makes the newest transistors. Its 18A process brought gate-all-around transistors and backside power, where power is fed from under the transistors, to market together. Intel is also the first to use High-NA EUV scanners, the newest kind, in volume production.	

A Blackwell GPU is 208 billion switches on two dies, each the largest a lithography machine can print in one shot ¹. Every switch has to turn on fully, turn off completely, and keep doing it for years. Making the switches is the front end of line; wiring them together is the back end.

How it works

The front end builds that valve in a fixed order. First it marks where each transistor will sit and fires atoms of boron or phosphorus into the silicon there, a step called ion implantation, so that those patches conduct the way the design needs.

Next it shapes the channel, in a FinFET by etching the silicon into thin fins standing up from the wafer and laying the gate over the top and both sides of each fin, three sides instead of one. In a gate-all-around transistor the fab instead grows alternating layers of silicon and silicon-germanium, cuts the stack into a narrow bar, then dissolves the silicon-germanium away, leaving thin silicon sheets held at their ends like shelves, and fills the gaps above, below and beside each sheet with gate metal, all four sides. Before the metal goes in, a film of insulator a few atoms thick is laid over every sheet, so that the gate controls the channel without touching it. Last come the contacts, small metal plugs down to the two ends of the channel and to the gate, ready for the wiring layers above.

Each of those is a deposition, an etch or an implant of its own, and they have to run in exact order, since a sheet cannot be wrapped once the metal is on, nor the insulator added once it is buried.

Current leaks two ways, straight through the gate insulator and along the channel from end to end while the gate is off. The second is called short-channel leakage, and wrapping the gate around the channel reduces it. Three fixes deal with the two leaks:

- **Better insulator.** A thicker hafnium-based film, paired with a metal gate, lets fewer electrons slip straight through yet controls the channel as tightly as before. Intel replaced silicon dioxide with it at 45 nm in 2007 and said it cut leakage through the insulator more than tenfold and, with the metal gate, leakage along the channel more than fivefold ².
- **More gate.** Wrap gate metal around more sides of the channel, as fins and nanosheets do.
- **Thinner channel.** Thin the silicon until no current can flow where the gate cannot reach it.

Variants and trade-offs

Planar and FinFET

A planar transistor lays the gate on one side of a flat channel, and loses control as the channel shortens. A fin stands the channel on edge so the gate covers three sides, but current then comes in whole fins: a designer who needs more adds one, and nobody gets half a fin.

¹ NVIDIA Blackwell Architecture. Nvidia · 18 December 2025 [\[A\] nvidia.com/en-us/data-center/technologies/blackwell-architecture](https://www.nvidia.com/en-us/data-center/technologies/blackwell-architecture)

² Intel's Transistor Technology Breakthrough Represents Biggest Change to Computer Chips in 40 Years. Intel · 27 January 2007

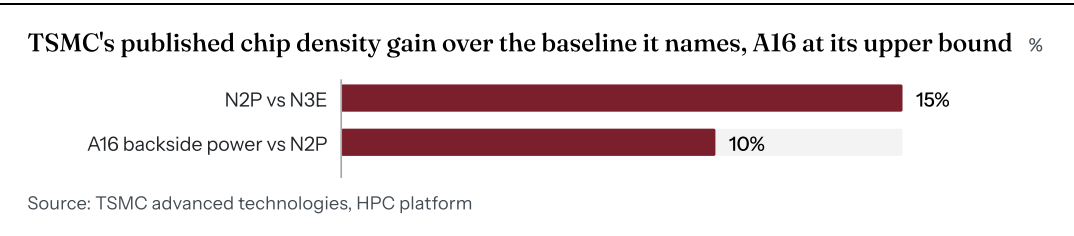
[\[A\] intel.com/pressroom/archive/releases/2007/20070128comp.htm](https://www.intel.com/pressroom/archive/releases/2007/20070128comp.htm)

Gate-all-around nanosheets

A nanosheet lays the channel back down, stacks two to four thin sheets and threads gate metal around each one. The sheets can be drawn at different widths, so current comes in fine steps again. TSMC sells this as NanoFlex, which lets designers mix short cells for small area with tall cells for performance ³.

N2 entered volume production in the fourth quarter of 2025, TSMC's first nanosheet node ⁴. TSMC rates the follow-on N2P at 18 percent more speed at the same power, 36 percent less power at the same speed, and 1.2 times the logic density of N3E ⁵. Intel's RibbonFET shipped on 18A, and 18A-P adds another 9 percent performance at the same power ⁶. Samsung began initial production of its 3 nm gate-all-around process in June 2022, more than three years before TSMC's N2 ⁷.

Those numbers are vendor claims until someone measures the silicon. Each foundry picks its own baseline, and none publishes a density figure that can be set against a rival's.



Backside power delivery

Power and signal share one stack of copper wiring above the transistors, where wide power rails crowd out the signal wires. Backside power grinds the wafer thin and builds a second network underneath it.

Intel shipped it first as PowerVia: on 18A, an 11 percent cut in routed area and a tenfold cut in dynamic voltage droop, the sag in supply voltage when a block of logic switches on at once ⁶. TSMC's Super Power Rail lands that network straight on each transistor's source and drain, with no buried rail between, which is harder to build and gives more: against N2P, A16 gives 8 to 10 percent more speed, 15 to 20 percent less power and up to 1.10 times the chip density ⁵.

TSMC said in April 2026 that A13, a direct shrink of A14 with 6 percent area savings, and A12, which adds Super Power Rail to the A14 platform, are both scheduled to enter production in 2029 ⁸.

3 News 3136 (TSMC website). TSMC pr.tsmc.com/english/news/3136

4 2nm Technology. TSMC tsmc.com/english/dedicatedFoundry/technology/logic/l_2nm

5 HPC Platform – Advanced Technologies. TSMC tsmc.com/english/dedicatedFoundry/technology/platform_HPC_tech_advancedTech

6 Intel Foundry Details Process Milestones and Future Innovation at VLSI Symposium. Intel · 16 June 2026 intc.com/news-events/press-releases/detail/1772/intel-foundry-details-process-milestones-a...

7 Samsung Begins Chip Production Using 3nm Process Technology With GAA Architecture - Samsung Global Newsroom. Samsung Global Newsroom · 30 June 2022 news.samsung.com/global/samsung-begins-chip-production-using-3nm-process-technology-with-g...

8 TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC · 23 April 2026 pr.tsmc.com/english/news/3302

TSMC's logic roadmap beyond N2, from its own announcements

- 2028-01-01
N2U, 3-4% faster or 8-10% lower power than N2P
- 2028-01-01
A14, up to 15% faster and more than 20% denser than N2
- 2029-01-01
A13, a direct shrink of A14 for 6% area savings
- 2029-01-01
A12, the A14 platform with Super Power Rail backside power

Source: TSMC, 2026 North America Technology Symposium

CFET and what comes after

A logic gate needs two transistors that switch on opposite signals, and today they sit side by side. The research institute imec sees complementary FETs, which stack the two on top of each other, as an attractive design for logic nodes beyond 1 nm ⁹.

The back end of line

Wiring is now as hard to make as the transistor. Copper seeps into the insulator around it, so every wire needs a barrier, a liner and a cap, and as the most critical wiring levels drop below a 20 nm pitch those extra layers take a large share of the wire's width ¹⁰. Two metals are moving into those narrow levels.

- **Ruthenium** shows promise for use without a barrier, which would keep the wire's resistance low ¹⁰. imec has demonstrated ruthenium lines at a 16 nm pitch ¹¹.
- **Molybdenum** conducts worse in bulk, 5.3 against copper's 1.68 microhm-cm, but in a thin film it beats tungsten by up to 30 percent and needs no barrier either, which is moving it into some contacts and local wiring layers ¹².

Who makes it

TSMC, Intel and Samsung build gate-all-around nodes with extreme ultraviolet lithography. SMIC builds 7 nm-class nodes without it ¹³. In July 2025 state-backed Rapidus said it had started making 2 nm prototypes at its

9 CFET (complementary FET). imec [\[A\]](https://imec-int.com/en/articles/imec-puts-complementary-fet-cfet-logic-technology-roadmap) imec-int.com/en/articles/imec-puts-complementary-fet-cfet-logic-technology-roadmap

10 Semi-damascene metallization. imec [\[A\]](https://imec-int.com/en/articles/semi-damascene-metallization-inflection-point-back-end-line-proce...) imec-int.com/en/articles/semi-damascene-metallization-inflection-point-back-end-line-proce...

11 16nm Ru lines using semi-damascene integration approach. imec · 3 June 2025 [\[A\]](https://imec-int.com/en/press/imec-demonstrates-16nm-pitch-ru-lines-record-low-resistance-obtained...) imec-int.com/en/press/imec-demonstrates-16nm-pitch-ru-lines-record-low-resistance-obtained...

12 Molybdenum's Role in Ultra-Fast Computing: The Metal Behind the Speed. Entegris · 18 May 2026 [\[A\]](https://blog.entegris.com/molybdenums-role-in-ultra-fast-computing-the-metal-behind-the-speed) blog.entegris.com/molybdenums-role-in-ultra-fast-computing-the-metal-behind-the-speed

13 Is SMIC N+3's Metal Pitch Smaller than Intel 18A's?. SemiAnalysis · 14 June 2026 [\[B\]](https://newsletter.semianalysis.com/p/steel-smic-n3-teardown) newsletter.semianalysis.com/p/steel-smic-n3-teardown

plant in Chitose, Hokkaido, and would begin mass production in 2027 ¹⁴. By June 2026 it had raised 424.95 billion yen in equity, the latest 150 billion yen from a state agency, and it has received government research subsidies since fiscal 2022 ¹⁵.

Node names describe nothing physical. SMIC's N+3, its third-generation 7 nm process, sets its narrowest wires 32.5 nm apart, tighter than Intel 18A's 36 nm, and reaches 113.4 million transistors per square millimeter against 107.7 for TSMC's N6 ¹³.

AI accelerators have usually trailed the leading edge, since a very large die comes out working reliably only on a process that has run for years. Blackwell uses a custom TSMC 4NP ¹. AMD's MI455X, launched on 23 July 2026, lists TSMC 2 nm and 3 nm silicon ¹⁶. It spreads its compute across eight separate dies ¹⁷.

SRAM, the fast memory on the logic die, is the scaling failure that hurts AI chips most. TSMC claims 22 percent more SRAM density from N3E to N2, but the gain comes mostly from the circuits around the array, and the cell that holds one bit shrinks little or not at all ¹⁸. See Memory and HBM.

The chokepoint

No single machine makes the front end a chokepoint. The recipe does, and a recipe is which steps run in which order on which tools. In September 2024 the United States put a worldwide license requirement on the know-how for building gate-all-around transistors, with an exception for countries that impose matching controls ¹⁹.

China shows what that recipe costs. The third National Integrated Circuit Fund launched in May 2024 with 344 billion yuan, about \$47 billion ²⁰, so money is not the constraint; tools are. A Shanghai state firm began building domestic immersion scanners in 2026 and planned about five that year and roughly 20 in 2027 ²¹. Those are deep-ultraviolet machines, a generation behind EUV, and SMIC gets fine features out of them by printing its tightest layers in several passes. That volume keeps those lines running and comes nowhere near replacing ASML. EUV

14 Rapidus Achieves Significant Milestone at its State-of-the-Art Foundry with Prototyping of Leading-Edge 2nm GAA Transistors First prototypes successfully demonstrate electrical characteristics as the company continues to hit targets leading up to 2027 mass-production - Information - Rapidus Corporation. Rapidus [\[A\]](https://rapidus.inc/en/news_topics/information/rapidus-achieves-significant-milestone-at-its-state-...) rapidus.inc/en/news_topics/information/rapidus-achieves-significant-milestone-at-its-state-...

15 Rapidus Completes 150 Billion Yen Funding Round from Japan Government - Information - Rapidus Corporation. Rapidus [\[A\]](https://rapidus.inc/en/news_topics/information/20260605-2) rapidus.inc/en/news_topics/information/20260605-2

13 Is SMIC N+3's Metal Pitch Smaller than Intel 18A's?. SemiAnalysis · 14 June 2026 [\[B\]](https://newsletter.semianalysis.com/p/steel-smic-n3-teardown) newsletter.semianalysis.com/p/steel-smic-n3-teardown

1 NVIDIA Blackwell Architecture. Nvidia · 18 December 2025 [\[A\]](https://nvidia.com/en-us/data-center/technologies/blackwell-architecture) nvidia.com/en-us/data-center/technologies/blackwell-architecture

16 AMD Instinct™ MI455X GPUs. AMD [\[A\]](https://amd.com/en/products/accelerators/instinct/mi400/mi455x.html) amd.com/en/products/accelerators/instinct/mi400/mi455x.html

17 AMD Instinct 455X GPU. AMD · 20 July 2026 [\[A\]](https://amd.com/content/dam/amd/en/documents/products/accelerators/instinct/amd-instinct-mi455x_br...) amd.com/content/dam/amd/en/documents/products/accelerators/instinct/amd-instinct-mi455x_br...

18 Clash of the Foundries: Gate All Around + Backside Power at 2nm. SemiAnalysis · 1 October 2024 [\[B\]](https://newsletter.semianalysis.com/p/clash-of-the-foundries) newsletter.semianalysis.com/p/clash-of-the-foundries

19 Commerce Control List Additions and Revisions; Implementation of Controls on Advanced Technologies Consistent With Controls Implemented by International Partners. Federal Register (Commerce Department; Industry and Security Bureau) · 6 September 2024 [\[A\]](https://federalregister.gov/documents/2024/09/06/2024-19633/commerce-control-list-additions-and-re...) federalregister.gov/documents/2024/09/06/2024-19633/commerce-control-list-additions-and-re...

20 China launches \$47bn chip fund to counter U.S. restrictions. Nikkei Asia · 27 May 2024 [\[B\]](https://asia.nikkei.com/spotlight/supply-chain/china-launches-47bn-chip-fund-to-counter-u.s.-restr...) asia.nikkei.com/spotlight/supply-chain/china-launches-47bn-chip-fund-to-counter-u.s.-restr...

21 China starts production of home-grown immersion DUV chipmaking tools, source says. Reuters · 28 July 2026 [\[B\]](https://reuters.com/world/china/china-starts-production-home-grown-immersion-duv-chipmaking-tools-...) reuters.com/world/china/china-starts-production-home-grown-immersion-duv-chipmaking-tools-...

is further away: China has announced \$43 billion for domestic development, and the Center for Strategic and International Studies judged in September 2025 that EUV remains firmly out of reach despite massive state investment ²².

See Lithography and Geopolitics.

Key evaluation criteria

- **Electrostatic control.** How far the gate wraps the channel. It sets how much the switch leaks when off, and the lowest supply voltage it can run on.
- **Density.** Transistors per square millimeter, comparable only inside one foundry's own numbering and for one kind of cell.
- **Interconnect resistance.** Below a 20 nm wire spacing, copper wiring adds more and more delay from its resistance and capacitance ¹¹.
- **Power delivery.** The voltage lost carrying power across the die. Backside power frees area and cuts the droop tenfold ⁶.
- **SRAM scaling.** The cell that holds one bit has barely shrunk since the 5 nm node, which caps how much cache an accelerator can afford ¹⁸.
- **Cost per transistor.** No foundry publishes wafer prices, so it cannot be worked out from public figures.

FOUR THINGS TO REMEMBER

- The newest transistors wrap the gate around all four sides of the channel to stop current leaking.
- Only TSMC, Intel and Samsung make them in volume.
- No firm sells its process recipe, so a newcomer has to develop its own.
- SMIC makes 7 nm-class chips without EUV by printing its tightest layers in several passes.

²² Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements | Strategic Technologies Blog. Center for Strategic and International Studies [\[A\]](https://csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chines...) csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chines...

¹¹ 16nm Ru lines using semi-damascene integration approach. imec · 3 June 2025 [\[A\]](https://imec-int.com/en/press/imec-demonstrates-16nm-pitch-ru-lines-record-low-resistance-obtained...) imec-int.com/en/press/imec-demonstrates-16nm-pitch-ru-lines-record-low-resistance-obtained...

⁶ Intel Foundry Details Process Milestones and Future Innovation at VLSI Symposium. Intel · 16 June 2026 [\[A\]](https://intc.com/news-events/press-releases/detail/1772/intel-foundry-details-process-milestones-a...) intc.com/news-events/press-releases/detail/1772/intel-foundry-details-process-milestones-a...

¹⁸ Clash of the Foundries: Gate All Around + Backside Power at 2nm. SemiAnalysis · 1 October 2024 [\[B\]](https://newsletter.semianalysis.com/p/clash-of-the-foundries) newsletter.semianalysis.com/p/clash-of-the-foundries

Foundries and Fabs

TSMC runs six plants that each print more than 100,000 wafers a month. All six are in Taiwan, and in 2025 their combined capacity passed 13 million wafers a year, out of more than 17 million for the whole company.

IN PLAIN TERMS

A foundry is a fab that makes chips for other companies. Those companies send in their designs, and the foundry runs them all through the same building on the same tools. The building costs tens of billions of dollars, and the air inside is cleaner than an operating room. Even so, a wafer crosses hundreds of machines over several months inside sealed boxes, never touching that air. No chip company sells enough of one product to fill a factory like that on its own, so the world shares a handful of them. TSMC runs the biggest, and all six of its largest plants sit in Taiwan, which is why one island's politics reaches the whole chip supply.

IN SHORT

In a May 2024 report, the Semiconductor Industry Association and Boston Consulting Group found that Taiwan, home of TSMC, held 69 percent of the world's capacity for logic chips below 10 nanometers in 2022 ²⁵. In December 2025 SemiAnalysis put Taiwan's share of the world's advanced-node capacity, which it did not define by node size, at over 90 percent ²⁷. All six of TSMC's largest plants, which it calls gigafabs, are in Taiwan ². TSMC is building more plants in Arizona, and once they are finished around 30 percent of its 2-nanometer and more advanced capacity will be there ¹⁸.

²⁵ R A J V A R A D A R A J A N / I A C O B K O C H - W E S E R / C H R I S R I C H A R D / J O S E P H F I T Z G E R A L D /. Semiconductor Industry Association · 9 May 2024 ^[A] [semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconduc...](https://www.semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconduc...)

²⁷ TSMC Overseas Fabs – A Success? SemiAnalysis · 1 December 2025 ^[B] newsletter.semianalysis.com/p/tsmc-overseas-fabs-a-success

² Fab Capacity. TSMC ^[A] tsmc.com/english/dedicatedFoundry/manufacturing/fab_capacity

¹⁸ TSMC Announces Additional \$100 Billion Investment In Arizona. City of Phoenix · 16 July 2026 ^[A] phoenix.gov/newsroom/ced-news/tsmc-announces-additional--100-billion-investment-in-arizona...

CHOKEPOINT CARD		EXTREME CONCENTRATION	HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY		PRICE OR MARKET SIZE
Extreme	Hard Intel and Samsung also run lines for the newest chips, but TSMC has not built one of its largest fabs outside Taiwan, and the slow part is training the workforce.		BCG's 2023 estimate puts the ten-year cost of owning a new 2 nm-class fab completed in 2026 at \$35-43 billion in March 2026 SIA put the cost to build and equip a leading-edge fab at as much as \$20-25 billion. TSMC's planned investment in Arizona rose to \$265 billion in July 2026
WHO LEADS	TW TSMC 77% of wafer revenue from 7 nm and below, 2Q26; six gigafabs, all in Taiwan US Intel Foundry \$5.8bn segment revenue, only \$293m of it from outside customers; \$2.089bn operating loss, 2Q26 KR Samsung Foundry Hwaseong and Pyeongtaek; an initial \$17bn minimum at Taylor, Texas, now part of over \$37bn planned in Texas (CHIPS award, Dec 2024) CN SMIC \$9.327bn revenue in 2025 at 93.5% utilization JP Rapidus State-backed 2 nm entrant, Chitose		
WHERE IT IS MADE	TW Taiwan TSMC's six gigafabs and UMC; TSMC's N2 and N3 lines KR South Korea Samsung Foundry, Hwaseong and Pyeongtaek CN China SMIC and Hua Hong; the largest installed capacity of any region, forecast by SEMI in 2026 to stay largest in 2026 and 2027, almost all of it on older nodes US United States Intel Foundry, GlobalFoundries, TSMC Arizona, Samsung Taylor JP Japan TSMC Kumamoto, Rapidus Chitose		
WHY SUBSTITUTION IS SLOW	Money can buy the building. In 2023 BCG put the ten-year cost of owning a new 2 nm-class fab finished in 2026 at \$35 to \$43 billion, and in March 2026 SIA put the cost to build and equip a leading-edge fab at as much as \$20 to \$25 billion. Intel and Samsung already run lines for the newest chips, so a newcomer is copying something that has been done. Money cannot quickly buy a workforce that has run one process for years. Even TSMC has yet to build one of its largest fabs anywhere but Taiwan.		
WHERE CHINA STANDS			
SMIC and Hua Hong are China's largest foundries. SMIC had revenue of \$9.327 billion in 2025 with its lines 93.5 percent full. It cannot buy an EUV scanner, yet it makes 7 nm-class chips on its N+2 and N+3 processes by printing the tightest layers in several passes on older deep-ultraviolet scanners. CSET reported in June 2024 that Huawei's Ascend 910B AI			

chip is believed to be made on N+2, though SemiAnalysis judged in April 2025 that most 910B and 910C chips were made at TSMC. In the third-quarter 2026 update of its World Fab Forecast, SEMI projected that China would keep the world's largest installed fab capacity in 2026 and 2027, and little of it is advanced.	WHERE THE US STANDS Intel Foundry is the only American-owned foundry that makes the newest chips. In the second quarter of 2026 it lost \$2.089 billion on \$5.8 billion of segment revenue, only \$293 million of which came from outside customers. The federal government bought a 9.9 percent stake in Intel in August 2025. The stake is passive, with no board seat or governance rights, and the government agreed to vote with Intel's board on shareholder matters, with limited exceptions.
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TSMC calls a plant a GIGAFAB once it can run more than 100,000 wafers a month, each a 300 mm disc, twelve inches across ¹. It operates six of them, and every one is in Taiwan ².

How it works

Inside, the work is one loop repeated for every layer. Wafers travel in a lot, a batch of 25 in a sealed pod called a FOUP that only a machine opens. An overhead track carries the pod from tool to tool. At each tool a robot lifts one wafer out, the tool does its one job, depositing a film, printing a pattern, etching it, cleaning it or measuring it, and the robot puts the wafer back. The pod moves on to the next tool, often across the building, and the loop starts again with the next layer. A chip takes hundreds of those visits, so a wafer spends months inside.

The pod keeps the wafer clean for all of that time, because the wafer never meets the room's air, and even that air is filtered until it carries almost no dust. Every design in the building runs on the same tools because each tool is set by recipe, the list of gases, temperatures and times for one step, and a foundry offers each customer the same list of recipes on shared machines. The tools run day and night, since an idle tool earns nothing. The finished wafer is tested (see Test and assembly), then cut and packaged.

TSMC, founded in 1987, pioneered the pure-play model, in which a foundry makes only its customers' products ³. In 2023 BCG estimated that a new fab for chips at 2 nm and below, completed in 2026, would cost \$35 to \$43 billion to own over ten years, 33 to 66 percent above 2023 costs ⁴. In March 2026 the Semiconductor Industry Association told the US Senate that building and equipping a leading-edge fab takes as much as \$20 to \$25 billion of capital ⁵.

1 GIGAFAB® Facilities. TSMC [\[A\]](https://www.tsmc.com/english/dedicatedFoundry/manufacturing/gigafab) [tsmc.com/english/dedicatedFoundry/manufacturing/gigafab](https://www.tsmc.com/english/dedicatedFoundry/manufacturing/gigafab)

2 Fab Capacity. TSMC [\[A\]](https://www.tsmc.com/english/dedicatedFoundry/manufacturing/fab_capacity) [tsmc.com/english/dedicatedFoundry/manufacturing/fab_capacity](https://www.tsmc.com/english/dedicatedFoundry/manufacturing/fab_capacity)

3 Company profile (TSMC website). TSMC [\[A\]](https://www.tsmc.com/english/aboutTSMC/company_profile) [tsmc.com/english/aboutTSMC/company_profile](https://www.tsmc.com/english/aboutTSMC/company_profile)

4 Navigating the Costly Economics of Chip Making. Boston Consulting Group · 28 September 2023 [\[A\]](https://www.bcg.com/publications/2023/navigating-the-semiconductor-manufacturing-costs) [bcg.com/publications/2023/navigating-the-semiconductor-manufacturing-costs](https://www.bcg.com/publications/2023/navigating-the-semiconductor-manufacturing-costs)

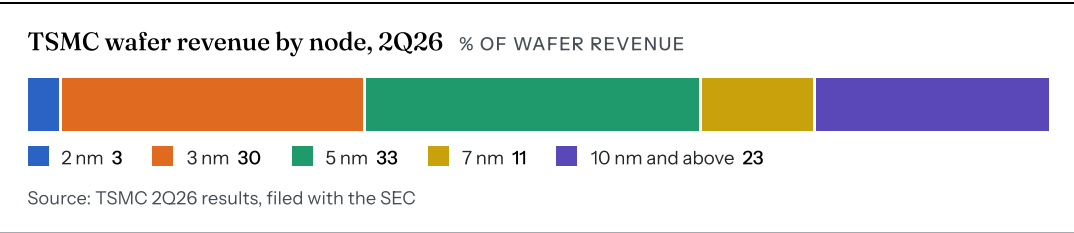
5 Testimony of the Semiconductor Industry Association (SIA). Senate · 2 March 2026 [\[A\]](https://www.epw.senate.gov/public/_cache/files/a/c/ac4552ff-551b-40d5-bea6-19dd17a1cfea/1F7BCD91016CBE...) [epw.senate.gov/public/_cache/files/a/c/ac4552ff-551b-40d5-bea6-19dd17a1cfea/1F7BCD91016CBE...](https://www.epw.senate.gov/public/_cache/files/a/c/ac4552ff-551b-40d5-bea6-19dd17a1cfea/1F7BCD91016CBE...)

Every plant TSMC and its subsidiaries run came to more than 17 million wafers a year in 2025, counted as if each were the standard 12-inch size ². The six largest plants, called gigafabs, had a combined capacity of more than 13 million ¹. All six are in Taiwan, and the other plants are five smaller fabs in Taiwan, two fabs in China, two in the United States and one in Japan ².

Variants and trade-offs

Pure-play foundries

TSMC and UMC build only for others. Chips at 7 nm and below, meaning the newest processes, were 77 percent of TSMC's wafer revenue in the second quarter of 2026, split 33 percent at 5 nm, 30 at 3 nm, 11 at 7 nm and 3 at 2 nm, on revenue of \$40.20 billion at a 67.7 percent gross margin ⁶.



Integrated device makers turned foundry

Intel and Samsung design and sell their own chips and rent out capacity too. Renting out capacity is harder for them, because customers dislike handing designs to a competitor and the company's own products take the best capacity. Intel Foundry reported \$5.8 billion of segment revenue in the second quarter of 2026 and an operating loss of \$2.089 billion ⁷. Only \$293 million of that revenue came from outside customers, and Intel says substantially all of its foundry business still makes Intel's own products ⁸.

National champions

SMIC, Hua Hong and Rapidus have government backing. SMIC's revenue rose 16.2 percent to \$9.327 billion in 2025 at 93.5 percent utilization, on monthly capacity above a million wafers counted in the smaller 8-inch size, and a 21 percent gross

2 Fab Capacity. TSMC tsmc.com/english/dedicatedFoundry/manufacturing/fab_capacity

1 GIGAFAB® Facilities. TSMC tsmc.com/english/dedicatedFoundry/manufacturing/gigafab

6 TAIWAN SEMICONDUCTOR MANUFACTURING CO LTD, Form 6-K report of foreign private issuer for the period ended 2026-06-30 (6-K). U.S. Securities and Exchange Commission (filing by TAIWAN SEMICONDUCTOR MANUFACTURING CO LTD) · 16 July 2026 sec.gov/Archives/edgar/data/0001046179/000104617926000451/a2q26e_withguidancexfinal.htm

7 Intel Reports Second-Quarter 2026 Financial Results. Intel · 23 July 2026 intc.com/news-events/press-releases/detail/1776/intel-reports-second-quarter-2026-financia...

8 INTEL CORP, Form 10-Q quarterly report for the period ended 2026-06-27 (10-Q). U.S. Securities and Exchange Commission (filing by INTEL CORP) · 24 July 2026 sec.gov/Archives/edgar/data/50863/000005086326000157/intc-20260627.htm

margin ⁹. SMIC cannot buy an EUV scanner, yet it makes 7 nm-class chips on its N+2 and N+3 processes by printing the tightest layers in several passes on older deep-ultraviolet scanners ¹⁰. CSET reported in June 2024 that Huawei's Ascend 910B AI chip is believed to be made on N+2, and that SMIC's limited 7 nm capacity forced Huawei to choose between its most advanced phone chips and its AI chips ¹¹. SemiAnalysis judged in April 2025 that most 910B and 910C chips were in fact made on TSMC's 7 nm process, from wafers Huawei bought through another company ¹². Rapidus raised 267.6 billion yen from the Japanese government and 32 companies in February 2026 to carry it to 2 nm mass production by 2027 ¹³.

Mature-node capacity

Most wafers come off older lines, which make power devices, analog chips and microcontrollers and compete on price. In January 2025 the industry association SEMI forecast that foundry capacity at all nodes would rise from 11.3 million wafers a month in 2024 to a record 12.6 million in 2025, counted in the 8-inch size ¹⁴. Its June 2024 forecast had credited much of that growth to Intel's new foundry business and China's expansion ¹⁵. In July 2025 Intel scaled back its own fab plans, saying it would no longer go ahead with planned projects in Germany and Poland and would slow construction in Ohio ¹⁶.

Capacity and cost

TSMC added \$100 billion in March 2025 to the \$65 billion already committed in Phoenix, for three more fabs, two packaging plants and an R&D center ¹⁷. In July 2026 it added another \$100 billion for four more fabs at 2 nm or below, taking its total investment in Arizona to \$265 billion across 12 facilities ¹⁸. All of TSMC's gigafabs are still in Taiwan ².

Some customers pay TSMC in advance to hold capacity at its fabs, and these deposits stood at NT\$189.9 billion at the end of 2025, down from NT\$291.1 billion a year earlier ¹⁹. In 2025 the four largest AI chip designers used around 90 percent of

9 SMIC Announces 2025 Annual Results. SMIC [\[A\]](https://smics.com/en/site/news_read/7951) smics.com/en/site/news_read/7951

10 Is SMIC N+3's Metal Pitch Smaller than Intel 18A's?. SemiAnalysis · 14 June 2026 [\[B\]](https://newsletter.semianalysis.com/p/steel-smic-n3-teardown) newsletter.semianalysis.com/p/steel-smic-n3-teardown

11 Pushing the Limits: Huawei's AI Chip Tests U.S. Export Controls. Center for Security and Emerging Technology (CSET) · 17 June 2024 [\[A\]](https://cset.georgetown.edu/publication/pushing-the-limits-huaweis-ai-chip-tests-u-s-export-controls) cset.georgetown.edu/publication/pushing-the-limits-huaweis-ai-chip-tests-u-s-export-controls

12 Huawei AI CloudMatrix 384. SemiAnalysis · 16 April 2025 [\[B\]](https://newsletter.semianalysis.com/p/huawei-ai-cloudmatrix-384-chinas-answer-to-nvidia-gb200-nvl72) newsletter.semianalysis.com/p/huawei-ai-cloudmatrix-384-chinas-answer-to-nvidia-gb200-nvl72

13 Rapidus Secures 267.6 Billion Yen in Funding from Japan Government and Private Sector Companies This strategic funding plan will enable Rapidus to steadily progress from its current R&D phase to mass production of 2nm logic semiconductors by 2027 - Information - Rapidus Corporation. Rapidus [\[A\]](https://rapidus.inc/en/news_topics/information/rapidus-secures-267-6-billion-yen-in-funding-from-j...) rapidus.inc/en/news_topics/information/rapidus-secures-267-6-billion-yen-in-funding-from-j...

14 Eighteen new semiconductor fabs to start construction in 2025 semi reports (SEMI website). SEMI [\[A\]](https://semi.org/en/semi-press-release/eighteen-new-semiconductor-fabs-to-start-construction-in-20...) semi.org/en/semi-press-release/eighteen-new-semiconductor-fabs-to-start-construction-in-20...

15 Global Semiconductor Fab Capacity Projected to Expand 6% in 2024 and 7% in 2025, SEMI Reports. SEMI · 18 June 2024 [\[A\]](https://semi.org/en/news-media-press-releases/semi-press-releases/global-semiconductor-fab-capacity...) semi.org/en/news-media-press-releases/semi-press-releases/global-semiconductor-fab-capacity...

16 Intel Reports Second-Quarter 2025 Financial Results. Intel · 24 July 2025 [\[A\]](https://intc.com/news-events/press-releases/detail/1745/intel-reports-second-quarter-2025-financia...) intc.com/news-events/press-releases/detail/1745/intel-reports-second-quarter-2025-financia...

17 TSMC Intends to Expand Its Investment in the United States to US\$165 Billion to Power the Future of AI. TSMC · 4 March 2025 [\[A\]](https://pr.tsmc.com/english/news/3210) pr.tsmc.com/english/news/3210

18 TSMC Announces Additional \$100 Billion Investment In Arizona. City of Phoenix · 16 July 2026 [\[A\]](https://phoenix.gov/newsroom/ced-news/tsmc-announces-additional-100-billion-investment-in-arizona...) phoenix.gov/newsroom/ced-news/tsmc-announces-additional-100-billion-investment-in-arizona...

2 Fab Capacity. TSMC [\[A\]](https://tsmc.com/english/dedicatedFoundry/manufacturing/fab_capacity) tsmc.com/english/dedicatedFoundry/manufacturing/fab_capacity

19 TAIWAN SEMICONDUCTOR MANUFACTURING CO LTD, Form 20-F annual report for the period ended 2025-12-31 (20-F). U.S. Securities and Exchange Commission (filing by TAIWAN SEMICONDUCTOR MANUFACTURING CO LTD) · 16 April 2026 [\[A\]](https://sec.gov/Archives/edgar/data/1046179/000162828026025362/tsm-20251231.htm) sec.gov/Archives/edgar/data/1046179/000162828026025362/tsm-20251231.htm

the world's CoWoS packaging capacity and HBM memory supply, against only 12 percent of advanced logic production ²⁰. See Advanced packaging.

Who makes it

Intel is now partly state-owned. In August 2025 Washington bought 433.3 million newly issued Intel shares at \$20.47, or \$8.9 billion, for a 9.9 percent stake, paid out of \$5.7 billion of unpaid CHIPS Act grants and \$3.2 billion from the Secure Enclave program. The stake is passive, with no board seat, and the government agreed to vote with Intel's board on matters that need shareholder approval, with limited exceptions. The deal also came with a five-year warrant to buy a further 5 percent of Intel at \$20 a share, which Washington can exercise only if Intel's ownership of its foundry business falls below 51 percent ²¹.

Intel's technical position improved in 2026. It reached high-volume manufacturing on part of Panther Lake using ASML's High-NA extreme ultraviolet scanners, and put 18A-P into risk production, the trial runs a process goes through before it is signed off ⁷.

Samsung broke ground in Taylor, Texas, in 2022 on a plant with an initial minimum investment of \$17 billion, \$6 billion of buildings and \$11 billion of equipment ²². In December 2024 the Commerce Department awarded Samsung up to \$4.745 billion of CHIPS Act funding to support more than \$37 billion of planned investment in Central Texas, covering two new leading-edge logic fabs and a research fab in Taylor and an expansion of its existing plant in Austin ²³.

The chokepoint

In June 2024 SEMI forecast China at 10.1 million wafers a month in 2025, the most of any region, against Taiwan's 5.8 million out of a world total of 33.7 million ¹⁵. In the third-quarter 2026 update of its World Fab Forecast, SEMI projected that China would keep the largest installed capacity in 2026 and 2027 ²⁴. Little of China's is advanced; in 2022 South Korea and Taiwan held almost all of the world's logic capacity below 10 nm ²⁵. The United States had almost no capacity below 10 nm in 2022, and in May 2024 SIA and BCG projected it would hold 28 percent of it by 2032, while new fab investment worldwide reaches around \$2.3 trillion from 2024 to 2032 ²⁵.

20 Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip production in 2025. Epoch AI · 12 March 2026 [\[A\]](#) epoch.ai/data-insights/ai-chip-supply-chain-constraints

21 Intel and Trump Administration Reach Historic Agreement to Accelerate American Technology and Manufacturing Leadership. Intel · 22 August 2025 [\[A\]](#) intc.com/news-events/press-releases/detail/1748/intel-and-trump-administration-reach-histo...

7 Intel Reports Second-Quarter 2026 Financial Results. Intel · 23 July 2026 [\[A\]](#) intc.com/news-events/press-releases/detail/1776/intel-reports-second-quarter-2026-financia...

22 Taylor | US Fab | Samsung Semiconductor Global. Samsung Electronics · 11 September 2025 [\[A\]](#) semiconductor.samsung.com/sas/company/taylor

23 Biden-Harris Administration Announces CHIPS Incentives Award with Samsung Electronics to Solidify U.S. Leadership in Leading-Edge Semiconductor Production. NIST · 20 December 2024 [\[A\]](#) nist.gov/news-events/news/2024/12/biden-harris-administration-announces-chips-incentives-a...

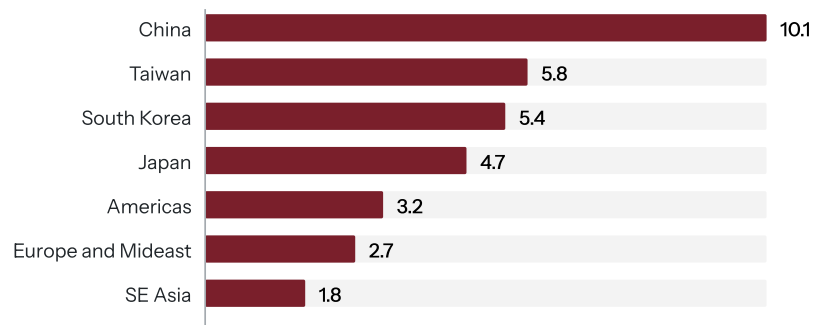
15 Global Semiconductor Fab Capacity Projected to Expand 6% in 2024 and 7% in 2025, SEMI Reports. SEMI · 18 June 2024 [\[A\]](#) semi.org/en/news-media-press-releases/semi-press-releases/global-semiconductor-fab-capacit...

24 World fab forecast (SEMI website). SEMI [\[A\]](#) semi.org/en/products-services/market-data/world-fab-forecast

25 R AJ VA RA DA RA JA N / I ACOB KOCH - W E SE R / CH RI S RI CH A RD / JOSE P H FI TZ GE RA L D /. Semiconductor Industry Association · 9 May 2024 [\[A\]](#) semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconduc...

Installed wafer fab capacity by region, 2025, as forecast by SEMI in June 2024, all nodes

MILLION 8-INCH-EQUIVALENT WAFERS PER MONTH



Source: SEMI World Fab Forecast, June 2024

Three risks meet on one island:

- **Seismic.** Taiwan sits on an active plate boundary, and after an earthquake in January 2025 TSMC had to scrap a number of wafers in process ²⁶.
- **Power.** A gigafab is a large industrial load on a small island grid.
- **Political.** Taiwan held 69 percent of the world's logic capacity below 10 nm in 2022 ²⁵. In December 2025 SemiAnalysis put Taiwan's share of the world's advanced-node capacity, a term it did not tie to a node size, at over 90 percent, so a blockade or conflict would cut most of that output off from the world market at once ²⁷. See Geopolitics.

Diversification is slow, and TSMC has yet to build a gigafab anywhere but Taiwan ².

Key evaluation criteria

- **Leading-edge share.** The share of revenue from the newest processes, 77 percent of TSMC's wafer revenue at 7 nm and below in the second quarter of 2026 ⁶.
- **Yield at ramp.** How many good chips a new process gives in its first year, which separates a profitable node from a subsidized one.
- **Ten-year cost of ownership.** \$35 to \$43 billion for a new 2 nm-class fab finished in 2026, in BCG's 2023 estimate, and rising ⁴.
- **Utilization.** How full the lines run. SMIC's lines ran 93.5 percent full in 2025, at a 21 percent gross margin ⁹.
- **Customer concentration.** A foundry owned by a chipmaker competes with its own customers, which caps who will trust it with a flagship design.

²⁶ News 3204 (TSMC website). TSMC [\[A\]](https://pr.tsmc.com/english/news/3204) pr.tsmc.com/english/news/3204

²⁵ R AJ VA RA DA RA JA N / I ACOB KOCH - W E S E R / CH RI S RI CH A RD / JOSE P H FI TZ GE RA L D /. Semiconductor Industry Association · 9 May 2024 [\[A\]](https://www.semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconduc...) semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconduc...

²⁷ TSMC Overseas Fabs – A Success?. SemiAnalysis · 1 December 2025 [\[B\]](https://newsletter.semianalysis.com/p/tsmc-overseas-fabs-a-success) newsletter.semianalysis.com/p/tsmc-overseas-fabs-a-success

² Fab Capacity. TSMC [\[A\]](https://tsmc.com/english/dedicatedFoundry/manufacturing/fab_capacity) tsmc.com/english/dedicatedFoundry/manufacturing/fab_capacity

⁶ TAIWAN SEMICONDUCTOR MANUFACTURING CO LTD, Form 6-K report of foreign private issuer for the period ended 2026-06-30 (6-K). U.S. Securities and Exchange Commission (filing by TAIWAN SEMICONDUCTOR MANUFACTURING CO LTD) · 16 July 2026 [\[A\]](https://sec.gov/Archives/edgar/data/0001046179/000104617926000451/a2q26e_withguidancexfinal.htm) sec.gov/Archives/edgar/data/0001046179/000104617926000451/a2q26e_withguidancexfinal.htm

⁴ Navigating the Costly Economics of Chip Making. Boston Consulting Group · 28 September 2023 [\[A\]](https://bcg.com/publications/2023/navigating-the-semiconductor-manufacturing-costs) bcg.com/publications/2023/navigating-the-semiconductor-manufacturing-costs

⁹ SMIC Announces 2025 Annual Results. SMIC [\[A\]](https://smics.com/en/site/news_read/7951) smics.com/en/site/news_read/7951

- **Geographic exposure.** How much of a buyer's supply sits on one island, one grid, one fault system.

FOUR THINGS TO REMEMBER

- A foundry makes chips for other companies, because no chip company can fill a fab alone.
- All six of TSMC's largest plants are in Taiwan.
- Money can buy a fab building, and training the workforce is the slow part.
- SEMI projected in 2026 that China would keep the world's largest installed fab capacity in 2026 and 2027, and little of it is advanced.

Memory and HBM

Three firms make nearly all the HBM sold worldwide. From HBM4 on, the package specification lets a finished stack stand 775 micrometers tall.

IN PLAIN TERMS

High bandwidth memory, or HBM, is where an AI chip keeps the numbers it is working on, and it is built to hand them over fast. A memory maker etches tiny holes into each memory wafer, fills them with copper, grinds the wafer until the copper shows through its back, tests each chip, and stacks up to sixteen good chips into a cube so that every layer is wired to the ones below. The cube then sits beside the processor, the chip that does the calculating. Stacking is the hard part, because each chip is ground very thin, the finished cube has to stay within a set height, and a chip that fails after stacking can scrap the whole cube. Only SK hynix, Samsung and Micron have made it work at scale, and a single line in an American export control reaches all three.

IN SHORT

Three companies, SK hynix, Samsung and Micron, make nearly all high-bandwidth memory (HBM), the stacked memory chips that sit beside an AI processor, and SK hynix alone sold 63.2 percent of it in 2025 ¹³. Since December 2024, HBM with a bandwidth density above 2 GB per second per square millimeter has been a controlled export to China under ECCN 3A090.c, including stacks made outside the United States, and BIS said every stack then in production crossed that line ¹. A license exception still lets exporters headquartered in the United States or a close ally ship HBM below 3.3 GB per second per square millimeter without a license, if the chip's designer buys it directly and it goes straight to the packaging site ²⁰. CSIS noted in December 2024 that HBM already packaged with a processor is judged by the chip performance rules instead, which then kept Nvidia's H20, with its HBM3, exportable to China ²¹. In late 2024, China's main memory maker, CXMT, was working toward mass production of HBM2, a generation introduced in 2016 ²¹. The Institute for Progress estimated in October 2025 that, even with CXMT planning to produce HBM3 in 2026, the United States and its partners would make 70 times as much HBM as China that year ²².

¹³ SK hynix Inc., Form 424B4 prospectus for the period ended 2026-07-10 (424(B)(4)). U.S. Securities and Exchange Commission (filing by SK hynix Inc.) · 10 July 2026 [A](https://sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm) sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm

¹ Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items. Federal Register (Commerce Department; Industry and Security Bureau) · 5 December 2024 [A](https://federalregister.gov/documents/2024/12/05/2024-28270/foreign-produced-direct-product-rule-a...)

²⁰ 15 CFR 740.25 -- License Exception High Bandwidth Memory (HBM).. Electronic Code of Federal Regulations [A](https://ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-740/section-740.25)

²¹ Understanding the Biden Administration's Updated Export Controls. Center for Strategic and International Studies · 11 December 2024 [A](https://csis.org/analysis/understanding-biden-administrations-updated-export-controls)

²² Should the US Sell Blackwell Chips to China?. Institute for Progress · 25 October 2025 [A](https://ifp.org/the-b30a-decision)

CHOKEPOINT CARD		EXTREME CONCENTRATION	HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY		PRICE OR MARKET SIZE
Extreme	Hard Three firms ship nearly all HBM, and no fourth firm has both the newest DRAM and a line that stacks it.		An HBM stack moves data over a path 16 times wider than a DDR5 memory module's That width costs chip area and lowers the share of stacks that come out working.
WHO LEADS	KR SK hynix 63.2% of HBM revenue, 2025; says it was first to complete HBM4 development, September 2025, at over 10 Gbps per pin KR Samsung 19.3% of HBM revenue, 2025; says it shipped the industry's first commercial HBM4 in February 2026, at 11.7 Gbps per pin on a 4 nm logic base die US Micron 17.4% of HBM revenue, 2025; HBM4 above 11 Gbps per pin		
WHERE IT IS MADE	KR South Korea SK hynix Cheongju and Icheon; Samsung Pyeongtaek and Hwaseong US United States Micron headquarters and R&D; SK hynix packaging plant under construction in Indiana TW Taiwan Micron DRAM and HBM production; TSMC builds the HBM4 base die for SK hynix JP Japan Micron Hiroshima, 1-gamma DRAM SG Singapore Micron HBM advanced packaging plant, adding capacity from 2027		
WHY SUBSTITUTION IS SLOW	Among the three HBM makers, market share moves quickly, and Micron went from 5.8 percent of HBM revenue in 2024 to 23.1 percent in the first quarter of 2026. A fourth maker would be harder. It would need the newest DRAM, a line that drills through and thins wafers, and a way to stack the thinned chips without warping them, all inside one company. Its stack would then have to pass a customer's qualification tests, and no Chinese firm ships HBM3E or HBM4 in volume yet.		
WHERE CHINA STANDS		WHERE THE US STANDS	
No Chinese firm ships HBM3E or HBM4 in volume. CXMT, China's strongest DRAM maker, was planning in October 2025 to produce HBM3 in 2026, and CSIS called it in December 2024 one of only two Chinese firms with a credible path to producing advanced HBM. Huawei said in September 2025 that its Ascend 950 chips would use two HBM designs of its own, HiBL 1.0 and HiZQ 2.0, and that the 950DT, due in the fourth quarter of 2026, would carry 144 GB of HiZQ 2.0 at 4 TB/s. The announcement did not say who would manufacture the memory.		Micron is the only American HBM maker. BIS, the US export control office, controls HBM with a memory bandwidth density above 2 GB per second per square millimeter under control number ECCN 3A090.c, and shipping it to Macau or a Country Group D:5 destination such as China needs a license unless an exception applies. BIS said in December 2024 that every HBM stack then in production exceeded that threshold. License Exception HBM (15 CFR 740.25) lets an exporter headquartered in the United States or a Country Group A:5 ally ship HBM below 3.3 GB per second per square	

millimeter without a license, if the designer of the co-packaged chip buys it directly and it goes straight to the packaging site. The control excludes co-packaged chips that combine HBM and logic and whose main function is processing, which the accelerator rules may cover instead.

An AI accelerator is a machine for moving numbers past arithmetic units, and arithmetic got cheap faster than the moving did. The US export control office notes that a processor cannot reach its full capabilities unless its memory capacity and bandwidth rise with its speed ¹.

How it works

Each layer in the cube is a DRAM chip, ground thin and bonded to the one below through microbumps, tiny metal bumps, and the whole stack sits on a base die that manages it. The copper-filled holes are TSVs, through-silicon vias, and they let a signal reach any layer without a wire around the outside.

An HBM3E cube talks to the processor over 1,024 wires at once, a 1,024-bit interface, sixteen times wider than a standard DDR5 memory module, the memory stick in a PC ². HBM4 doubles that to 2,048 wires ³. Ordinary memory cannot be made that wide, because the pins would not fit on a circuit board. The stack can, since its wires run down through the TSVs and across a silicon interposer to the processor beside it, with no board in the way ².

Answering a prompt is what the width is for. Training reuses each stored number across a huge multiplication, so a chip can fetch little and compute a lot. To generate one word of an answer, the chip reads the whole model from memory, and the whole record of the conversation so far, does a little arithmetic, and waits for the next read. That record grows with the length of the conversation and the number of users served at once. So memory size and speed usually set how many people one chip can serve.

Variants and trade-offs

GENERATION	INTERFACE	BANDWIDTH PER STACK	CAPACITY PER STACK
HBM3E	1,024-bit, 16 channels (32 pseudo-channels)	over 1.2 TB/s	24 GB (8 chips), 36 GB (12 chips)

¹ Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items. Federal Register (Commerce Department; Industry and Security Bureau) · 5 December 2024 [A](https://www.federalregister.gov/documents/2024/12/05/2024-28270/foreign-produced-direct-product-rule-a...)

² High-bandwidth memory (HBM). Micron Technology [A](https://www.micron.com/products/memory/hbm) [micron.com/products/memory/hbm](https://www.micron.com/products/memory/hbm)

³ JEDEC® and Industry Leaders Collaborate to Release JESD270-4 HBM4 Standard: Advancing Bandwidth, Efficiency, and Capacity for AI and HPC. JEDEC Solid State Technology Association · 16 April 2025 [A](https://www.jedec.org/news/pressreleases/jedec%C2%AE-and-industry-leaders-collaborate-release-jesd270-...)

HBM4	2,048-bit, 32 channels	over 2.0 TB/s, up to 3.3 TB/s	up to 64 GB (16 chips, 32 Gb dies)
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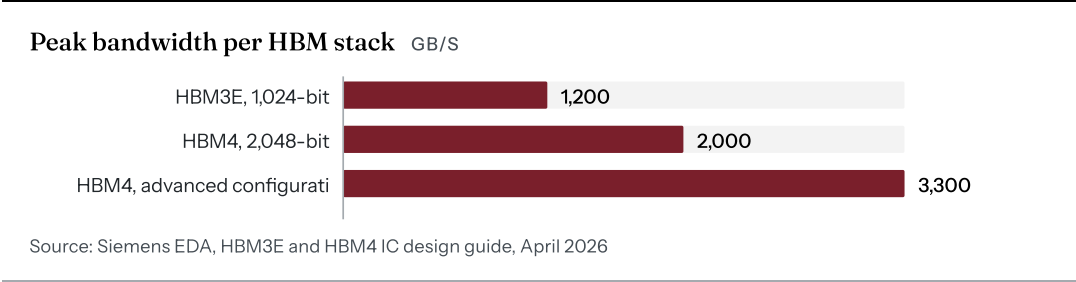
HBM3E

Micron ships the high-volume parts, 24 GB with eight chips stacked and 36 GB with twelve ⁴. SK hynix's January 2026 market outlook says major research and brokerage analysts expect HBM3E to be about two thirds of all HBM shipments in 2026 ⁵.

HBM4

The standards body JEDEC published JESD270-4 in April 2025, setting the 2,048-bit interface and 2 TB/s per stack at 8 Gb/s per pin ³. SK hynix says it was first to complete HBM4 development, in September 2025, at over 10 Gb/s per pin ⁶. Samsung says it began mass production and shipped the first commercial HBM4 in February 2026, at 11.7 Gb/s per pin, with a 4 nm logic base die ⁷. Micron's parts run above 11 Gb/s for more than 2.8 TB/s per stack ⁸.

The chip at the bottom of the stack is a base die, and SK hynix, which made its own base dies up to HBM3E, chose TSMC's advanced logic process for the HBM4 base die so it can hold more functions ⁹. That gives TSMC a role inside a product it does not make.



How a stack is built

- **Drill and thin.** Etch vertical holes, the through-silicon vias, into a memory wafer, fill them with copper, then grind the wafer from behind until the copper comes through.

4 Micron, HBM3E product page. Micron Technology micron.com/products/memory/hbm/hbm3e

5 2026 Market Outlook – “Focus on the HBM-Led Memory Supercycle”. SK hynix news.skhynix.com/en/2026-market-outlook-focus-on-the-hbm-led-memory-supercycle

3 JEDEC® and Industry Leaders Collaborate to Release JESD270-4 HBM4 Standard: Advancing Bandwidth, Efficiency, and Capacity for AI and HPC. JEDEC Solid State Technology Association · 16 April 2025 jedec.org/news/pressreleases/jedec%C2%AE-and-industry-leaders-collaborate-release-jesd270-4

6 SK hynix Completes World’s First HBM4 Development and Readies Mass Production. SK hynix news.skhynix.com/en/sk-hynix-completes-worlds-first-hbm4-development-and-readies-mass-prod...

7 Samsung Ships Industry-First Commercial HBM4 With Ultimate Performance for AI Computing - Samsung Global Newsroom. Samsung Global Newsroom · 12 February 2026 news.samsung.com/global/samsung-ships-industry-first-commercial-hbm4

8 Micron, HBM4 product page. Micron Technology micron.com/products/memory/hbm/hbm4

9 SK hynix Partners with TSMC to Strengthen HBM Technological Leadership. SK hynix news.skhynix.com/sk-hynix-partners-with-tsmc-to-strengthen-hbm-technological-leadership

- **Stack and join.** The chips are joined by thermocompression bonding, which connects them through metal bumps under heat and pressure and comes in several forms ¹¹. SK hynix uses Advanced MR-MUF, which stacks the chips, injects a liquid protective material between them and hardens it, and the company says the process controls warping and dissipates heat well ⁶. Samsung said in February 2024 that its twelve-high HBM3E uses TC-NCF, thermocompression with a thin non-conductive film between the chips, which it expected to help limit warping as chips get thinner ¹².
- **Stay under the height limit.** HBM4 raised the package specification height of a finished cube from 720 micrometers to 775, still under a millimeter ¹¹.

Hybrid bonding is the next step and it is not ready. Pressing copper pad straight onto copper pad, with no solder and no filler, would cut the spacing between connections from about 20 micrometers to under 1, but a tech note on SK hynix's newsroom says full-scale adoption in HBM is most likely at HBM4E or HBM5, where stacks are projected to pass twenty layers ¹¹.

Who makes it

Ordinary computer memory, DRAM, is a three-firm oligopoly, and HBM is the same three firms reordered: SK hynix, Samsung and Micron ¹³. Nobody else has both leading-edge DRAM and a stacking line inside one company.

SK hynix was the first company to mass-produce several generations of HBM, including HBM3 and HBM3E ¹³. UBS, as quoted in SK hynix's January 2026 market outlook, expected SK hynix to take about 70 percent of the HBM4 market for Nvidia's Rubin platform in 2026 ⁵. Samsung says it shipped the first commercial HBM4 in February 2026 ⁷. SK hynix broke ground in August 2026 on an advanced packaging plant in West Lafayette, Indiana, an investment of over \$4

¹¹ [Tech Note] Hybrid Bonding: Evolving into a Foundational Technology for Improving Semiconductor Performance. SK hynix [\[A\] news.skhynix.com/en/tech-note-series-ep2](https://news.skhynix.com/en/tech-note-series-ep2)

⁶ SK hynix Completes World's First HBM4 Development and Readies Mass Production. SK hynix [\[A\] news.skhynix.com/en/sk-hynix-completes-worlds-first-hbm4-development-and-readies-mass-prod...](https://news.skhynix.com/en/sk-hynix-completes-worlds-first-hbm4-development-and-readies-mass-prod...)

¹² Samsung Develops Industry-First 36GB HBM3E 12H DRAM - Samsung Global Newsroom. Samsung Global Newsroom · 27 February 2024 [\[A\] news.samsung.com/global/samsung-develops-industry-first-36gb-hbm3e-12h-dram](https://news.samsung.com/global/samsung-develops-industry-first-36gb-hbm3e-12h-dram)

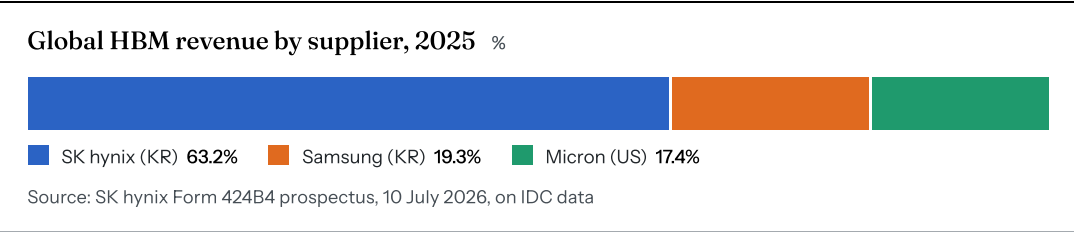
¹³ SK hynix Inc., Form 424B4 prospectus for the period ended 2026-07-10 (424(B)(4)). U.S. Securities and Exchange Commission (filing by SK hynix Inc.) · 10 July 2026 [\[A\] sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm](https://sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm)

⁵ 2026 Market Outlook – “Focus on the HBM-Led Memory Supercycle”. SK hynix [\[A\] news.skhynix.com/en/2026-market-outlook-focus-on-the-hbm-led-memory-supercycle](https://news.skhynix.com/en/2026-market-outlook-focus-on-the-hbm-led-memory-supercycle)

⁷ Samsung Ships Industry-First Commercial HBM4 With Ultimate Performance for AI Computing - Samsung Global Newsroom. Samsung Global Newsroom · 12 February 2026 [\[A\] news.samsung.com/global/samsung-ships-industry-first-commercial-hbm4](https://news.samsung.com/global/samsung-ships-industry-first-commercial-hbm4)

billion ¹⁴. Micron is modernizing its DRAM and HBM production capacity in Taiwan and has broken ground on an HBM advanced packaging plant in Singapore to expand its packaging capacity from 2027 ¹⁵.

The split is on the record because SK hynix registered shares in the United States: of 2025 HBM revenue, SK hynix took 63.2 percent, Samsung 19.3 and Micron 17.4 ¹³. The filing credits the research firm IDC. These shares move fast, and in 2024 the same three stood at 56.4, 37.8 and 5.8 percent ¹³. In the first quarter of 2026 they stood at 56.4, 20.5 and 23.1 percent ¹³.



Bank of America, in an estimate SK hynix quoted in January 2026, put the 2026 HBM market at \$54.6 billion, up 58 percent on 2025 ⁵. SK hynix says HBM requires greater wafer input than traditional DRAM ¹³. It also says the industry-wide reallocation of production capacity to HBM has left traditional DRAM, the kind used in PCs and phones, undersupplied, which helped drive a significant price recovery in that market from the third quarter of 2025 ¹³.

The chokepoint

Every leading accelerator made outside China depends on Korean or American HBM. Nvidia's GB300 NVL72 carries 20 TB of HBM3E at up to 576 TB/s ¹⁶, Rubin up

14 SK hynix breaks ground on \$4 billion advanced packaging production facility in Purdue Research Park. Purdue University · 27 August 2026 [\[A\]](#) purdue.edu/newsroom/2026/Q3/sk-hynix-breaks-ground-on-4-billion-advanced-packaging-product...

15 MICRON TECHNOLOGY INC, Form 10-K annual report for the period ended 2025-08-28 (10-K). U.S. Securities and Exchange Commission (filing by MICRON TECHNOLOGY INC) · 3 October 2025 [\[A\]](#) sec.gov/Archives/edgar/data/723125/000072312525000028/mu-20250828.htm

13 SK hynix Inc., Form 424B4 prospectus for the period ended 2026-07-10 (424(B)(4)). U.S. Securities and Exchange Commission (filing by SK hynix Inc.) · 10 July 2026 [\[A\]](#) sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm

5 2026 Market Outlook – “Focus on the HBM-Led Memory Supercycle”. SK hynix [\[A\]](#) news.skhynix.com/en/2026-market-outlook-focus-on-the-hbm-led-memory-supercycle

16 NVIDIA GB300 NVL72. Nvidia · 23 July 2026 [\[A\]](#) nvidia.com/en-us/data-center/gb300-nvl72

to 288 GB of HBM4 per GPU at up to 22 TB/s ¹⁷, and AMD's MI355X 288 GB of HBM3E at 8 TB/s ¹⁸.

The Bureau of Industry and Security rule of 5 December 2024, at 89 FR 96790, added an export classification, ECCN 3A090.c, for "High bandwidth memory (HBM) having a 'memory bandwidth density' greater than 2 gigabytes per second per square millimeter". Its technical note defines that density as the memory bandwidth in gigabytes per second divided by the area of the package or stack in square millimeters. The rule also reaches stacks made outside the United States, through a foreign direct product rule that catches goods made abroad with American technology ¹. BIS stated in the rule that all HBM stacks then in production exceeded that threshold ¹. Under 15 CFR 742.6(b)(10)(ii) BIS reviews applications for 3A090.c to Macau or a Country Group D:5 destination such as China with a presumption of approval when neither the buyer nor its ultimate parent is headquartered in one of those places, and with a presumption of denial otherwise ¹⁹.

Two provisions narrow the control. License Exception HBM, at 15 CFR 740.25, lets an exporter headquartered in the United States or a Country Group A:5 ally ship HBM below 3.3 GB per second per square millimeter without a license, if the designer of the co-packaged chip buys it directly and it goes straight to the packaging site ²⁰. The rule also excludes co-packaged chips that combine HBM and logic and whose main function is processing, which other chip controls may cover instead ¹. CSIS said in December 2024 that the rules still allowed HBM2 to go to China with end-use and end-user restrictions, and that Nvidia's H20, whose HBM3 is packaged with the processor, was then still exportable under the accelerator thresholds ²¹.

In December 2024 CSIS called China's strongest DRAM maker, CXMT, one of only two Chinese firms with a credible path to producing advanced HBM ²¹. The Institute for Progress reported in October 2025 that CXMT was planning to

17 Inside NVIDIA Rubin GPU Architecture: Powering the Era of Agentic AI. Nvidia · 21 July 2026 [\[A\]](https://developer.nvidia.com/blog/inside-nvidia-rubin-gpu-architecture-powering-the-era-of-agentic-ai/) developer.nvidia.com/blog/inside-nvidia-rubin-gpu-architecture-powering-the-era-of-agentic-ai/

18 AMD Instinct™ MI355X GPUs. AMD [\[A\]](https://amd.com/en/products/accelerators/instinct/mi350/mi355x.html) amd.com/en/products/accelerators/instinct/mi350/mi355x.html

1 Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items. Federal Register (Commerce Department; Industry and Security Bureau) · 5 December 2024 [\[A\]](https://www.federalregister.gov/documents/2024/12/05/2024-28270/foreign-produced-direct-product-rule-a-) federalregister.gov/documents/2024/12/05/2024-28270/foreign-produced-direct-product-rule-a-...

19 15 CFR 742.6, Regional stability. Electronic Code of Federal Regulations [\[A\]](https://www.ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-742/section-742.6) ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-742/section-742.6

20 15 CFR 740.25 -- License Exception High Bandwidth Memory (HBM).. Electronic Code of Federal Regulations [\[A\]](https://www.ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-740/section-740.25) ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-740/section-740.25

21 Understanding the Biden Administration's Updated Export Controls. Center for Strategic and International Studies · 11 December 2024 [\[A\]](https://www.csis.org/analysis/understanding-biden-administrations-updated-export-controls) csis.org/analysis/understanding-biden-administrations-updated-export-controls

produce HBM3 in 2026 ²². Huawei said in September 2025 that its Ascend 950 chips would use two HBM designs of its own, HiBL 1.0 and HiZQ 2.0, and that the 950DT, due in the fourth quarter of 2026, would carry 144 GB of HiZQ 2.0 at 4 TB/s ²³. The announcement did not say who would manufacture the memory ²³. SK hynix says HBM requires advanced production processes such as TSV packaging and compliance with the rigorous testing and approval processes its customers set ¹³.

Key evaluation criteria

- **Bandwidth per stack** sets how fast a chip can serve answers: over 1.2 TB/s on HBM3E, over 2 TB/s on HBM4 ¹⁰.
- **Capacity per stack** decides how large a model fits on one accelerator, up to 64 GB with sixteen chips stacked in the JEDEC HBM4 standard ³. Samsung said in February 2026 that its twelve-high HBM4 comes in 24 to 36 GB and that sixteen-high parts would take it to 48 GB ⁷.
- **Stack height**, 775 micrometers in the HBM4 package specification, caps how many layers fit in a stack ¹¹.
- **Stack yield** matters because a chip that fails after stacking can scrap the whole cube. Micron sends only dies that pass testing on to assembly and tests the finished cube again ⁸.
- **Thermal path** gets harder with every layer, and heat dissipation becomes a major challenge at 16 to 20 layers as heat builds up in the stack ¹¹.
- **Qualification** means passing each customer's tests, and SK hynix credits its experience with complex qualification processes for its standing as a trusted HBM supplier ¹³.

FOUR THINGS TO REMEMBER

- HBM is memory stacked into a cube beside the processor and wired to pass data fast.

22 Should the US Sell Blackwell Chips to China?. Institute for Progress · 25 October 2025 [\[A\]](https://ifp.org/the-b30a-decision) ifp.org/the-b30a-decision

23 Groundbreaking SuperPoD Interconnect: Leading a New Paradigm for AI Infrastructure - Huawei. Huawei · 18 September 2025 [\[A\]](https://huawei.com/en/news/2025/9/hc-xu-keynote-speech) huawei.com/en/news/2025/9/hc-xu-keynote-speech

13 SK hynix Inc., Form 424B4 prospectus for the period ended 2026-07-10 (424(B)(4)). U.S. Securities and Exchange Commission (filing by SK hynix Inc.) · 10 July 2026 [\[A\]](https://sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm) sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm

10 HBM3e and HBM4: IC design guide for next-generation high bandwidth memory. Siemens Digital Industries Software · 24 April 2026 [\[A\]](https://blogs.sw.siemens.com/semiconductor-packaging/2026/04/24/hbm3e-hbm4-ic-design-guide) blogs.sw.siemens.com/semiconductor-packaging/2026/04/24/hbm3e-hbm4-ic-design-guide

3 JEDEC® and Industry Leaders Collaborate to Release JESD270-4 HBM4 Standard: Advancing Bandwidth, Efficiency, and Capacity for AI and HPC. JEDEC Solid State Technology Association · 16 April 2025 [\[A\]](https://jedec.org/news/pressreleases/jedec%C2%AE-and-industry-leaders-collaborate-release-jesd270-...) jedec.org/news/pressreleases/jedec%C2%AE-and-industry-leaders-collaborate-release-jesd270-...

7 Samsung Ships Industry-First Commercial HBM4 With Ultimate Performance for AI Computing - Samsung Global Newsroom. Samsung Global Newsroom · 12 February 2026 [\[A\]](https://news.samsung.com/global/samsung-ships-industry-first-commercial-hbm4) news.samsung.com/global/samsung-ships-industry-first-commercial-hbm4

11 [Tech Note] Hybrid Bonding: Evolving into a Foundational Technology for Improving Semiconductor Performance. SK hynix [\[A\]](https://news.skhynix.com/en/tech-note-series-ep2) news.skhynix.com/en/tech-note-series-ep2

8 Micron, HBM4 product page. Micron Technology [\[A\]](https://micron.com/products/memory/hbm/hbm4) micron.com/products/memory/hbm/hbm4

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- An AI chip reads its whole model from memory for each word, so memory speed limits it.
 - SK hynix, Samsung and Micron make nearly all HBM.
 - Since December 2024 US controls have covered the HBM stacks then in production, with two exceptions, and no Chinese firm ships HBM3E or HBM4 in volume.

Advanced Packaging

Lithography no longer sets the limit on the size of an AI accelerator. The limit now is how large an interposer, the wiring layer that joins the chips, TSMC can build, and how many it can build a month.

IN PLAIN TERMS

Packaging joins finished chips into one component and mounts them on a base, called a substrate, wired almost as finely as the chips themselves. A lithography machine, which prints a chip's circuits, can cover only a rectangle about the size of a postage stamp in one shot. Many leading accelerators, Nvidia's Blackwell among them, need more logic than fits in one, so they are made as several dies, set side by side on a shared interposer and wired together through it, with the stacked memory a few millimeters away. The interposer is one piece of silicon, or layers of fine copper wiring that often carry small silicon bridges where the links are densest. Interposer, chips and base all expand at different rates when heated, so the package can warp and its joints crack. Getting that right in large numbers is hard enough that nearly every AI accelerator is packaged by TSMC, in Taiwan.

IN SHORT

TSMC's chief executive said in July 2024 that demand for its CoWoS advanced packaging was so high that he could not yet balance supply and demand ¹⁰. Epoch AI found that CoWoS, which joins an AI chip's logic dies to its memory, and the memory itself were the main limits on AI chip production in 2025 ⁴. In March 2026, the analyst firm SemiAnalysis judged that CoWoS supply was easing and that the factories that print the chips had become the main bottleneck ⁷. TSMC's chief executive gave a different account on the July 2026 earnings call, saying that its packaging capacity was so tight that it limited customers' growth and that back-end capacity was still in shortage ¹². He welcomed Intel's EMIB-T and said he hoped it would take some of that load off TSMC ¹².

¹⁰ Q2 2024 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 18 July 2024 [\[A\]](https://investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2024-08/5122725a56670882d777a...)

⁴ Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip production in 2025. Epoch AI · 12 March 2026 [\[A\]](https://epoch.ai/data-insights/ai-chip-supply-chain-constraints)

⁷ The Great AI Silicon Shortage. SemiAnalysis · 12 March 2026 [\[B\]](https://newsletter.semianalysis.com/p/the-great-ai-silicon-shortage)

¹² Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. LSEG StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 July 2026 [\[A\]](https://investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897a...)

CHOKEPOINT CARD		EXTREME CONCENTRATION
		MODERATELY HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY	PRICE OR MARKET SIZE
Extreme	Moderate Intel's EMIB can do the same job as TSMC's CoWoS, and the real shortage is in making enough working packages at the volume Nvidia orders.	About 65,000 to 75,000 CoWoS wafers a month at the end of 2025, in industry estimates from SemiWiki and TrendForce compiled by Epoch AI, up from 35,000 to 40,000 a year earlier. TSMC does not publish its CoWoS capacity, and at its 2024 symposium it projected 60 percent annual growth for the next few years. Epoch AI estimates Nvidia alone used 60.3 percent of the world's CoWoS capacity in 2025
WHO LEADS	TW TSMC Almost all CoWoS for leading AI accelerators US Intel Foveros 3D packaging in volume at Rio Rancho, New Mexico; EMIB 2.5D bridges TW ASE Technology NT\$389.2B assembly, test and materials revenue, 2025; the leading provider of outsourced assembly and test US Amkor \$6.71B net sales, 2025; the largest American assembly and test firm CN JCET RMB 38.87B revenue, 2025; a leading Chinese assembly and test firm SG ASMPT \$532.1M advanced packaging revenue, 2025; thermocompression bonders	
WHERE IT IS MADE	TW Taiwan TSMC AP fabs and the OSAT cluster; almost all 2.5D capacity for AI accelerators US United States Intel Foveros packaging in volume at Rio Rancho, New Mexico; Amkor Peoria, Arizona from 2028; two TSMC advanced packaging plants planned in Arizona CN China JCET, Tongfu and HT-Tech; four of the top ten outsourced assembly and test firms by 2024 revenue are Chinese NL Netherlands Besi hybrid and die bonders JP Japan Disco grinders and dicers; TEL and Shibaura bonding tools	
WHY SUBSTITUTION IS POSSIBLE	None of the packaging steps is unusual, and Intel's EMIB is another 2.5D option, which Trainium and TPU were adopting to different degrees as of March 2026. The hard part is volume. A newcomer has to buy enough bonding machines and run enough practice lots to make the interposer at 5.5 times the area a scanner prints in one shot. It then has to attach the memory stacks, have them work, and do all of that at the volume Nvidia alone orders. Amkor's plant in Peoria, Arizona shows the timing. Its production is expected to start in early 2028, so the wait is two to five years.	

WHERE CHINA STANDS	WHERE THE US STANDS
Four of the top ten outsourced assembly and test firms by 2024 revenue are headquartered in China, and JCET alone had revenue of RMB 38.87 billion in 2025. Between 2019 and 2024, Chinese firms gained 5 percentage points of share in test tools and 4 points in fabrication tools built for advanced packaging, particularly etch and clean tools, but lost share in bonding and other conventional assembly and packaging tools, the category where CSET counts hybrid and thermocompression bonders. In 2024 China held 7 percent of advanced packaging fabrication tools, against 65 percent for the United States and 15 percent for Japan.	Intel opened Fab 9 in Rio Rancho, New Mexico, in January 2024 to make its Foveros 3D packages in volume, and called it the only US factory producing the most advanced packaging at scale. Intel offers its EMIB 2.5D packaging to outside customers, and SemiAnalysis reported in March 2026 that Trainium and TPU were adopting it to different degrees. No US site yet packages Nvidia-class accelerators with HBM on CoWoS. Amkor is building a \$7B packaging and test plant in Peoria, Arizona, with up to \$407M of CHIPS Act money, and expects production to start in early 2028.

A lithography scanner prints a rectangle 26 mm by 33 mm, or 858 mm², in one exposure ¹. Every AI accelerator worth buying is bigger than that. Packaging is the stage that lets an accelerator be larger than that rectangle, and it decides how much larger.

How it works

High bandwidth memory gives a second reason for the interposer. An HBM4 stack connects through 2,048 data signals, packed too tightly for a standard resin base board, so the memory sits beside the logic on that shared carrier, the interposer ². Even Nvidia's H100, whose single logic die is 814 mm² and fits inside one exposure, carries five HBM stacks ³. Epoch AI counts CoWoS packaging among the three inputs the H100 needs, along with its logic die and its HBM ⁴.

The name CoWoS says the order: chip onto wafer, then wafer onto substrate. For CoWoS-S, TSMC makes a thin silicon wafer carrying wiring and vertical copper vias, metal-filled holes that join one layer of wiring to the next, but no transistors. It bonds the logic dies and memory stacks face down onto that wafer with microbumps, dots of solder 30 to 40 microns apart, about a third of a hair's width, each dot one electrical joint. Then it cuts the interposer out of the wafer, attaches it to the resin substrate, and the substrate goes onto its board.

Each of those packaging steps is ordinary on its own. But one cracked joint scraps a package holding eight qualified HBM stacks and two large, expensive logic dies.

Variants and trade-offs

FAMILY	CARRIER	SIZE LIMIT	USED FOR
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1 TWINSKAN NXE:3400C. ASML [\[A\]](https://asml.com/en/products/euv-lithography-systems/twinscan-nxe3400c) asml.com/en/products/euv-lithography-systems/twinscan-nxe3400c

2 New JEDEC® SPHBM4 Standard Enables HBM4-Class Bandwidth on Organic Substrates. JEDEC Solid State Technology Association · 13 July 2026 [\[A\]](https://jedec.org/news/pressreleases/new-jedec%C2%AE-sphbm4-standard-enables-hbm4-class-bandwidth-...) jedec.org/news/pressreleases/new-jedec%C2%AE-sphbm4-standard-enables-hbm4-class-bandwidth-...

3 NVIDIA Hopper Architecture In-Depth. Nvidia · 22 March 2022 [\[A\]](https://developer.nvidia.com/blog/nvidia-hopper-architecture-in-depth) developer.nvidia.com/blog/nvidia-hopper-architecture-in-depth

4 Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip production in 2025. Epoch AI · 12 March 2026 [\[A\]](https://epoch.ai/data-insights/ai-chip-supply-chain-constraints) epoch.ai/data-insights/ai-chip-supply-chain-constraints

CoWoS-S	Full silicon interposer	3.3x reticle, about 2,700 mm2	H100-class parts
CoWoS-R	Resin interposer with fine redistribution wiring	Above 3.3x reticle	Cost-sensitive, fewer HBM stacks
CoWoS-L	Redistribution wiring with local silicon bridges	5.5x reticle in production, 9.5x in development	Blackwell, Rubin

2.5D: silicon, RDL and bridges

TSMC has run CoWoS in volume since 2012 ⁵. CoWoS-S wires most finely, but its interposer is one unbroken piece of silicon whose yield falls as the area grows. CoWoS-L replaces that slab with an interposer of redistribution wiring and small embedded silicon bridges where the wiring is densest ⁶. Intel's EMIB buries the same bridge idea in the resin substrate, and SemiAnalysis reported in March 2026 that Trainium and TPU were adopting it to different degrees ⁷.

Blackwell was the first high-volume design on CoWoS-L, and packaging issues at TSMC and in Nvidia's design limited its supply ⁸. The bridges carrying the 10 TB/s link between the two compute dies need very high placement accuracy, and the different expansion rates of the dies, bridges, interposer and substrate caused warpage ⁸.

3D: SoIC and Foveros

TSMC's SoIC and Intel's Foveros bond dies face to face, copper pad to copper pad with no solder, packing the connections far closer than microbumps allow. TSMC put 3 nm SoIC into volume production in 2025 ⁶. An A14-on-A14 version due in 2029 will carry 1.8 times the die-to-die connection density of the 2 nm version ⁹. Heat decides the layout: the bottom die overheats and the top is hard to power, so 3D designs often put cache underneath and compute on top.

The same bonding brings optics into the package. TSMC's COUPE uses SoIC to join a silicon photonics chip, which sends data as light, to its electrical control chip ⁶. TSMC said in April 2026 that COUPE on substrate would begin production in 2026, and that placing this optical engine inside the package gives twice the power efficiency of a pluggable version on the circuit board ⁹.

Two ways off the silicon interposer

Panel-level packaging swaps the round wafer for a rectangular panel and wastes far less area; see Test and assembly. JEDEC published SPHBM4 on 13 July 2026. It puts HBM4 memory on a base chip carrying 512 data signals instead of 2,048,

5 TSMC, CoWoS technology page. TSMC ^[A] 3dfabric.tsmc.com/english/dedicatedFoundry/technology/cowos.htm

6 TSMC 2025 Annual Report, chapter 5. TSMC ^[A] investor.tsmc.com/static/annualReports/2025/english/pdf/2025_tsmc_ar_e_ch5.pdf

7 The Great AI Silicon Shortage. SemiAnalysis · 12 March 2026 ^[B] newsletter.semianalysis.com/p/the-great-ai-silicon-shortage

8 Nvidia's Blackwell Reworked - Shipment Delays & GB200A Reworked Platforms. SemiAnalysis · 4 August 2024 ^[B] semianalysis.com/2024/08/04/nvidias-blackwell-reworked-shipment

9 TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC · 23 April 2026 ^[A] pr.tsmc.com/english/news/3302

which spaces the connections widely enough to mount the stack on a standard resin substrate, off the silicon interposer altogether ².

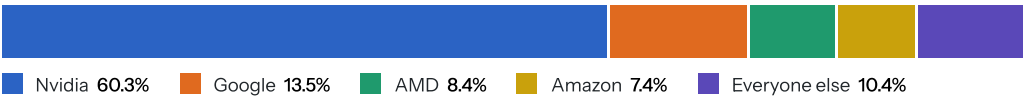
Capacity

TSMC does not publicly disclose its CoWoS capacity ⁴. Industry estimates from SemiWiki and TrendForce, compiled by Epoch AI, put it at about 65,000 to 75,000 wafers a month at the end of 2025, up from 35,000 to 40,000 a year earlier ⁴. At its 2024 symposium TSMC said capacity would grow at a 60 percent compound annual rate over the next few years, but when asked about that rate on the July 2024 earnings call, C.C. Wei said only that he would keep adding capacity wherever he could and could not yet balance supply and demand ¹⁰.

In October 2025 Wei would still say only that TSMC was working to increase capacity in 2026 and would probably give the real number in 2026, and that front-end and back-end capacity were both, in his words, very tight ¹¹.

Epoch AI weighs each designer's component use against world supply and puts Nvidia at 60.3 percent of all CoWoS in 2025, with a 90 percent confidence interval of 56.5 to 64.3; Google took 13.5, AMD 8.4 and Amazon 7.4 ⁴. Those four consumed around 90 percent of global CoWoS capacity and HBM supply, with HBM measured by value, while consuming only 12 percent of advanced logic die production ⁴.

Estimated share of CoWoS capacity used, 2025 %



Source: Epoch AI, advanced packaging and HBM were the bottlenecks on AI chip production in 2025

In March 2026, one analyst firm, SemiAnalysis, judged that front-end capacity had become the dominant bottleneck and CoWoS constraints were easing, and that TSMC was planning CoWoS capacity around its N3 limits because added packaging capacity is of no use without front-end wafers to fill it ⁷.

2 New JEDEC® SPHBM4 Standard Enables HBM4-Class Bandwidth on Organic Substrates. JEDEC Solid State Technology Association · 13 July 2026 [\[A\]](#) [jedec.org/news/pressreleases/new-jedec%25AE-sphbm4-standard-enables-hbm4-class-bandwidth-...](https://www.jedec.org/news/pressreleases/new-jedec%25AE-sphbm4-standard-enables-hbm4-class-bandwidth-...)

4 Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip production in 2025. Epoch AI · 12 March 2026 [\[A\]](#) epoch.ai/data-insights/ai-chip-supply-chain-constraints

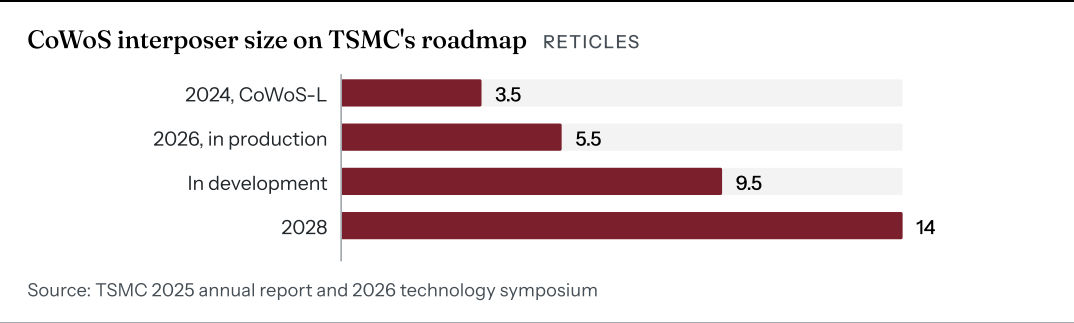
10 Q2 2024 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 18 July 2024 [\[A\]](#) investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2024-08/5122725a56670882d777a...

11 Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 October 2025 [\[A\]](#) investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2025-10/6860312f04fd291d0f26b...

7 The Great AI Silicon Shortage. SemiAnalysis · 12 March 2026 [\[B\]](#) newsletter.semianalysis.com/p/the-great-ai-silicon-shortage

TSMC gave a different account four months later. On the July 2026 earnings call, Wei said its packaging capacity was so tight that it limited customers' growth, and that back-end capacity was still in shortage ¹². Asked about Intel's EMIB-T, he said he welcomed the extra flexibility and hoped it would take some of the load off TSMC ¹².

Who makes it



The word packaging covers three kinds of firm. TSMC, which makes chips for others, and Intel, which makes its own, package chips in their own back-end fabs, and outsourced assembly and test firms do the rest. Intel opened Fab 9 in Rio Rancho, New Mexico, in January 2024 to make its Foveros 3D packages in volume, and called it the only US factory producing the most advanced packaging at scale ¹³. ASE Technology Holding, the leading provider of assembly and test services, billed NT\$645.4 billion in 2025, about 40 percent of it from electronics manufacturing services ¹⁴. Its assembly, test and materials business brought in NT\$389.2 billion, up from NT\$325.9 billion in 2024 ¹⁴. Amkor, the world's largest US-headquartered one, billed \$6.71 billion ¹⁵.

The tools are a narrower chokepoint than the assembly houses.

- **Thermocompression bonding.** Pressing dies together under heat and force. ASMPT's advanced packaging revenue reached \$532.1 million in 2025, with thermocompression bonder revenue up about 146 percent; it targets 35 to 40 percent of a market it puts at \$1.6 billion in 2028 ¹⁶.
- **Hybrid bonding.** Solder disappears and copper pads meet directly. Applied Materials co-developed its Kinex hybrid bonding system with Besi, which

12 Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. LSEG StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 July 2026 [\[A\]](https://investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897a...)

13 Intel Opens Fab 9 in New Mexico. Intel [\[A\]](https://intel.com/content/www/us/en/newsroom/news/intel-opens-fab-9-new-mexico.html)

14 ASE Technology Holding Co., Ltd. Reports Its Unaudited Consolidated Financial Results for the Fourth Quarter and the Full Year of 2025. PR Newswire · 5 February 2026 [\[A\]](https://prnewswire.com/news-releases/ase-technology-holding-co-ltd-reports-its-unaudited-consolida...)

15 AMKOR TECHNOLOGY, INC., Form 8-K current report for the period ended 2026-02-09 (8-K). U.S. Securities and Exchange Commission (filing by AMKOR TECHNOLOGY, INC.) · 9 February 2026 [\[A\]](https://sec.gov/Archives/edgar/data/1047127/000104712726000007/amkr123125erex-991.htm)

16 ASMPT Announces 2025 Annual Results AI-Driven Structural Growth Underpins Group Performance. ASMPT · 4 March 2026 [\[A\]](https://asmpt.com/en/investor-relations/news-events/asmpt-announces-2025-annual-results)

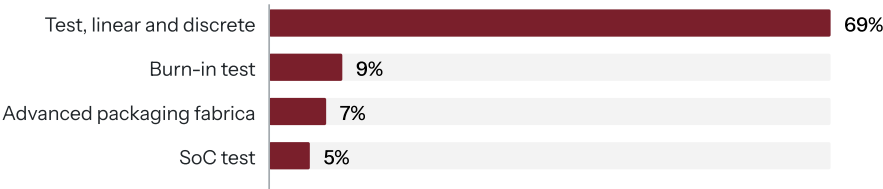
Applied calls the industry leader in hybrid bonding ¹⁷.

- **Grinding and dicing.** Disco held 87 percent of the \$1.9 billion world market for dicing tools in 2025, a category that covers the grinders that thin wafers and the saws that cut them into chips, by CSET's count from TechInsights data; see Test and assembly ¹⁸.

TSMC's Arizona commitment reached \$265 billion in July 2026 and covers two advanced packaging plants alongside 10 fabs ¹⁹. Amkor started building a \$7 billion campus in Peoria in October 2025 and expects production from early 2028 ²⁰. The Commerce Department awarded Amkor up to \$407 million in CHIPS Act funding for the site in December 2024 ²¹. In October 2025 Wei said a large outsourced packaging partner already breaking ground in Arizona was on an earlier schedule than TSMC's own two packaging fabs there ¹¹.

The chokepoint

China-based suppliers' share of selected tool segments, 2024 %



Source: CSET, Inside Beijing's Chipmaking Offensive

JCET, a leading Chinese assembler, billed a record RMB 38.87 billion in 2025, up 8.1 percent ²³. Between 2019 and 2024, Chinese firms gained 5 percentage points of share in test tools and 4 points in fabrication tools built for advanced packaging, but lost share in bonding and other conventional assembly and packaging tools, the category where CSET counts hybrid and thermocompression bonders ²². Within those advanced packaging fabrication tools, China gained 10 points in etch and clean tools and 3 points in deposition tools, and lost 2 points each in

17 Applied Materials, Kinex integrated die-to-wafer hybrid bonding system product page. Applied Materials ^A
appliedmaterials.com/eu/en/product-library/kinex-integrated-die-to-wafer-hybrid-bonding-sy...

18 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) ^A chipexplorer.eto.tech

19 TSMC Announces Additional \$100 Billion Investment in Arizona. Arizona Commerce Authority · 16 July 2026 ^A
azcommerce.com/news-events/news/2026/7/tsmc-announcement

20 Amkor Technology Breaks Ground on New Semiconductor Advanced Packaging and Test Campus in Arizona; Expands Investment to \$7 Billion. Amkor Technology ^A ir.amkor.com/news-releases/news-release-details/amkor-technology-breaks-ground-new-semicon...

21 AMKOR TECHNOLOGY, INC., Form 10-K annual report for the period ended 2025-12-31 (10-K). U.S. Securities and Exchange Commission (filing by AMKOR TECHNOLOGY, INC.) · 20 February 2026 ^A
sec.gov/Archives/edgar/data/1047127/000104712726000014/amkr-20251231.htm

11 Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) – edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 October 2025 ^A
investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2025-10/6860312f04fd291d0f26b...

23 News detail (JCET Group website). JCET Group ^A jcetglobal.com/en/site/news-detail

22 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology (CSET) · 14 July 2025 ^A
cset.georgetown.edu/article/inside-beijings-chipmaking-offensive

lithography and CMP tools ²². In 2024 China held 7 percent of advanced packaging fabrication tools, against 65 percent for the United States and 15 percent for Japan ²². Four of the top ten outsourced assembly and test firms by 2024 revenue are headquartered in China ²². JCET says its XDFOI platform has entered high-volume manufacturing with redistribution-layer interposer, silicon interposer and silicon bridge options ²⁴.

Each generation on TSMC's roadmap needs a larger interposer.

- **2028.** A 14-reticle interposer carrying about ten large compute dies and 20 HBM stacks, roughly 12,000 mm² of interposer, about the area of a compact disc ⁹.
- **2029.** More than 14 reticles, and a 40-reticle System-on-Wafer beside it ⁹.

Key evaluation criteria

- **Interposer area** is the limit on how much logic and memory fit, now 5.5x reticle on CoWoS-L ⁹.
- **Package yield** decides whether a generation ships on time, and nobody publishes it.
- **Warpage control** covers the expansion mismatch between die, bridge, interposer and substrate that caused warpage in Blackwell, the first high-volume CoWoS-L design ⁸.
- **HBM stacks supported** is about 20 on the 14-reticle package due in 2028 ⁹.
- **Bonder throughput** depends on the toolmakers, and ASMPT alone targets 35 to 40 percent of the thermocompression bonding market ¹⁶.
- **Substrate size** limits everything above it. A 14-reticle interposer needs a resin substrate that will not warp under it, which pushes ABF build-up film to its limits; see Substrates and PCBs.

FOUR THINGS TO REMEMBER

- Many leading accelerators, Blackwell among them, need more logic than one chip can hold, so packaging joins

²² Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology (CSET) · 14 July 2025 ^[A]
 cset.georgetown.edu/article/inside-beijings-chipmaking-offensive

²⁴ News detail (JCET Group website). JCET Group ^[A] jcetglobal.com/en/site/news-detail

⁹ TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC · 23 April 2026 ^[A]
 pr.tsmc.com/english/news/3302

⁸ Nvidia's Blackwell Reworked - Shipment Delays & GB200A Reworked Platforms. SemiAnalysis · 4 August 2024 ^[B]
 semianalysis.com/2024/08/04/nvidias-blackwell-reworked-shipment

¹⁶ ASMPT Announces 2025 Annual Results AI-Driven Structural Growth Underpins Group Performance. ASMPT · 4 March 2026
^[A] asmpt.com/en/investor-relations/news-events/asmpt-announces-2025-annual-results

several chips and their memory.

- TSMC packages nearly every AI accelerator, in Taiwan.
- Packaging was one of the main limits on AI chip output in 2025, and in July 2026 TSMC said its packaging capacity was still so tight that it limited customers' growth.
- No US site yet packages Nvidia-class accelerators with HBM on CoWoS, though Intel makes its own Foveros 3D packages in volume in New Mexico.

Substrates and PCBs

A Japanese food company told investors in June 2026 that it holds over 95 percent of the market for the insulating film inside high-end chip packages, and a Japanese textile company claims an overwhelming lead in the low-expansion glass cloth beneath it.

IN PLAIN TERMS

A package substrate is the adapter between a chip and the circuit board under it. The chip's connections come out finer than a human hair; the board is wired in millimeters. The substrate is built up like plywood. A stiff core of glass cloth and resin sits in the middle. Thin sheets of epoxy film are pressed onto both faces, a laser burns holes through each sheet, and copper is plated into the holes to carry signals from one layer to the next. Every added layer is another set of holes that can fail. A handful of firms build these substrates, one Japanese company dominates the film, and another dominates the low-expansion glass cloth in the core.

IN SHORT

Ajinomoto, a Japanese food company, makes the insulating film that separates the wiring layers inside high-end chip packages, and told investors in June 2026 that its share of that market has stayed above 95 percent since launch ². Nitto Boseki, another Japanese company, makes T-glass, a glass cloth essential for dense package substrates, and says it holds an overwhelming advantage in quality and production capacity for this kind of glass ⁴. It also says Chinese and Taiwanese companies are aggressively catching up with it in the special glass sector ⁴.

² Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto · 30 June 2026 [\[A\]](https://ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList...)
ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList...

⁴ 2-4-1, Kojimachi, Chiyoda-ku, Tokyo, 102-8489, Japan. Nitto Boseki (Nittobo) · 16 September 2025 [\[A\]](https://nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf)
nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf

CHOKEPOINT CARD		EXTREME CONCENTRATION	HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY		PRICE OR MARKET SIZE
Extreme	Hard		Ibiden alone is spending about JPY 500 billion on high-performance substrate capacity from fiscal 2026 to 2028, about JPY 220 billion of it in the first phase
WHO LEADS		JP Ajinomoto Told investors in June 2026 that its build-up film has held over 95% of its market since launch JP Nitto Boseki Claims an overwhelming advantage in low thermal expansion glass JP Ibiden Says it typically takes close to 100% of each new generation of interposer-type substrates at launch, which may fall by 20 to 30% after about three to six months TW Unimicron Build-up substrates were 52% of sales in Q2 2026 KR Samsung Electro-Mechanics Package solution sales KRW 771.6bn in Q2 2026, up 37%	
WHERE IT IS MADE		JP Japan Build-up film, low-expansion glass cloth, Ibiden and Shinko substrate plants in Gifu and Nagano, and a plant in Chiba that Shinko agreed to buy in September 2026 TW Taiwan Unimicron, Nan Ya PCB, Kinsus; substrate makers selling to outside customers KR South Korea Samsung Electro-Mechanics, LG Innotek, and a planned glass-core joint venture with Sumitomo Chemical's Dongwoo Fine-Chem CN China With Taiwan, home to most of TTM's circuit board competitors; now pushing into special glass cloth AT Austria AT&S, which says it is the only company in Europe able to develop and produce IC substrates locally	
WHY SUBSTITUTION IS SLOW		A few firms build substrates. Money can expand their plants. The weakest points are the materials inside the substrate. Ajinomoto makes the thin insulating film between the substrate's wiring layers and has been the standard since 1999. It told investors in June 2026 that the film has held a share of over 95 percent since its launch. Beneath that film is Nitto Boseki's glass cloth, made from a glass that expands little with heat. A newcomer can build a line to make a rival film. That film would then have to be approved by every substrate maker and chip customer, in each layer of each product.	
WHERE CHINA STANDS		TTM, an American circuit board maker, says its circuit board competitors are mostly based in China and Taiwan. Nitto Boseki says Chinese and Taiwanese companies are aggressively catching up	

with it in the special glass sector. Ajinomoto, which is Japanese, told investors in June 2026 that its build-up film has held a share of over 95 percent since launch.	WHERE THE US STANDS The White House's 2021 supply chain review listed no American firm among the key substrate makers, and a May 2024 report by the Semiconductor Industry Association and Boston Consulting Group counted none among the major package substrate vendors. Since 2021 the Commerce Department has made a final award of up to \$75 million to Absolics, a subsidiary of Korea's SKC, for a glass substrate plant in Covington, Georgia, and as of October 2026 NIST's project page expected its production capacity to come online in 2027. TTM Technologies, an American circuit board maker, calls itself one of the largest technology manufacturers in North America and says it offers IC substrates. Data center computing was 24 percent of its sales in 2025, up from 14 percent in 2023. Intel said in 2023 that it planned glass substrates for the latter part of this decade.
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On TSMC's July 2026 earnings call, chief executive C.C. Wei said packaging capacity is now so tight that it limits customers' growth ¹. The silicon interposer wires chips together inside a package. Past its edge the wiring turns to epoxy and glass: a build-up substrate, a printed circuit board of thirty layers, then a rack.

How it works

The substrate maker drills the core and plates it with copper before the build-up starts. Each cycle then presses on a film of epoxy, burns holes through it with a laser to connect the layers, and adds copper wiring on top ². Each film is about 10 micrometers thick, and a human hair is about 80 micrometers across ³.

Silicon and epoxy swell at different rates when heated, so the larger the package, the more it warps. Ajinomoto counts 22 layers of its film in a 2026 AI package substrate about 100 mm square, against 18 on a high-performance computing substrate about 70 mm square around 2023, and six when PCs first adopted it in 1999 ². Nitto Boseki says its low-expansion T-glass cloth has been highly evaluated

1 Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. LSEG StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 July 2026 [A](https://investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897a...)

2 Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto · 30 June 2026 [A](https://ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList...)

3 The Ajinomoto Group’s Unexpected Role in Semiconductor Manufacturing: The Insulating Film “ABF” Born from “AminoScience” | Stories. Ajinomoto · 5 March 2026 [A](https://ajinomoto.com/stories/the-ajinomoto-groups-unexpected-role-in-semiconductor-manufacturing-...)

as an effective solution to that warping, and its adoption in substrates has increased significantly ⁴.

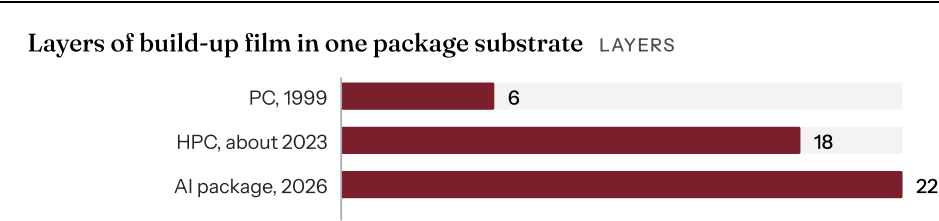
Variants and trade-offs

BT substrates

Bismaleimide-triazine laminate, or BT, is the other main family. Mitsubishi Gas Chemical, which makes BT materials, says they go mostly into thin packages for smartphone processors, radio modules and memory ⁵. The company also lists flip-chip substrates for computer CPUs and GPUs among BT's uses, where its laminate forms the core between layers of build-up film ⁵. In an October 2024 investor presentation, it estimated that its BT resins held about 40 percent of the substrate materials market ⁵.

ABF build-up substrates

Ajinomoto Build-up Film, or ABF, is the insulating film between the layers of package substrates for logic chips, used in PCs, network equipment, servers and AI equipment ². Ajinomoto first developed it in 1999, and says major chipmakers have used it as the de facto standard ever since ⁶. Asked on the company's own site whether its share was nearer 30 or 50 percent, the electronic materials division answered: "More like 95 percent market share", and said practically all high-performance computers and servers rely on it ³. In June 2026 Ajinomoto told investors that the film has held a share of over 95 percent since its launch ².



Source: Ajinomoto, Growth Strategy for the Electronic Materials Business, June 2026

Glass core substrates

A glass core in place of resin expands less with heat and stays flatter, which is why chipmakers and substrate makers are both trying it ⁷.

4 2-4-1, Kojimachi, Chiyoda-ku, Tokyo, 102-8489, Japan. Nitto Boseki (Nittobo) · 16 September 2025 [A](https://nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf)
nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf

5 2410022e. Mitsubishi Gas Chemical · 10 January 2025 [A](https://mgc.co.jp/eng/ir/files/2410022e.pdf)
mgc.co.jp/eng/ir/files/2410022e.pdf

2 Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto · 30 June 2026 [A](https://ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList...)
ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList...

6 Ajinomoto, Business Briefing: ABF-Based Growth Strategy in ICT, 12 June 2023. Ajinomoto · 12 June 2023 [A](https://ajinomoto.co.jp/company/en/ir/event/business_briefing/main/01113/teaserItems1/01/linkList/...)
ajinomoto.co.jp/company/en/ir/event/business_briefing/main/01113/teaserItems1/01/linkList/...

3 The Ajinomoto Group's Unexpected Role in Semiconductor Manufacturing: The Insulating Film "ABF" Born from "AminoScience" | Stories. Ajinomoto · 5 March 2026 [A](https://ajinomoto.com/stories/the-ajinomoto-groups-unexpected-role-in-semiconductor-manufacturing-...)
ajinomoto.com/stories/the-ajinomoto-groups-unexpected-role-in-semiconductor-manufacturing-...

7 Samsung Electro-Mechanics Signs MOU with Sumitomo Chemical Group to Establish a Joint Venture for Glass Core Used in Package Substrates. Samsung Electro-Mechanics · 5 November 2025 [A](https://samsungsem.com/global/newsroom/news/view.do)
samsungsem.com/global/newsroom/news/view.do

- **Absolics**, a subsidiary of Korea's SKC, has a final Commerce Department award of up to \$75 million for a 120,000-square-foot glass substrate plant in Covington, Georgia, and as of October 2026 NIST's project page expected first deliveries to customers in 2025 and production capacity to come online in 2027 ⁸.
- **Intel** announced glass substrates in September 2023 for the latter part of this decade ⁹.
- **Samsung Electro-Mechanics** signed a joint venture agreement with Sumitomo Chemical's subsidiary Dongwoo Fine-Chem in July 2026 to make glass core substrates, with a supply system planned by the second half of fiscal 2027 ¹⁰.

All three timelines reach into the later years of this decade.

The materials underneath

Ajinomoto's film is a small line in a food company's accounts and a chokepoint for high-end chip packages. The Healthcare and Others segment that carries electronic materials lifted business profit 45.1 percent to JPY 66.2 billion in the year to March 2026, which Ajinomoto attributes mainly to higher electronic materials revenue and higher profit in Bio-Pharma Services & Ingredients ¹¹. Ajinomoto has set an investment budget of JPY 25 billion between 2023 and 2030 to expand production, and says there are no concerns about its current supply chain overall ². In May 2026 it announced the acquisition of land in Gifu Prefecture for a third production site, scheduled to start operating in 2032 to meet demand after 2030 ².

The core one layer down also has a dominant supplier. Nitto Boseki's T-glass is stiff and expands little when heated, and the company calls it essential for making high-density package substrates ⁴. Laminate makers such as Mitsubishi Gas Chemical coat the glass cloth with resin and press it with copper foil into the core laminate that substrate makers build on ⁵. Nitto Boseki claims an overwhelming advantage in quality and capacity for low-expansion glass, says market demand seems to have risen about two to three times since its fiscal 2024 to 2027 plan was set, and planned about JPY 80 billion of capital spending over those four years ⁴. In August 2025 it decided to expand glass fiber cloth production at its Fukushima Enterprise Center, with production scheduled to begin in the fourth quarter of its

⁸ Absolics (Georgia). NIST · 5 July 2024 [\[A\]](https://www.nist.gov/chips/absolics-georgia-covington) [nist.gov/chips/absolics-georgia-covington](https://www.nist.gov/chips/absolics-georgia-covington)

⁹ Intel Unveils Industry-Leading Glass Substrates to Meet Demand for.... Intel · 31 January 2025 [\[A\]](https://www.intel.com/newsroom/archive/2025/en-us-2023-09-18-intel-unveils-industry-leading-gl...) [download.intel.com/newsroom/archive/2025/en-us-2023-09-18-intel-unveils-industry-leading-gl...](https://www.intel.com/newsroom/archive/2025/en-us-2023-09-18-intel-unveils-industry-leading-gl...)

¹⁰ Sumitomo Chemical Subsidiary to Establish of a Joint Venture with Samsung Electro-Mechanics for the Glass Core Substrate BusinessJointly Promoting the Next-Generation Core Substrate Business for Advanced Semiconductor Packages | Business & Products. Sumitomo Chemical [\[A\]](https://www.sumitomo-chem.co.jp/english/news/detail/20260702e_2.html) [sumitomo-chem.co.jp/english/news/detail/20260702e_2.html](https://www.sumitomo-chem.co.jp/english/news/detail/20260702e_2.html)

¹¹ Note: This document has been translated from the Japanese original for reference purposes only. In the event of any. Ajinomoto · 1 May 2026 [\[A\]](https://www.ajinomoto.co.jp/company/en/ir/library/result/main/014/teaserItems1/0/linkList/06/link/FY25...) [ajinomoto.co.jp/company/en/ir/library/result/main/014/teaserItems1/0/linkList/06/link/FY25...](https://www.ajinomoto.co.jp/company/en/ir/library/result/main/014/teaserItems1/0/linkList/06/link/FY25...)

² Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto · 30 June 2026 [\[A\]](https://www.ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList...) [ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList...](https://www.ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList...)

⁴ 2-4-1, Kojimachi, Chiyoda-ku, Tokyo, 102-8489, Japan. Nitto Boseki (Nittobo) · 16 September 2025 [\[A\]](https://www.nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf) [nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf](https://www.nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf)

⁵ 2410022e. Mitsubishi Gas Chemical · 10 January 2025 [\[A\]](https://www.mgc.co.jp/eng/ir/files/2410022e.pdf) [mgc.co.jp/eng/ir/files/2410022e.pdf](https://www.mgc.co.jp/eng/ir/files/2410022e.pdf)

fiscal 2026 ⁴. Apple and Qualcomm are among the customers worried about Japanese glass cloth supply ¹².

Chinese firms are entering this layer, and Nitto Boseki says Chinese and Taiwanese companies are aggressively catching up with it in the special glass sector ⁴. At stake is a chip materials market Nikkei sizes at \$73 billion ¹³.

Who makes it

The plants that build substrates for other firms are an Asian oligopoly. The White House's 2021 hundred-day supply chain review recorded build-up substrate among the materials commenters called vulnerable, and named key substrate makers including Ibiden, Nanya, Shinko, Samsung, Unimicron, Shennan Circuits, Zhuhai Yueya and AKM. None of the eight is American ¹⁴. A May 2024 report by the Semiconductor Industry Association and Boston Consulting Group counted the major vendors of package substrates by headquarters and found two in Japan, two in Taiwan, one in mainland China and none in the United States ¹⁵. TTM Technologies, an American circuit board maker, says it also offers IC substrates ¹⁶.

- **Ibiden** will invest about JPY 500 billion from fiscal 2026 to fiscal 2028, starting with about JPY 220 billion, mainly at its Gama plant, and planned mass production from fiscal 2027 ¹⁷. In May 2026 management said it typically takes close to 100 percent of a new generation of interposer-type substrates at launch, and that this share may decline by 20 to 30 percent after about three to six months ¹⁸. On silicon-bridge substrates, it said, wiring the underside is hard enough that it expects to keep its technical lead at least through fiscal 2030 ¹⁸.

4 2-4-1, Kojimachi, Chiyoda-ku, Tokyo, 102-8489, Japan. Nitto Boseki (Nittobo) · 16 September 2025 [\[A\]](#)
nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf

12 Apple and Qualcomm fret over strained supplies of Japan's glass cloth. Nikkei Asia · 14 January 2026 [\[B\]](#)
asia.nikkei.com/business/technology/tech-asia/apple-and-qualcomm-fret-over-strained-suppli...

13 China chip material makers battle Japan rivals for \$73bn market. Nikkei Asia · 1 July 2026 [\[B\]](#)
asia.nikkei.com/business/tech/semiconductors/china-chip-material-makers-battle-japan-rival...

14 BUILDING RESILIENT SUPPLY CHAINS,. The White House (Biden administration archive) · 7 June 2021 [\[A\]](#)
bidenwhitehouse.archives.gov/wp-content/uploads/2021/06/100-day-supply-chain-review-report...

15 R AJ VA RA DA RA JA N / I ACOB KOCH -W E SE R / CH RI S RI CH A RD / JOSE P H FI TZ GE RA L D /. Semiconductor Industry Association · 9 May 2024 [\[A\]](#) semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconduc...

16 TTM TECHNOLOGIES INC, Form 10-K annual report for the period ended 2025-12-29 (10-K). U.S. Securities and Exchange Commission (filing by TTM TECHNOLOGIES INC) · 17 February 2026 [\[A\]](#)
sec.gov/Archives/edgar/data/1116942/000119312526051976/ttmi-20251229.htm

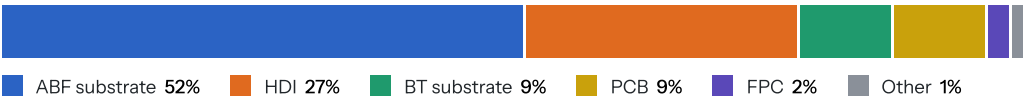
17 Ibiden, Notice Regarding Capital Investment Plan for High-Performance IC Package Substrates. Ibiden · 3 February 2026 [\[A\]](#)
ibiden.com/company/2026/02/notice-regarding-capital-investment-plan-for-high-performance-i...

18 Ibiden, questions and answers from the financial presentation for the year ended 31 March 2026. Ibiden · 12 May 2026 [\[A\]](#)
ibiden.com/ir/items/en_QA_FY25Q4.pdf

- **Unimicron** took NT\$42.9 billion of sales in the second quarter of 2026, 52 percent of it build-up substrates and 61 percent of it AI data center work ¹⁹.
- **Samsung Electro-Mechanics** grew package solution sales 37 percent year on year to KRW 771.6 billion in the second quarter of 2026, on substrates for AI accelerators, server processors and cars ²⁰.

A company owned mainly by funds of JIC Capital, a subsidiary of Japan Investment Corporation, launched a tender offer for Shinko's other shares in February 2025 as part of a deal to take it private, and Fujitsu agreed to sell its 50.02 percent stake back to Shinko ²¹. The tender offer succeeded in March 2025 ²². In September 2026 Shinko agreed to buy a plant in Mobara, Chiba Prefecture, from Japan Display, a display maker, and said it would make the site a new core plant for advanced chip packages while also expanding capacity at its plants in Nagano ²³. Production there is scheduled to start in fiscal 2028 ²³.

Unimicron sales by technology, second quarter 2026 %



Source: Unimicron 2026 Q2 earnings conference

The boards under the GPU

TTM Technologies says it regularly builds printed circuit boards of more than 30 layers and can go past 70 ¹⁶. Those layers carry power to the GPUs and route fast signals between them, so how much signal the laminate absorbs becomes a main design constraint. Nitto Boseki also makes NE-glass, a low-dielectric glass cloth that absorbs less signal, used in switches and routers in data centers ⁴.

19 Unimicron consolidated financial statements, second quarter 2026. Unimicron Technology ^A
unimicron.com/files/money/Earnings/en/2026-Q2-consolidated-en.pdf

20 Samsung Electro-Mechanics, Q2 2026 business results. Samsung Electro-Mechanics · 30 July 2026 ^A
m.samsungsem.com/global/newsroom/news/view.do

21 February 17, 2025 Japan Investment Corporation. Japan Investment Corporation · 17 February 2025 ^A
jiccapital.co.jp/en/news/assets/E_20250217_JIC_JICC_PressRelease.pdf

22 (Progress Report on Disclosed Matters) Notice Regarding Completion of JICC-04's Tender Offer for Shares of a Consolidated Subsidiary of Fujitsu Limited (SHINKO ELECTRIC INDUSTRIES CO., LTD.). Fujitsu · 19 March 2025 ^A
pr.fujitsu.com/jp/news/2025/03/en/19-1.pdf

23 Notice Concerning the Acquisition of Japan Display Inc.'s Mobara Fab. Shinko Electric Industries · 30 September 2026 ^A
shinko.co.jp/english/news/docs/20260930-01_en.pdf

16 TTM TECHNOLOGIES INC, Form 10-K annual report for the period ended 2025-12-29 (10-K). U.S. Securities and Exchange Commission (filing by TTM TECHNOLOGIES INC) · 17 February 2026 ^A
sec.gov/Archives/edgar/data/1116942/000119312526051976/ttmi-20251229.htm

4 2-4-1, Kojimachi, Chiyoda-ku, Tokyo, 102-8489, Japan. Nitto Boseki (Nittobo) · 16 September 2025 ^A
nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf

Data center computing was 24 percent of TTM's \$2.91 billion of fiscal 2025 revenue, against 14 percent two years earlier ¹⁶. It says its circuit board competitors are mostly based in China and Taiwan ¹⁶. In its annual report for 2025, TTM said it was building a plant in Syracuse, New York, to make ultra-high-density circuit boards for national security needs, with volume production expected in the second half of 2026 ¹⁶. Thailand aims to be the biggest circuit board hub outside China as makers race to diversify production ²⁴.

The chokepoint

Money can expand an oligopoly of substrate plants, and it is being spent. The weakest points are one layer down, where one Japanese company dominates the film and another dominates the low-expansion glass cloth in the core. Both are adding capacity on plans that run for years.

Packages lose flatness as they grow. TSMC has told investors that its CoWoS packaging roadmap goes beyond 14 times the area a lithography machine can print in one shot ¹. Bigger bodies mean more warping, more layers, more holes that can break the circuit, and lower yield on a part that is already expensive before a die touches it.

Key evaluation criteria

- **Layer count** sets how much current and how many signals the substrate can carry. Each added layer is another chance to lose the part.
- **Body size** drives everything else. Once a body is much larger than the dies it carries, warping and handling take over from the wiring in deciding what can be built.
- **Coefficient of thermal expansion**, how much a material swells when heated, must be close enough to silicon that the package survives repeated heating and cooling, which is what T-glass provides and why its supply matters.
- **Dielectric properties**, how much signal the core laminate absorbs, set the speeds the substrate and the board underneath can run.
- **Qualification time** protects the incumbents. A second supplier's film or laminate has to be approved by each substrate maker and chip customer before it can be used.

¹⁶ TTM TECHNOLOGIES INC, Form 10-K annual report for the period ended 2025-12-29 (10-K). U.S. Securities and Exchange Commission (filing by TTM TECHNOLOGIES INC) · 17 February 2026 [\[A\]](https://sec.gov/Archives/edgar/data/1116942/000119312526051976/ttmi-20251229.htm)
sec.gov/Archives/edgar/data/1116942/000119312526051976/ttmi-20251229.htm

²⁴ Thailand carves out a less-glamorous AI niche: printed circuit boards. Nikkei Asia · 3 September 2025 [\[B\]](https://asia.nikkei.com/business/technology/tech-asia/thailand-carves-out-a-less-glamorous-ai-nich...)
asia.nikkei.com/business/technology/tech-asia/thailand-carves-out-a-less-glamorous-ai-nich...

¹ Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. LSEG StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 July 2026 [\[A\]](https://investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897a...)
investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897a...

FOUR THINGS TO REMEMBER

- A package substrate connects a chip's fine connections to a circuit board wired in millimeters.
- A Japanese supplier leads the film, and another leads the glass cloth inside it.
- Replacing the film would mean re-approval by every substrate maker and chip customer.
- The White House's 2021 supply chain review named no American firm among the key substrate makers, and the glass substrate plant Absolics is building in Georgia expects production capacity in 2027.

Test and Assembly

Assembly and test decide which dies are allowed into an expensive package. One Japanese firm took about 65 percent of 2025 spending on chip testers, by its own estimate.

IN PLAIN TERMS

Before a chip can be sold, a machine has to put questions to it and check every answer. While the chips are still on the wafer, thousands of needles press onto small metal pads on each one, send in signals and read what comes back; the tester marks any chip that answers wrong, and that chip goes no further. A modern accelerator glues together a dozen expensive pieces, and one bad piece throws away all of them. So the industry tests sooner, hotter and longer than it used to, to make a weak chip fail on the test bench before it reaches a finished product, and two firms, one Japanese and one American, sell most of the machines that do it.

IN SHORT

Advantest, a Japanese company, estimates that it took about 65 percent of 2025 spending on chip testers, as demand for testing AI chips grew ⁹. Customers are cautious about switching tester suppliers, because a switch means rebuilding their development, evaluation and production testing ³⁶. Four of the ten largest companies that assemble and test chips for others, ranked by 2024 revenue, are based in China ²⁶.

9 Advantest, presentation notes for the FY2025 (year ended 31 March 2026) results briefing, 27 April 2026. Advantest · 27 April 2026 [\[A\]](https://advantest.com/document/en/investors/ir-library/result/JE_BIZ_260427_note.pdf) advantest.com/document/en/investors/ir-library/result/JE_BIZ_260427_note.pdf

36 Investors Guide April 25, 2025. Advantest · 13 May 2025 [\[A\]](https://advantest.com/document/en/investors/ir-library/investors-guide/Investors_Guide_2504E.pdf) advantest.com/document/en/investors/ir-library/investors-guide/Investors_Guide_2504E.pdf

26 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology (CSET) · 14 July 2025 [\[A\]](https://cset.georgetown.edu/article/inside-beijings-chipmaking-offensive) cset.georgetown.edu/article/inside-beijings-chipmaking-offensive

CHOKEPOINT CARD		HIGH CONCENTRATION
		MODERATELY HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY	PRICE OR MARKET SIZE
High	Moderate No test or assembly tool has only one maker, but switching testers means rebuilding the customer's whole test setup.	ASE's packaging and test business (about \$12.1 billion) and Amkor (\$6.71 billion) took about \$18.8 billion in 2025 ASE spent \$4.1 billion on machinery, buildings, facilities and automation in the first half of 2026
WHO LEADS	JP Advantest About 65% of the tester market in 2025, by its own estimate US Teradyne Second in testers; \$2.52bn of semiconductor test revenue in 2025, including system-level testers and service TW ASE \$20.6bn of 2025 revenue, about 59 percent from packaging and test and 40 percent from electronics manufacturing; the largest assembly and test contractor US Amkor \$6.71bn of 2025 revenue JP Disco 87% of the \$1.9bn market for dicing saws and wafer grinders in 2025, on CSET's analysis of TechInsights data	
WHERE IT IS MADE	TW Taiwan ASE, Powertech, KYEC and ChipMOS; the largest assembly and test cluster JP Japan Advantest testers, Accretech and Tokyo Electron probers, Disco and Accretech dicing and grinding, Micronics Japan probe cards US United States Teradyne, FormFactor, Cohu, Aehr; Amkor's Arizona packaging plant CN China Four of the top ten assembly and test firms by 2024 revenue are China-headquartered MY Malaysia Penang and Kulim; Malaysia said in July 2026 that it ships 13% of the world's packaged chips	
WHY SUBSTITUTION IS POSSIBLE	Advantest and Teradyne sell most of the testers between them, but both make machines that customers have approved, and the smaller kinds of test and assembly tool have several makers each. Customers are highly cautious about switching, because a new tester means rebuilding their whole setup for development, evaluation and volume production. Advantest tells its investors the same thing. A newcomer pays that cost once and takes two to five years. Four of the top ten outsourced assembly and test firms by 2024 revenue are based in China.	
WHERE CHINA STANDS		
Between 2019 and 2024, according to CSET at Georgetown, Chinese toolmakers gained 5 percentage points of share in test tools and 4 points in fabrication tools built for advanced packaging, but lost		

share in bonding and other conventional assembly and packaging tools. They still lag significantly behind foreign suppliers. CSET counts four of the top ten assembly and test firms by 2024 revenue as China-headquartered.	WHERE THE US STANDS American firms are strong in test machines and probe cards, the beds of pins that touch each chip on the wafer: Teradyne, FormFactor, Cohu and AeHR. They are weak in assembly. Amkor is building a \$7 billion packaging and test campus in Arizona and has a long-term deal to run packaging and test there for TSMC.
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Turning silicon into a finished, packaged chip takes 1,000 to 1,500 steps, depending on how complex the chip is, the Semiconductor Industry Association estimated in 2025 ¹. Advantest's investor guide of July 2026 counts test as the only step that puts electrical signals through the chip ². Every stage so far makes dies; the back end of the industry, assembly and test, decides which of them are allowed into a package.

How it works

Each round of test catches failures the round before it cannot see.

- **Wafer sort.** Thousands of needles land on each die while it is still on the wafer, a tester drives patterns in and checks the answers, and the failures go no further.
- **Burn-in.** Run the part hot and at raised voltage for minutes to days, on the wafer or in the package, so anything that would fail early fails in the factory ³.
- **Final test.** The tester runs the packaged part again, because packaging adds failures of its own.
- **System-level test.** The finished part sits in a socket and runs something close to a real workload, because some failures appear only when everything runs at once.

Proving a die good before it is packaged matters more as packages hold more valuable parts ⁴. AeHR's wafer-level burn-in systems look for early-life and hidden failures before dies are cut from the wafer, which lowers the risk of committing high-bandwidth memory and an expensive substrate to a processor that may later fail ⁴. AeHR's lead AI customer is shifting burn-in for its AI accelerators from the

1 Testimony of David Isaacs, Vice President of Government Affairs. Senate · 12 May 2025 [\[A\]](https://www.finance.senate.gov/download/051425-isaacs-testimony&download=1) [finance.senate.gov/download/051425-isaacs-testimony&download=1](https://www.finance.senate.gov/download/051425-isaacs-testimony&download=1)

2 Investors Guide July 29, 2026. Advantest · 30 July 2026 [\[A\]](https://www.advantest.com/document/en/investors/ir-library/investors-guide/Investors_Guide_2607E.pdf) [advantest.com/document/en/investors/ir-library/investors-guide/Investors_Guide_2607E.pdf](https://www.advantest.com/document/en/investors/ir-library/investors-guide/Investors_Guide_2607E.pdf)

3 AEHR TEST SYSTEMS, Form 10-K annual report for the period ended 2026-05-29. U.S. Securities and Exchange Commission (filing by AEHR TEST SYSTEMS) · 27 July 2026 [\[A\]](https://www.sec.gov/Archives/edgar/data/1040470/000165495426006919/aeHR_10k.htm) [sec.gov/Archives/edgar/data/1040470/000165495426006919/aeHR_10k.htm](https://www.sec.gov/Archives/edgar/data/1040470/000165495426006919/aeHR_10k.htm)

4 AeHR Receives \$22 Million Follow-On Order for AI Processor Wafer-Level Burn-In Systems. AeHR Test Systems · 12 August 2026 [\[A\]](https://www.aehr.com/2026/08/aeHR-receives-22-million-follow-on-order-for-ai-processor-wafer-level-bur...) [aehr.com/2026/08/aeHR-receives-22-million-follow-on-order-for-ai-processor-wafer-level-bur...](https://www.aehr.com/2026/08/aeHR-receives-22-million-follow-on-order-for-ai-processor-wafer-level-bur...)

finished system to the wafer ⁵. The FOX-XP systems that customer ordered from AeHR in August 2026 each burn in nine 300 mm wafers at a time ⁴.

Variants and trade-offs

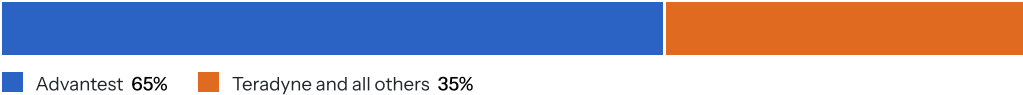
Wafer sort and known-good die

The probe card that holds those needles is the hard part. FormFactor says the high-frequency capability of its probe cards lets it compete favorably in testing high-bandwidth memory, a stack of eight, twelve or even sixteen memory dies ⁶. For a large logic die every needle must sit in the same plane, survive repeated touchdowns without drifting, and do it hot. Cards are custom to the device, so each new part means a new card and a new qualification.

Final test, burn-in and system-level test

The economics get worse as packages grow. TSMC has told investors that its CoWoS packaging roadmap runs beyond 14 times the area a lithography machine can print in one shot ⁷. Every added die is another chance to lose the whole assembly, along with its memory and substrate ⁴. ASE ran 6,797 testers in the second quarter of 2025 and 8,348 a year later ⁸.

Automated test equipment: share of the ~\$9.0bn tester market, 2025 %



Source: Advantest FY2025 results briefing, April 2026

Who makes it

Advantest puts its own share at about 65 percent of an estimated \$9.0 billion tester market in 2025 ⁹. Its share of system-on-chip (SoC) testers, the machines that test processors and other non-memory chips, rose about ten points in a year to 66 percent, and it held about 60 percent of memory test ⁹. Teradyne, its main rival,

5 AeHR Test Systems Reports Fiscal 2026 Fourth Quarter and Full Year Financial Results with Record Quarterly Bookings and \$100 Million Effective Backlog. AeHR Test Systems · 14 July 2026 [A] aehr.com/2026/07/aehr-test-systems-reports-fiscal-2026-fourth-quarter-and-full-year-financ...

4 AeHR Receives \$22 Million Follow-On Order for AI Processor Wafer-Level Burn-In Systems. AeHR Test Systems · 12 August 2026 [A] aehr.com/2026/08/aehr-receives-22-million-follow-on-order-for-ai-processor-wafer-level-bur...

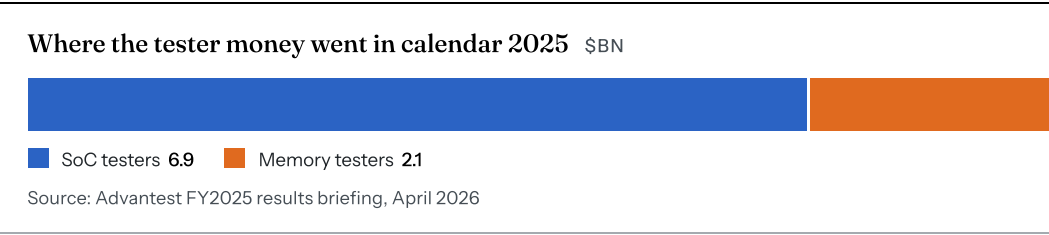
6 FORMFACTOR INC, Form 10-K annual report for the period ended 2025-12-27 (10-K). U.S. Securities and Exchange Commission (filing by FORMFACTOR INC) · 20 February 2026 [A] sec.gov/Archives/edgar/data/1039399/000103939926000009/form-20251227.htm

7 Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. LSEG StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 July 2026 [A] investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897a...

8 ASE Technology Holding Co., Ltd., Form 6-K report of foreign private issuer for the period ended 2026-07-30. U.S. Securities and Exchange Commission (filing by ASE Technology Holding Co., Ltd.) · 30 July 2026 [A] sec.gov/Archives/edgar/data/1122411/000095010326011351/dp250868_6k.htm

9 Advantest, presentation notes for the FY2025 (year ended 31 March 2026) results briefing, 27 April 2026. Advantest · 27 April 2026 [A] advantest.com/document/en/investors/ir-library/result/JE_BIZ_260427_note.pdf

took \$2.52 billion of semiconductor test revenue in 2025, service included, of which \$1.89 billion came from SoC testers and \$505 million from memory testers¹⁰. Teradyne as a whole grew 13 percent to \$3.19 billion for 2025, with fourth-quarter revenue up 44 percent on AI demand¹¹.



Below the two tester makers, the rest of the test and assembly equipment splits into niches, each with its own suppliers.

- **Probe cards.** FormFactor took \$785.0 million in fiscal 2025¹²; Technoprobe grew 15.7 percent to EUR 628.4 million, about 38 percent of it from AI, and aims to double capacity by the end of 2027¹³.
- **Probers**, the machines that move each wafer under the probe card and keep it at a set temperature. Tokyo Seimitsu, which sells as Accretech, says it has the top global share in probers and also makes dicing machines and grinders¹⁴. Tokyo Electron also makes probers¹⁵.
- **Handlers and burn-in**, the machines that feed parts into a tester and heat them. Cohu took \$453.0 million in fiscal 2025¹⁶; Aehr did \$50.0 million in fiscal 2026 but booked a record \$60.7 million in the fourth quarter alone and guides to \$130 million to \$150 million in fiscal 2027⁵.
- **Dicing and grinding.** In 2025 Disco held 87 percent and Accretech 8.1 percent of a \$1.9 billion market for the saws that cut wafers into dies and the grinders that thin them, according to CSET's analysis of TechInsights data¹⁷. In

10 TERADYNE, INC, Form 10-K annual report for the period ended 2025-12-31 (10-K). U.S. Securities and Exchange Commission (filing by TERADYNE, INC) · 19 February 2026 [\[A\]](https://sec.gov/Archives/edgar/data/97210/000119312526059002/ter-20251231.htm) sec.gov/Archives/edgar/data/97210/000119312526059002/ter-20251231.htm

11 Teradyne Reports Fourth Quarter and Full Year 2025 Results. Teradyne · 2 February 2026 [\[A\]](https://investors.teradyne.com/news-events/press-releases/detail/433/teradyne-reports-fourth-quart...) investors.teradyne.com/news-events/press-releases/detail/433/teradyne-reports-fourth-quart...

12 Revenue from Contract with Customer, Excluding Assessed Tax (us-gaap:RevenueFromContractWithCustomerExcludingAssessedTax) reported by FormFactor, Inc., XBRL company concept data. U.S. Securities and Exchange Commission (XBRL data for FormFactor, Inc.) [\[A\]](https://data.sec.gov/api/xbrl/companyconcept/CIK0001039399/us-gaap/RevenueFromContractWithCustomer...) data.sec.gov/api/xbrl/companyconcept/CIK0001039399/us-gaap/RevenueFromContractWithCustomer...

13 Technoprobe, press release: the Board of Directors approves the draft statutory and consolidated annual report as at 31 December 2025. Technoprobe · 18 March 2026 [\[A\]](https://technoprobe.com/wp-content/uploads/2026/03/PR-FY-2025_.pdf) technoprobe.com/wp-content/uploads/2026/03/PR-FY-2025_.pdf

14 INTEGRATED REPORT 2025 Tokyo Seimitsu Co., Ltd.. Accretech · 3 December 2025 [\[A\]](https://accretech.com/en/ir/index/main/00/teaserItems1/00/linkList/02/link/IntegratedReport2025_E...) accretech.com/en/ir/index/main/00/teaserItems1/00/linkList/02/link/IntegratedReport2025_E...

15 Test Precio™ Series | Products and Service(products). Tokyo Electron [\[A\]](https://tel.com/product/precio.html) tel.com/product/precio.html

16 Revenue from Contract with Customer, Including Assessed Tax (us-gaap:RevenueFromContractWithCustomerIncludingAssessedTax) reported by COHU, INC., XBRL company concept data. U.S. Securities and Exchange Commission (XBRL data for COHU, INC.) [\[A\]](https://data.sec.gov/api/xbrl/companyconcept/CIK0000021535/us-gaap/RevenueFromContractWithCustomer...) data.sec.gov/api/xbrl/companyconcept/CIK0000021535/us-gaap/RevenueFromContractWithCustomer...

5 Aehr Test Systems Reports Fiscal 2026 Fourth Quarter and Full Year Financial Results with Record Quarterly Bookings and \$100 Million Effective Backlog. Aehr Test Systems · 14 July 2026 [\[A\]](https://aehr.com/2026/07/aehr-test-systems-reports-fiscal-2026-fourth-quarter-and-full-year-financ...) aehr.com/2026/07/aehr-test-systems-reports-fiscal-2026-fourth-quarter-and-full-year-financ...

17 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) [\[A\]](https://chipexplorer.eto.tech) chipexplorer.eto.tech

December 2025 Disco announced a saw that cuts packages up to 400 by 400 mm

¹⁸.

- **Bonding.** Kulicke and Soffa did \$654.1 million in fiscal 2025 ¹⁹, while Besi's second-quarter 2026 revenue rose 68.7 percent to EUR 249.9 million on hybrid bonding and data center demand ²⁰.

Thermocompression bonders press memory dies into a stack and place chiplets on substrates. ASMPT says it remained the leader in that market in 2025 and aims for a 35 to 40 percent share ²¹. In its 2025 results it said it expects the market to reach \$1.6 billion by 2028 ²¹. It took a repeat order for fifteen chip-to-substrate bonders in December 2025 ²². Hanmi Semiconductor in Korea also sells thermocompression bonders, including dual bonders for high-bandwidth memory ²³. See Memory and HBM.

The back end's geography

Outsourced assembly and test, the OSAT business, is Taiwanese with a large Chinese challenger. ASE, the biggest, billed \$20.6 billion in 2025 ²⁴. About 59 percent of that came from packaging and test and 40 percent from its electronics manufacturing arm ²⁵. Georgetown's CSET counts four of the top ten OSATs by 2024 revenue as China-headquartered ²⁶. Malaysia's investment agency said in July 2026 that the country ships 13 percent of the world's packaged chips and wants 7 percent of advanced packaging shipments by 2035 ²⁷. A 2024 study by the Semiconductor Industry Association and Boston Consulting Group measured factory floor space at contractors and chipmakers' own plants, and gave Malaysia 7 percent of global assembly, test and packaging capacity in 2022, the largest share in Southeast Asia ²⁸.

18 DISCO develops the DFD6080 fully automatic dicing saw for work sizes up to 400 mm square (最大400mm角のパッケージ切断に対応したダイシングソー「DFD6080」を開発). DISCO Corporation · 15 December 2025 [\[A\]](https://disco.co.jp/eg/news/corp/20251215_1.html) disco.co.jp/eg/news/corp/20251215_1.html

19 Revenues (us-gaap:Revenues) reported by KULICKE AND SOFFA INDUSTRIES, INC., XBRL company concept data. U.S. Securities and Exchange Commission (XBRL data for KULICKE AND SOFFA INDUSTRIES, INC.) [\[A\]](https://data.sec.gov/api/xbrl/companyconcept/CIK0000056978/us-gaap/Revenues.json) data.sec.gov/api/xbrl/companyconcept/CIK0000056978/us-gaap/Revenues.json

20 BE Semiconductor Industries N.V. Announces Q2-26 and H1-26 Results. BE Semiconductor Industries (Besi) · 23 July 2026 [\[A\]](https://besi.com/investor-relations/press-releases/2025/details-1/be-semiconductor-industries-nv-a...) besi.com/investor-relations/press-releases/2025/details-1/be-semiconductor-industries-nv-a...

21 ASMPT Announces 2025 Annual Results AI-Driven Structural Growth Underpins Group Performance. ASMPT · 4 March 2026 [\[A\]](https://asmpt.com/en/investor-relations/news-events/asmpt-announces-2025-annual-results) asmpt.com/en/investor-relations/news-events/asmpt-announces-2025-annual-results

22 ASMPT Secures Additional Orders for Fifteen Chip-to-Substrate Thermo-Compression Bonding Tools Driven by AI Tailwind. ASMPT · 22 December 2025 [\[A\]](https://asmpt.com/en/investor-relations/news-events/asmpt-secures-additional-orders-for-fifteen-ch...) asmpt.com/en/investor-relations/news-events/asmpt-secures-additional-orders-for-fifteen-ch...

23 HANMI Semiconductor. Hanmi Semiconductor [\[A\]](https://hanmisemi.com/en/product/index.html) hanmisemi.com/en/product/index.html

24 Revenue (ifrs-full:Revenue) reported by ASE Technology Holding Co., Ltd., XBRL company concept data. U.S. Securities and Exchange Commission (XBRL data for ASE Technology Holding Co., Ltd.) [\[A\]](https://data.sec.gov/api/xbrl/companyconcept/CIK0001122411/ifrs-full/Revenue.json) data.sec.gov/api/xbrl/companyconcept/CIK0001122411/ifrs-full/Revenue.json

25 ASE Technology Holding Co., Ltd., Form 6-K report of foreign private issuer for the period ended 2026-02-05. U.S. Securities and Exchange Commission (filing by ASE Technology Holding Co., Ltd.) · 5 February 2026 [\[A\]](https://sec.gov/Archives/edgar/data/1122411/000095010326001661/dp241159_6k.htm) sec.gov/Archives/edgar/data/1122411/000095010326001661/dp241159_6k.htm

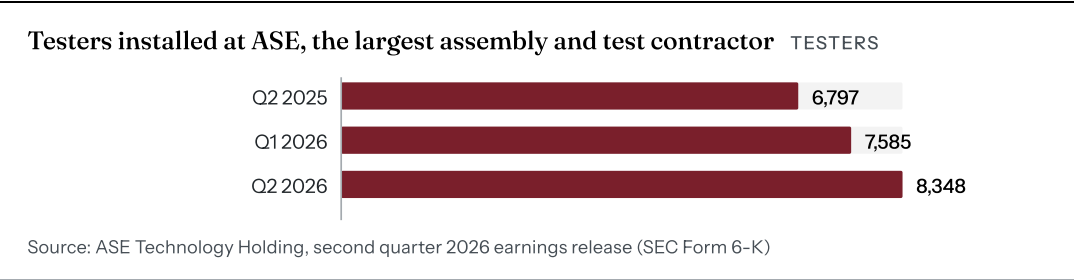
26 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology (CSET) · 14 July 2025 [\[A\]](https://cset.georgetown.edu/article/inside-beijings-chipmaking-offensive) cset.georgetown.edu/article/inside-beijings-chipmaking-offensive

27 Advanced Packaging: How Malaysia is Packaging the Future of AI. Malaysian Investment Development Authority · 1 July 2026 [\[A\]](https://mida.gov.my/advanced-packaging-how-malaysia-is-packaging-the-future-of-ai) mida.gov.my/advanced-packaging-how-malaysia-is-packaging-the-future-of-ai

28 R AJ VA RA DA RA JA N / I ACOB KOCH - W E S E R / CH RI S RI CH A RD / JOSE P H FI TZ GE RA L D /. Semiconductor Industry Association · 9 May 2024 [\[A\]](https://semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconduc...) semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconduc...

ASE spent \$2.7 billion on machinery and \$1.4 billion on buildings, facilities and automation in the first half of 2026, and says revenue from leading-edge advanced packaging is running ahead of its \$3.5 billion guidance for the year ²⁹. Powertech aims to run the first panel-level packaging line for AI chips in 2027 ³⁰.

Amkor took \$6.71 billion of revenue in 2025 ³¹, and \$1.90 billion in the second quarter of 2026 alone, up 26 percent year on year ³². It has expanded its Arizona campus to a \$7 billion investment ³³. In October 2024 TSMC and Amkor signed a memorandum of understanding under which TSMC would buy packaging and test services from Amkor's planned plant in Peoria, Arizona, to serve TSMC customers, especially those using its Phoenix fabs ³⁴. The two announced a long-term partnership in June 2026 ³⁵.



The chokepoint

Unlike lithography, no test or assembly tool has a single supplier. Advantest argues that switching tester vendor means rebuilding the whole development, evaluation and production test environment, which is why share moves slowly ³⁶.

Between 2019 and 2024, CSET finds, Chinese toolmakers gained 5 percentage points of share in test tools and 4 points in fabrication tools built for advanced

29 ASE Technology Holding Co., Ltd., Form 6-K report of foreign private issuer for the period ended 2026-07-30. U.S. Securities and Exchange Commission (filing by ASE Technology Holding Co., Ltd.) · 30 July 2026 [\[A\]](#)
sec.gov/Archives/edgar/data/1122411/000095010326011353/dp250875_6k.htm

30 Powertech eyes world's first panel-level packaging for AI chips in 2027. Nikkei Asia · 27 August 2026 [\[B\]](#)
asia.nikkei.com/business/tech/semiconductors/powertech-eyes-world-s-first-panel-level-pack...

31 AMKOR TECHNOLOGY, INC., Form 8-K current report for the period ended 2026-02-09 (8-K). U.S. Securities and Exchange Commission (filing by AMKOR TECHNOLOGY, INC.) · 9 February 2026 [\[A\]](#)
sec.gov/Archives/edgar/data/1047127/000104712726000007/amkr123125erex-991.htm

32 AMKOR TECHNOLOGY, INC., Form 8-K current report for the period ended 2026-07-27 (8-K). U.S. Securities and Exchange Commission (filing by AMKOR TECHNOLOGY, INC.) · 27 July 2026 [\[A\]](#)
sec.gov/Archives/edgar/data/1047127/000104712726000043/amkr6302026erex-991.htm

33 Amkor Technology Breaks Ground on New Semiconductor Advanced Packaging and Test Campus in Arizona; Expands Investment to \$7 Billion. Amkor Technology [\[A\]](#) ir.amkor.com/news-releases/news-release-details/amkor-technology-breaks-ground-new-semicon...

34 Amkor and TSMC to Expand Partnership and Collaborate on Advanced Packaging in Arizona. TSMC · 4 October 2024 [\[A\]](#)
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35 TSMC and Amkor Technology Announce Long Term Partnership to Accelerate Advanced Packaging in the United States. Amkor Technology [\[A\]](#) ir.amkor.com/news-releases/news-release-details/tsmc-and-amkor-technology-announce-long-te...

36 Investors Guide April 25, 2025. Advantest · 13 May 2025 [\[A\]](#) advantest.com/document/en/investors/ir-library/investors-guide/Investors_Guide_2504E.pdf

packaging, but lost share in bonding and other conventional assembly and packaging tools ²⁶. They still lag significantly behind foreign suppliers ²⁶. ASE's packaging and test business took about \$12.1 billion from outside customers in 2025 ³⁷. With Amkor's \$6.71 billion, the two billed about \$18.8 billion between them, against industry sales of \$791.7 billion ³⁸. That is a small share of the money for a step every chip has to pass through.

Key evaluation criteria

- **Test coverage** is the share of hidden failures caught before they reach a package that cannot be taken apart.
- **Test time per part** sets throughput and cost, and large dies, memory stacks and chiplets all push it up.
- **Probe card flatness and life** decide what wafer sort costs. Every needle must stay in the same plane across a full die and hold that over a long life.
- **Thermal control** matters more every generation. A kilowatt-class accelerator has to be held at temperature in the socket while it is tested at speed.
- **Capacity and geography** are the practical constraint. Taiwan, China and Malaysia hold most of the floor space, and new capacity takes years.

THREE THINGS TO REMEMBER

- Chips are tested early and often because one bad chip can ruin a package of expensive ones.
- Advantest and Teradyne account for most spending on chip testers.
- Four of the top ten outsourced assembly and test firms by 2024 revenue are based in China.

²⁶ Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology (CSET) · 14 July 2025 [\[A\]](https://cset.georgetown.edu/article/inside-beijings-chipmaking-offensive)
cset.georgetown.edu/article/inside-beijings-chipmaking-offensive

³⁷ ASE Technology Holding Co., Ltd., Form 20-F annual report for the period ended 2025-12-31. U.S. Securities and Exchange Commission (filing by ASE Technology Holding Co., Ltd.) · 1 April 2026 [\[A\]](https://sec.gov/Archives/edgar/data/1122411/000119312526135585/d50802d20f.htm)
sec.gov/Archives/edgar/data/1122411/000119312526135585/d50802d20f.htm

³⁸ Global Annual Semiconductor Sales Increase 25.6% to \$791.7 Billion in 2025 - Semiconductor Industry Association. Semiconductor Industry Association · 6 February 2026 [\[A\]](https://semiconductors.org/global-annual-semiconductor-sales-increase-25-6-to-791-7-billion-in-2025)
semiconductors.org/global-annual-semiconductor-sales-increase-25-6-to-791-7-billion-in-2025

Systems and Networking

A finished package is useless until it is bolted to a baseboard, fed a thousand amps and wired to seventy-one other packages. Many firms can do the assembly; few can make the lasers for the optical links.

IN PLAIN TERMS

One AI chip is not enough to train a model. So seventy-two of them are wired together in a rack, a cabinet the size of a wardrobe, and run as one computer. Each chip sits on its own board and draws more than a thousand amps, several times the current a whole house is wired to carry. The chips have to swap results with each other all the time, and a copper wire can carry those signals only a few meters before they fade, so the longer links send them as light down glass fiber. Many companies can build the rack. Only a few can make the lasers that send the light, and that is the narrow point.

IN SHORT

In an Nvidia GB300 NVL72 rack, 72 AI chips are wired together to work as one computer, and the rack draws up to 142 kW¹. Longer links between racks carry data as light, and in March 2026 Nvidia agreed to invest \$2 billion in Lumentum, which makes the lasers for these links, alongside a purchase commitment and future capacity access rights for its laser components²². Many fiber-optic lasers use indium phosphide, and China produced 70 percent of the world's indium in 2025²¹. Since February 2025 China has also required export permits for indium phosphide substrates, the wafers those lasers are grown on²⁹.

¹ System Hardware & Components. Nvidia [\[A\]](https://docs.nvidia.com/enterprise-reference-architectures/nvl72-ai-factory/latest/components.html) docs.nvidia.com/enterprise-reference-architectures/nvl72-ai-factory/latest/components.html

²² NVIDIA Announces Strategic Partnership With Lumentum to Develop State-of-the-Art Optics Technology. Nvidia · 2 March 2026 [\[A\]](https://nvidianews.nvidia.com/news/nvidia-announces-strategic-partnership-with-lumentum-to-develop...) nvidianews.nvidia.com/news/nvidia-announces-strategic-partnership-with-lumentum-to-develop...

²¹ Mineral Commodity Summaries 2026. U.S. Geological Survey · 5 February 2026 [\[A\]](https://pubs.usgs.gov/periodicals/mcs2026/mcs2026-indium.pdf) pubs.usgs.gov/periodicals/mcs2026/mcs2026-indium.pdf

²⁹ AXT INC, Form 10-Q quarterly report for the period ended 2026-06-30. U.S. Securities and Exchange Commission (filing by AXT INC) · 13 August 2026 [\[A\]](https://sec.gov/Archives/edgar/data/1051627/000143774926027677/axti20260630_10q.htm) sec.gov/Archives/edgar/data/1051627/000143774926027677/axti20260630_10q.htm

CHOKEPOINT CARD		HIGH CONCENTRATION
		MODERATELY HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY	
High	Moderate Rated on the two most concentrated parts: Nvidia controls NVLink and its NVSwitch chips, which join the accelerators in a rack, and few firms make the lasers for the optical links.	
	PRICE OR MARKET SIZE Nvidia agreed in March 2026 to invest \$2B each in Coherent and Lumentum, alongside multibillion-dollar purchase commitments for their laser products	
WHO LEADS	US Nvidia NVLink and NVSwitch for links inside a rack; InfiniBand and Spectrum-X Ethernet between racks US Broadcom Switch chips sold to any buyer (Tomahawk, Jericho) and custom AI accelerators TW Foxconn World's largest AI server provider, by its own account; builds in Taiwan, Mexico, Texas CN InnoLight High-speed optical modules; sites in Suzhou, Taiwan and Thailand US Coherent Indium phosphide lasers and data center transceivers	
WHERE IT IS MADE	US United States Switch and accelerator silicon, system design, indium phosphide lasers (Coherent's Sherman, Texas fab) TW Taiwan Contract design and rack assembly; high-layer-count circuit boards JP Japan Laser maker Lumentum's wafer fab in Sagamihara; low-loss board laminate CN China Optical module assembly and test; most of the world's indium; export permits on indium phosphide substrates TH Thailand Chinese module makers' offshore transceiver plants MX Mexico Rack integration for the North American market	
WHY SUBSTITUTION IS POSSIBLE	Rack assembly can be moved, though the move would likely take several quarters, an unsourced estimate. The two concentrated parts are inside the rack, and work is under way on each. UALink is a published open specification for the same job as NVLink, running 200 Gb/s per lane and addressing up to 1,024 endpoints, and AMD's Helios rack, launched in July 2026, runs it over Ethernet. Since May 2025 Nvidia's NVLink Fusion program has let other firms' custom chips use NVLink, including CPUs from Fujitsu and Qualcomm that connect to Nvidia GPUs. That brings more chips onto Nvidia's link, so the dependence stays. For the lasers, Nvidia agreed in March 2026 to invest \$2 billion each in Coherent and Lumentum, alongside multibillion-dollar purchase commitments and future capacity access rights.	

China holds strong positions in the optical link. Chinese firms such as InnoLight assemble high-speed optical modules in volume, in plants that include Suzhou and Thailand. In 2025 China produced about 70 percent of the world's indium, the raw material for the lasers inside those modules. In February 2025 it put indium under new export restrictions and began requiring export permits for indium phosphide substrates, the wafers the lasers are grown on.	WHERE THE US STANDS American firms make the switch chips, the links that join accelerators inside a rack, and the lasers, though some of their wafer fabs are abroad, including Lumentum's in Japan. Nvidia said in August 2026 that Wistron's new plant in Fort Worth, Texas, was producing its GB300 superchips and that Foxconn was building a factory in Houston for its AI systems. In July 2026 the Federal Communications Commission barred new authorizations for devices containing logic-bearing components made by firms on its Covered List.
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A package computes nothing until it is built into a machine, and building the machine is a separate industry from making the package.

How it works

An accelerator ships as a module, the chip on a small board with its power supply and memory stacks. Nvidia calls its version SXM, and the open-standards equivalent is the Open Compute Project's accelerator module. Eight bolt onto a baseboard that carries their power and the switch chips, which pass data between any two modules at full speed.

Rack-scale systems drop the baseboard. An Nvidia GB300 NVL72 holds 18 compute trays plus nine switch trays, 72 GPUs in all, and draws up to 142 kW ¹. Vera Rubin NVL72 uses the same rack footprint ². Inside the rack the trays reach each other over copper. Between neighboring racks, active electrical cables, copper cables sold by firms such as Credo, can carry the signal up to 7 meters ³. Longer links run on glass fiber with an optical transceiver at each end, where a laser turns the electrical signal into pulses of light and a detector at the far end turns the pulses back into current.

Every AI cluster runs two networks that are not interchangeable. Scale-up binds anywhere from a few dozen accelerators (72 in an Nvidia NVL72 rack) to thousands (9,216 in a Google Ironwood superpod) tightly enough that they can read each other's memory, at terabytes per second; scale-out joins those groups to one another at hundreds of gigabits per second. A byte is eight bits, so the inner network is tens of times faster than the outer one. A model too big for one accelerator is split across many. The parts that exchange data constantly stay inside the scale-up group, while whole blocks of layers can sit on different groups across the slower scale-out network ⁴. So scale-up bandwidth sets how efficiently a large model trains.

1 System Hardware & Components. Nvidia [\[A\]](https://docs.nvidia.com/enterprise-reference-architectures/nvl72-ai-factory/latest/components.html) docs.nvidia.com/enterprise-reference-architectures/nvl72-ai-factory/latest/components.html

2 NVIDIA, Partners Drive Next-Gen Efficient Gigawatt AI Factories in Buildup for Vera Rubin. Nvidia · 13 October 2025 [\[A\]](https://blogs.nvidia.com/blog/gigawatt-ai-factories-ocp-vera-rubin) blogs.nvidia.com/blog/gigawatt-ai-factories-ocp-vera-rubin

3 Credo Technology Group Holding Ltd, Form 10-K annual report for the period ended 2026-05-02 (10-K). U.S. Securities and Exchange Commission (filing by Credo Technology Group Holding Ltd) · 15 June 2026 [\[A\]](https://sec.gov/Archives/edgar/data/1807794/000162828026043303/crdo-20260502.htm) sec.gov/Archives/edgar/data/1807794/000162828026043303/crdo-20260502.htm

4 Parallelisms Guide — Megatron Bridge. Nvidia [\[A\]](https://docs.nvidia.com/nemo-framework/user-guide/latest/nemotoolkit/features/parallelisms.html) docs.nvidia.com/nemo-framework/user-guide/latest/nemotoolkit/features/parallelisms.html

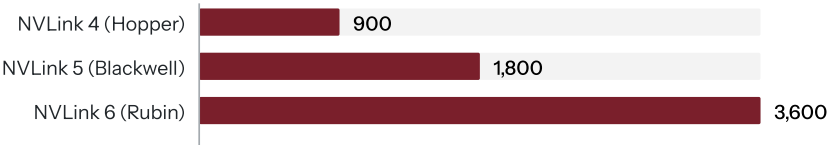
Variants and trade-offs

Scale-up: NVLink, UALink and Google's torus

The designs differ in how many accelerators can share one pool of memory.

- **NVLink and NVSwitch.** Nvidia's per-GPU bandwidth went from 900 GB/s in NVLink 4 to 1,800 in NVLink 5, and the rack's own network moves 130 TB/s on Blackwell ⁵. Nvidia's Rubin launch release of January 2026 gives NVLink 6 as 3,600 GB/s per GPU and 260 TB/s for a Vera Rubin NVL72 rack ⁶. As of October 2026, Nvidia's NVLink product page still lists preliminary figures of 3,000 GB/s and 216 TB/s ⁵.
- **UALink.** The open specification runs 200 Gb/s per lane, four lanes to a station for 800 Gb/s, and can address up to 1,024 endpoints in one group ⁷. AMD's Helios rack, launched in July 2026, joins 72 GPUs and runs UALink over Ethernet for its scale-up network ⁸.
- **Google's 3D torus.** Ironwood, Google's own TPU accelerator, wires 64 chips into each rack, called a cube, and uses optical circuit switches to join cubes into superpods of 9,216 chips that can bypass a failed cube or link ⁹.

NVLink bandwidth per GPU by generation GB/S



Source: NVIDIA NVLink product page (NVLink 4 and 5); NVIDIA Rubin launch release, January 2026 (NVLink 6)

Scale-out: InfiniBand versus Ethernet

InfiniBand, the specialized network built for supercomputers, was the main scale-out network when AI clusters were small and alike. Ethernet switch capacity grew quickly as Broadcom doubled the bandwidth of the switch chips it sells to all comers every generation, from 25.6 Tbps on one chip in Tomahawk 4 ¹⁰ to 51.2 in Tomahawk 5 ¹¹ and 102.4 in Tomahawk 6 ¹². In June 2025 the Ultra Ethernet Consortium published its 1.0 specification, an Ethernet-based stack for AI and supercomputing that covers transport protocols, congestion control and direct memory access ¹³.

5 NVLink & NVLink Switch for Advanced Multi-GPU Communication. Nvidia · 20 April 2026 [A](#) [nvidia.com/en-us/data-center/nvlink](#)

6 NVIDIA Kicks Off the Next Generation of AI With Rubin. Nvidia [A](#) [nvidianews.nvidia.com/news/rubin-platform-ai-supercomputer](#)

7 UALink™ 200G 1.0 Specification Overview. UALink Consortium [A](#) [ualinkconsortium.org/blog/ualink-200g-1-0-specification-overview-802](#)

8 AAI 2026: AMD Launches AMD Helios Rackscale Solution for.... AMD Newsroom · 23 July 2026 [A](#) [newsroom.amd.com/news/aai-2026-helios-update](#)

9 Inside the Ironwood TPU codesigned AI stack. Google Cloud · 6 November 2025 [A](#) [cloud.google.com/blog/products/compute/inside-the-ironwood-tpu-codesigned-ai-stack](#)

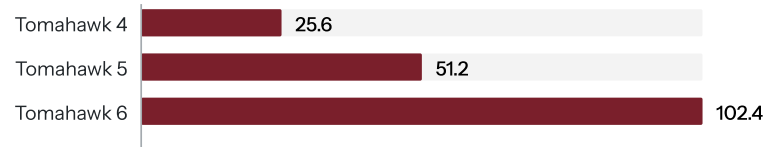
10 Broadcom ships tomahawk 4 industrys highest bandwidth ethernet (Broadcom website). Broadcom [A](#) [investors.broadcom.com/news-releases/news-release-details/broadcom-ships-tomahawk-4-indust...](#)

11 Broadcom Ships Tomahawk 5, Industry's Highest Bandwidth Switch Chip to Accelerate AI/ML Workloads. Broadcom [A](#) [investors.broadcom.com/news-releases/news-release-details/broadcom-ships-tomahawk-5-indust...](#)

12 Broadcom ships tomahawk 6 worlds first 1024 tbps switch (Broadcom website). Broadcom [A](#) [investors.broadcom.com/news-releases/news-release-details/broadcom-ships-tomahawk-6-worlds...](#)

13 Ultra Ethernet Consortium (UEC) Launches Specification 1.0 Transforming Ethernet for AI and HPC at Scale - Ultra Ethernet Consortium. Ultra Ethernet Consortium · 11 June 2025 [A](#) [ultraethernet.org/ultra-ethernet-consortium-uec-launches-specification-1-0-transforming-et...](#)

Broadcom Tomahawk switching capacity on one chip TBPS



Source: Broadcom product releases for Tomahawk 4, 5 and 6

Nvidia sells both networks, and its data center revenue reached \$89.0 billion in the quarter to July 2026, up 117 percent from a year earlier ¹⁴. In the quarter before, it credited its data center growth to Blackwell 300 products and to demand for its "InfiniBand, Spectrum-X Ethernet, and NVLink" solutions ¹⁵.

Optics: pluggable, then co-packaged

Almost every link longer than 7 meters is optical, and a cluster needs several transceivers, the modules that turn electricity into light and back, for each accelerator. Their power cost is one reason Broadcom and Nvidia are moving the optics onto the switch package itself. Broadcom's Tomahawk 6 Davisson cuts optical interconnect power by 70 percent, more than 3.5 times lower than traditional pluggable modules ¹⁶. Nvidia's Spectrum-X Photonics switches, due in 2026, reach 512 ports of 800 gigabits and use four times fewer lasers ¹⁷.

Who makes it

Optical modules are assembled where labor and land are cheap, and the Chinese makers went offshore early. InnoLight has run a Thai plant since 2019 alongside Suzhou and Taiwan ¹⁸, and Eoptolink's Thai subsidiary lists sites in Chonburi and Rayong ¹⁹. The Federal Communications Commission's July 2026 order bars new authorizations for devices that contain logic-bearing hardware components produced by firms on its Covered List, and commenters in the record named optical transceivers as one such component ²⁰. The same order notes that the key players in the optical transceiver market, Coherent and InnoLight among them, do not appear on the Covered List ²⁰.

14 NVIDIA CORP, Form 10-Q quarterly report for the period ended 2026-07-26 (10-Q). U.S. Securities and Exchange Commission (filing by NVIDIA CORP) · 26 August 2026 [\[A\]](#) sec.gov/Archives/edgar/data/1045810/000104581026000075/nvda-20260726.htm

15 NVIDIA CORP, Form 10-Q quarterly report for the period ended 2026-04-26 (10-Q). U.S. Securities and Exchange Commission (filing by NVIDIA CORP) · 20 May 2026 [\[A\]](#) sec.gov/Archives/edgar/data/1045810/000104581026000052/nvda-20260426.htm

16 Broadcom announces tomahawkr 6 davisson industrys first 1024 (Broadcom website). Broadcom [\[A\]](#) investors.broadcom.com/news-releases/news-release-details/broadcom-announces-tomahawkr-6-davisson-industrys-first-1024

17 NVIDIA Announces Spectrum-X Photonics, Co-Packaged Optics Networking Switches to Scale AI Factories to Millions of GPUs. Nvidia · 18 March 2025 [\[A\]](#) nvidianews.nvidia.com/news/nvidia-spectrum-x-co-packaged-optics-networking-switches-ai-factories-to-millions-of-gpus

18 InnoLight Technology, company overview page. InnoLight Technology [\[A\]](#) innolight.com/about

19 Eoptolink Technology, contacts page. Eoptolink Technology [\[A\]](#) eoptolink.com/about-us/contacts

20 Federal Communications Commission FCC-26-50. U.S. Federal Communications Commission [\[A\]](#) docs.fcc.gov/public/attachments/FCC-26-50A1.pdf

The lasers inside those modules come from far fewer firms. Indium phosphide is used in the high-speed laser diodes and photodetectors for optical communications, and China accounted for 70 percent of world indium production in 2025 ²¹. In February 2025 China's Ministry of Commerce placed indium under new export restrictions ²¹. In March 2026 Nvidia agreed to invest \$2 billion in Lumentum, alongside a multibillion purchase commitment and future capacity access rights for advanced laser components ²². It made the same \$2 billion investment in Coherent, with a multibillion-dollar purchase commitment for advanced laser and optical networking products ²³.

Two US firms, Broadcom and Marvell, design both custom accelerators and switch silicon. Broadcom sells the Ethernet switch chips other firms build their switches around, along with custom AI accelerators, and its AI semiconductor revenue reached \$16.7 billion in the third quarter of fiscal 2026, up 221 percent ²⁴. Marvell's five-year agreement with AWS, announced in December 2024, covers custom AI chips alongside the optical and networking parts that go with them ²⁵.

Much of the physical assembly is done by Taiwanese firms. Foxconn booked NT\$8.1 trillion of revenue in 2025, up 18 percent, with cloud and networking among the drivers ²⁶. Assembly is moving closer to the customer. In April 2025 Nvidia said it was building supercomputer manufacturing plants in Texas with Foxconn in Houston and Wistron in Dallas, with mass production expected to ramp up in the next 12 to 15 months ²⁷. In August 2026 Nvidia said Wistron's new plant in Fort Worth, Texas, was producing its GB300 superchips and Foxconn was building its factory in Houston ²⁸.

The chokepoint

Several contract manufacturers on three continents assemble racks, and the power shelves, copper busbars, cables and connectors have many suppliers. Rack-scale systems are complex, and in its filing for the quarter to April 2026 Nvidia said that complexity had caused production delays ¹⁵. Moving Foxconn's share to Quanta and Wistron would likely take several quarters, though no source puts a figure on it.

The parts that cannot be replaced that fast are the components that go into the rack.

21 Mineral Commodity Summaries 2026. U.S. Geological Survey · 5 February 2026 [\[A\]](https://pubs.usgs.gov/periodicals/mcs2026/mcs2026-indium.pdf) pubs.usgs.gov/periodicals/mcs2026/mcs2026-indium.pdf

22 NVIDIA Announces Strategic Partnership With Lumentum to Develop State-of-the-Art Optics Technology. Nvidia · 2 March 2026 [\[A\]](https://nvidianews.nvidia.com/news/nvidia-announces-strategic-partnership-with-lumentum-to-develop...) nvidianews.nvidia.com/news/nvidia-announces-strategic-partnership-with-lumentum-to-develop...

23 NVIDIA and Coherent Announce Strategic Partnership to Develop Optics Technology to Scale Next-Generation Data Center Architecture. Nvidia · 2 March 2026 [\[A\]](https://nvidianews.nvidia.com/news/nvidia-and-coherent-announce-strategic-partnership-to-develop-o...) nvidianews.nvidia.com/news/nvidia-and-coherent-announce-strategic-partnership-to-develop-o...

24 Broadcom Inc., Form 8-K current report for the period ended 2026-09-02 (8-K). U.S. Securities and Exchange Commission (filing by Broadcom Inc.) · 2 September 2026 [\[A\]](https://sec.gov/Archives/edgar/data/1730168/000173016826000076/avgo-08022026x8kxex99.htm) sec.gov/Archives/edgar/data/1730168/000173016826000076/avgo-08022026x8kxex99.htm

25 Marvell Technology, Inc., Form 8-K current report for the period ended 2024-12-02 (8-K). U.S. Securities and Exchange Commission (filing by Marvell Technology, Inc.) · 2 December 2024 [\[A\]](https://sec.gov/Archives/edgar/data/1835632/000183563224000193/final2024_12x02xmarvell-.htm) sec.gov/Archives/edgar/data/1835632/000183563224000193/final2024_12x02xmarvell-.htm

26 Hon Hai Technology Group (Foxconn) Announces FY2025 & 4Q25 Financial Results - Hon Hai Technology Group. Hon Hai Precision Industry (Foxconn) · 16 March 2026 [\[A\]](https://honhai.com/en-us/press-center/press-releases/latest-news/1978) honhai.com/en-us/press-center/press-releases/latest-news/1978

27 NVIDIA to Manufacture American-Made AI Supercomputers in US for First Time. Nvidia · 14 April 2025 [\[A\]](https://blogs.nvidia.com/blog/nvidia-manufacture-american-made-ai-supercomputers-us) blogs.nvidia.com/blog/nvidia-manufacture-american-made-ai-supercomputers-us

28 NVIDIA and Partners Build in America, for America. Nvidia · 5 August 2026 [\[A\]](https://blogs.nvidia.com/blog/nvidia-and-partners-build-in-america-for-america) blogs.nvidia.com/blog/nvidia-and-partners-build-in-america-for-america

15 NVIDIA CORP, Form 10-Q quarterly report for the period ended 2026-04-26 (10-Q). U.S. Securities and Exchange Commission (filing by NVIDIA CORP) · 20 May 2026 [\[A\]](https://sec.gov/Archives/edgar/data/1045810/000104581026000052/nvda-20260426.htm) sec.gov/Archives/edgar/data/1045810/000104581026000052/nvda-20260426.htm

- **Indium phosphide laser capacity.** In March 2026 Nvidia agreed to invest \$2 billion in Coherent, alongside a multibillion-dollar purchase commitment and future access and capacity rights for Coherent's advanced laser and optical networking products ²³. In 2025 China produced 70 percent of the world's indium, which those lasers need, and it put indium under new export restrictions in February 2025 ²¹.
- **Indium phosphide substrates.** China added indium phosphide substrates, the wafers the lasers are grown on, to its export control list on 4 February 2025 ²⁹. In its filing for the quarter to June 2026, AXT, a US-listed maker of these wafers that does all its manufacturing in China, called the permits the most significant challenge it faces and said it could not estimate when it would resume shipping the wafers to the United States ²⁹.
- **NVSwitch.** NVLink and NVSwitch are Nvidia's own designs, and UALink is an open standard designed for accelerator communications within a pod ⁷. Since May 2025 Nvidia's NVLink Fusion program has let other firms' custom chips use NVLink, including CPUs from Fujitsu and Qualcomm that connect to Nvidia GPUs ³⁰.
- **High-layer-count circuit boards.** The boards, and the low-loss laminate they are built from, are concentrated in Taiwan and Japan; see Substrates and PCBs.

Optical module assembly is concentrated, but where it happens follows cost and policy, and it has moved before, as the Chinese makers' Thai plants show ¹⁸.

Key evaluation criteria

- **Scale-up domain size** is how many accelerators share one pool of memory: up to 1,024 endpoints in the UALink spec ⁷ and 9,216 for an Ironwood superpod ⁹.
- **Bandwidth per accelerator** limits how efficiently one model can be split across chips. NVLink 6 is 3,600 GB/s ⁶.
- **Picojoules per bit** is the energy cost of moving data. Broadcom says traditional pluggable optics consume more power as AI traffic grows, and its co-packaged switch cuts optical interconnect power by 70 percent ¹⁶.
- **Serviceability** changes with co-packaged optics, which move the optics off plug-in modules and onto the switch package. Broadcom's Davisson switch keeps its lasers in field-replaceable modules ¹⁶.

23 NVIDIA and Coherent Announce Strategic Partnership to Develop Optics Technology to Scale Next-Generation Data Center Architecture. Nvidia · 2 March 2026 [A] nvidianews.nvidia.com/news/nvidia-and-coherent-announce-strategic-partnership-to-develop-o-...

21 Mineral Commodity Summaries 2026. U.S. Geological Survey · 5 February 2026 [A] pubs.usgs.gov/periodicals/mcs2026/mcs2026-indium.pdf

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7 UALink™ 200G 1.0 Specification Overview. UALink Consortium [A] ualinkconsortium.org/blog/ualink-200g-1-0-specification-overview-802

30 NVIDIA Unveils NVLink Fusion for Industry to Build Semi-Custom AI Infrastructure With NVIDIA Partner Ecosystem. Nvidia [A] nvidianews.nvidia.com/news/nvidia-nvlink-fusion-semi-custom-ai-infrastructure-partner-ecos-...

18 InnoLight Technology, company overview page. InnoLight Technology [A] innolight.com/about

9 Inside the Ironwood TPU codedigned AI stack. Google Cloud · 6 November 2025 [A] cloud.google.com/blog/products/compute/inside-the-ironwood-tpu-codedigned-ai-stack

6 NVIDIA Kicks Off the Next Generation of AI With Rubin. Nvidia [A] nvidianews.nvidia.com/news/rubin-platform-ai-supercomputer

16 Broadcom announces tomahawk 6 davisson industrys first 1024 (Broadcom website). Broadcom [A] investors.broadcom.com/news-releases/news-release-details/broadcom-announces-tomahawk-6-d-...

- **Supply concentration** is in the components: many firms assemble the modules; far fewer can make the lasers inside them.

FOUR THINGS TO REMEMBER

- An AI rack wires 72 chips together to run as one computer.
- Almost every link longer than 7 meters carries its signal as light, because copper fades over longer runs.
- NVLink switching and the lasers are the hard parts, and moving rack assembly would take an estimated several quarters.
- China produced about 70 percent of the world's indium in 2025 and has required export permits for indium phosphide substrates since February 2025.

Data Centers and Power

Chips are no longer the only slow part of a data center buildout. A large transformer commonly took three years to arrive in 2024, GE Vernova is working toward 30 GW of gas turbine output a year in 2030, and Texas had about 474 GW of large loads, mostly data centers, seeking a grid connection in June 2026. In August 2026 the governor of Texas ordered every data center in that queue audited before any of them moves forward.

IN PLAIN TERMS

A data center's job is to feed electricity to the machines inside it and carry away the heat they give off. One rack of AI chips, a cabinet the size of a wardrobe, draws up to 142 kilowatts, and every watt of it comes back out as heat, so the rack is cooled by liquid piped through it. A large training site already holds more than a hundred thousand chips, and the newest sites are planned in gigawatts. One gigawatt is the whole output of a large power station, and OpenAI's planned sites add up to more than nine of them by 2029. Getting that much electricity to the door is harder than putting up the building, because the transformers and heavy switches that connect a site to the grid, and the turbines that make the power, come from a few suppliers and take years to arrive.

IN SHORT

Large power transformers, a core part of the electric grid, commonly took 36 months to deliver in 2024, against less than a year before the pandemic ¹. GE Vernova says data center orders for its electrification business, which makes grid equipment such as transformers and switchgear, passed \$5 billion in the first half of 2026, more than double its total for 2025 ¹³. In Texas, about 474 GW of large loads, mostly data centers, were seeking a grid connection in June 2026 ¹⁷. In August 2026 the governor of Texas ordered every data center in that queue audited before any of them moves forward ¹⁹.

¹ U.S. Department of Energy Large Power Transformer Resilience Report to Congress, July 2024. U.S. Department of Energy · 10 July 2024 [\[A\]](https://energy.gov/sites/default/files/2024-10/EXEC-2022-001242%20-%20Large%20Power%20Transformer%20Report%20to%20Congress.pdf)

¹³ GE Vernova Inc., Form 8-K current report for the period ended 2026-07-22 (8-K). U.S. Securities and Exchange Commission (filing by GE Vernova Inc.) · 22 July 2026 [\[A\]](https://sec.gov/Archives/edgar/data/1996810/000199681026000147/gevpresrelease2q26.htm)

¹⁷ Electric Reliability Council of Texas, ERCOT update to the Senate Committee on Business and Commerce, 29 July 2026. Electric Reliability Council of Texas · 29 July 2026 [\[A\]](https://ercot.com/files/docs/2026/07/29/ERCOT-Senate-July-29-Panel-1-Assessing-The-Grid.pdf)

¹⁹ Governor Abbott Directs Comprehensive Data Center Audit. Texas [\[A\]](https://gov.texas.gov/news/post/governor-abbott-directs-comprehensive-data-center-audit)

CHOKEPOINT CARD		HIGH CONCENTRATION
		MODERATELY HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY	
High	Moderate	
	Nvidia names nine data center power system providers for its gigawatt designs, but a large transformer commonly took three years to arrive in 2024 and GE Vernova's gas backlog and reserved slots stood at 116 GW in mid-2026.	
	PRICE OR MARKET SIZE	
	Large power transformer lead times of 36 months commonly quoted in 2024, against under a year before the pandemic	
	GE Vernova's gas backlog and reserved slots grew from 100 GW to 116 GW in the second quarter of 2026	
WHO LEADS	US GE Vernova 116 GW of gas equipment backlog and reserved factory slots at mid-2026; also makes transformers and switchgear, including through Prolec GE CH Hitachi Energy Large power transformers and high-voltage switchgear DE Siemens Energy Grid technologies, transformers, turbines JP Mitsubishi Power Power generation equipment, including gas turbines; named by GE Vernova as a key competitor alongside Siemens Energy US Vertiv Data center power and cooling systems; NVIDIA gigawatt AI factory partner FR Schneider Electric Electrical distribution and cooling; partner in NVIDIA's 800-volt DC designs	
WHERE IT IS MADE	US United States Most new AI capacity; ERCOT and PJM carry the load growth CH Switzerland Hitachi Energy and ABB transformer and switchgear engineering DE Germany Siemens Energy grid technologies and turbines TW Taiwan Delta Electronics power shelves, busbars and thermal modules JP Japan Mitsubishi Heavy Industries power equipment, including gas turbines; Hitachi group transformers	
WHY SUBSTITUTION IS POSSIBLE	Nvidia names nine data center power system providers for its gigawatt designs, so a buyer can choose among suppliers. Money cannot shorten the wait. In 2024, large power transformer lead times of 36 months were commonly quoted, against under a year before the pandemic, and the longest reached 60 months. An IEA survey published in 2025 found waits of up to four years worldwide. GE Vernova's gas equipment backlog and slot reservations reached 116 GW in mid-2026, and it expects to reach 20 GW of annual gas turbine output in the third quarter of 2026.	
WHERE CHINA STANDS	China has spare generating capacity, a large domestic industry making	

transformers and switchgear, and can connect new sites quickly. Its AI buildout is limited by the supply of accelerators, and it has power to spare.	WHERE THE US STANDS The United States has the demand and the money but cannot shorten the wait for equipment. Transformers and turbines both take years to arrive. Most large power transformers are imported, and US factories supplied 29.2 percent of those bought in the US in 2023, measured by capacity. No restarted nuclear reactor is serving data centers yet.
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For thirty years the semiconductor industry set the pace and everything downstream followed. A wafer clears a leading-edge fab in months; in 2024 a large power transformer commonly took three years, and before the pandemic the same order took under one ¹.

How it works

A rack is now the unit of AI compute. A GB300 NVL72 draws up to 142 kW through eight 33 kW power shelves, the rack's own power supplies ². Colossus 1, an AI data center in Memphis, Tennessee, held an estimated 230,000 Nvidia GPUs by July 2025 ³.

Between the grid and the rack, a substation steps the high voltage down with transformers. Switchgear, the building's heavy circuit breakers, can cut any part of the site off in a fault. Battery-backed supplies hold the load for the seconds it takes backup generators to start. Distribution boards split the feed among the rows of racks. At the back of each rack a busbar, a solid copper bar doing a job a cable would melt at, carries the current down to the trays. Every one of those is heavy equipment with its own lead time.

Heat leaves in water. Cold plates on the GPU packages pass it to a building loop that releases it outdoors, and Nvidia's Rubin racks run coolant at up to 45 °C, warm enough that in many climates the loop can reject heat without turning on chillers ⁵.

Nvidia is also moving rack distribution to 800 volts of direct current. Raising the voltage cuts the current for the same power, and heat in copper comes from current, so the same conductor carries over 150 percent more power and the 200 kg busbars feeding a single rack are no longer needed ⁶.

Variants and trade-offs

1

U.S. Department of Energy Large Power Transformer Resilience Report to Congress, July 2024. U.S. Department of Energy · 10 July 2024 [\[A\]](https://www.energy.gov/sites/default/files/2024-10/EXEC-2022-001242%20-%20Large%20Power%20Transformer%20Report%20to%20Congress.pdf)

2

System Hardware & Components. Nvidia [\[A\]](https://docs.nvidia.com/enterprise-reference-architectures/nvl72-ai-factory/latest/components.html)

3

Colossus 1 | AI data centers. Epoch AI [\[A\]](https://epoch.ai/data/ai-data-centers/directory/colossus-1)

5

Hotter Than a Hot Tub: The 45°C Breakthrough to Cool AI's Biggest Machines. Nvidia · 22 June 2026 [\[A\]](https://blogs.nvidia.com/blog/liquid-cooling-ai-factories)

6

NVIDIA, Partners Drive Next-Gen Efficient Gigawatt AI Factories in Buildup for Vera Rubin. Nvidia · 13 October 2025 [\[A\]](https://blogs.nvidia.com/blog/gigawatt-ai-factories-ocp-vera-rubin)

Cooling

- **Air.** Heat exchangers in the rack door work at moderate densities, but Nvidia's GB300 NVL72 rack is liquid cooled ².
- **Direct-to-chip liquid.** Nvidia's Rubin platform is 100 percent liquid cooled, and every cloud provider and data center operator building for it is moving to liquid ⁵.
- **Immersion.** Higher density still, but hard to service.

Nvidia says the cooling supply chain is keeping pace with the move to liquid, and Schneider Electric's cooling division, Motivair, has worked alongside Nvidia's product roadmap for nearly a decade ⁵.

Rack power

Nvidia's 800-volt DC architecture is drawn for racks from 100 kW to more than a megawatt, with megawatt racks from 2027, because the 54-volt distribution in today's racks begins to hit physical limits once racks exceed 200 kW ⁷.

Nvidia names nine data center power system providers for its 800-volt gigawatt designs, among them ABB, Eaton, Hitachi Energy, Mitsubishi Electric, Schneider Electric, Siemens and Vertiv ⁶.

A megawatt rack changes the busbar, the floor loading, the coolant flow, the leak detection and the stored energy that carries the rack through a dip. Nvidia's Vera Rubin NVL72 rack design holds 20 times more energy storage to keep power steady ⁶.

Where the electrons come from

- **Grid interconnection.** The slow path, with lengthy queues to connect ⁴.
- **Behind-the-meter gas,** generation on the site itself. The fast path, which at least three of the seven Stargate sites will use to sidestep grid queues ⁴.
- **Nuclear.** Existing plants already sell power to data centers, and Talen supplies Amazon's data center campus next to the Susquehanna nuclear plant in Pennsylvania under a June 2025 contract expected to reach 1,920 MW no later than 2032 ⁸. Restarts and new reactors are still prospective. Constellation

² System Hardware & Components. Nvidia [\[A\]](https://docs.nvidia.com/enterprise-reference-architectures/nvl72-ai-factory/latest/components.html) docs.nvidia.com/enterprise-reference-architectures/nvl72-ai-factory/latest/components.html

⁵ Hotter Than a Hot Tub: The 45°C Breakthrough to Cool AI's Biggest Machines. Nvidia · 22 June 2026 [\[A\]](https://blogs.nvidia.com/blog/liquid-cooling-ai-factories)
blogs.nvidia.com/blog/liquid-cooling-ai-factories

⁷ NVIDIA 800 VDC Architecture Will Power the Next Generation of AI Factories. Nvidia · 20 May 2025 [\[A\]](https://developer.nvidia.com/blog/nvidia-800-v-hvdc-architecture-will-power-the-next-generation-of-ai-factories)
developer.nvidia.com/blog/nvidia-800-v-hvdc-architecture-will-power-the-next-generation-of...

⁶ NVIDIA, Partners Drive Next-Gen Efficient Gigawatt AI Factories in Buildup for Vera Rubin. Nvidia · 13 October 2025 [\[A\]](https://blogs.nvidia.com/blog/gigawatt-ai-factories-ocp-vera-rubin)
blogs.nvidia.com/blog/gigawatt-ai-factories-ocp-vera-rubin

⁴ OpenAI Stargate: where the US sites stand. Epoch AI · 17 April 2026 [\[A\]](https://epoch.ai/publications/openai-stargate-where-the-us-sites-stand)
epoch.ai/publications/openai-stargate-where-the-us-sites-stand

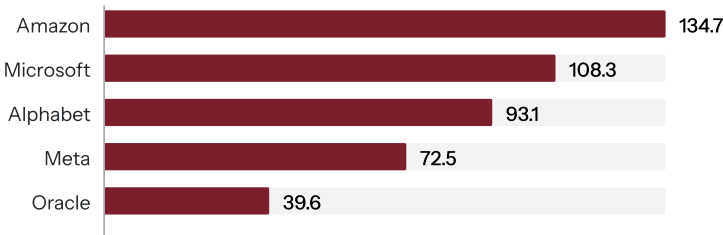
⁸ Talen Energy Corp, Form 8-K current report for the period ended 2025-06-11 (8-K). U.S. Securities and Exchange Commission (filing by Talen Energy Corp) · 11 June 2025 [\[A\]](https://sec.gov/Archives/edgar/data/1622536/000162828025030559/a20250611pressreleasebusin.htm)
sec.gov/Archives/edgar/data/1622536/000162828025030559/a20250611pressreleasebusin.htm

signed a power purchase agreement with Microsoft to restart Three Mile Island Unit 1 as the 835 MW Crane Clean Energy Center ⁹. The plant shut in 2019, and a \$1 billion federal loan closed in November 2025 partly finances its restart, subject to Nuclear Regulatory Commission licensing approvals ¹⁰. No restarted reactor is serving data centers yet.

Who makes it

The largest data center operators pay for the buildout. Alphabet, Amazon, Meta, Microsoft and Oracle spent \$448.2 billion of capital in 2025, and if that trend continues they will spend \$770 billion in 2026 ¹¹.

Capital spending by five large US data center operators, 2025 \$B



Source: Epoch AI, hyperscaler capex trend, February 2026, from company filings

Campuses are now described in gigawatts. Epoch AI projects OpenAI's seven US Stargate sites to exceed 9 GW by 2029, with Abilene, Texas, growing from an estimated 0.3 GW in April to 1.2 GW in the fourth quarter of 2026 ⁴.

The equipment vendors are the constraint. GE Vernova builds large gas turbines, and its 2025 annual report names Siemens Energy and Mitsubishi Power among the key competitors of its power generation business ¹². Hitachi Energy, Siemens Energy, GE Vernova, ABB, Eaton and Schneider Electric supply transformers and switchgear. GE Vernova bought the remaining half of Prolec GE, a transformer maker, in the first half of 2026 ¹³. GE Vernova's gas equipment backlog and reserved factory slots went from 100 GW to 116 GW in the second quarter of 2026, and its electrification orders from data centers passed \$5 billion in the first half, more than double its 2025 total ¹³.

9 Constellation Ahead of Schedule for Launch of Crane Clean Energy Center. Constellation Energy · 19 February 2025 ^A constellationenergy.com/news/2025/constellation-ahead-of-schedule-for-launch-of-crane-clea...

10 Energy Department Closes Loan to Restart Nuclear Power Plant in Pennsylvania. U.S. Department of Energy · 17 November 2025 ^A energy.gov/articles/energy-department-closes-loan-restart-nuclear-power-plant-pennsylvania

11 Hyperscaler capex has quadrupled since GPT-4's release. Epoch AI · 26 February 2026 ^A epoch.ai/data-insights/hyperscaler-capex-trend

4 OpenAI Stargate: where the US sites stand. Epoch AI · 17 April 2026 ^A epoch.ai/publications/openai-stargate-where-the-us-sites-stand

12 GE Vernova Inc., Form 10-K annual report for the period ended 2025-12-31 (10-K). U.S. Securities and Exchange Commission (filing by GE Vernova Inc.) · 29 January 2026 ^A sec.gov/Archives/edgar/data/1996810/000199681026000015/gev-20251231.htm

13 GE Vernova Inc., Form 8-K current report for the period ended 2026-07-22 (8-K). U.S. Securities and Exchange Commission (filing by GE Vernova Inc.) · 22 July 2026 ^A sec.gov/Archives/edgar/data/1996810/000199681026000147/gevpressrelease2q26.htm

GE Vernova annual gas turbine output, planned GW/YR

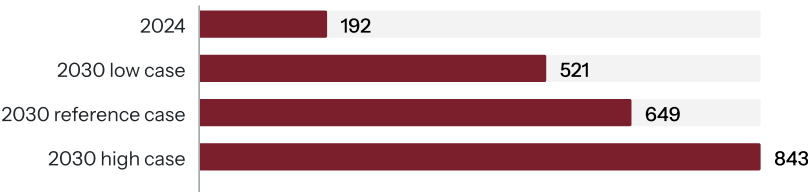


Source: GE Vernova second-quarter 2026 results, July 2026

Capacity and demand

US data centers used 192 TWh in 2024, 4.7 percent of national electricity, according to a June 2026 estimate by Lawrence Berkeley National Laboratory that leaves out cryptocurrency mining ¹⁴. The lab's reference case projects 464 TWh in 2028 and 649 TWh in 2030, 11.8 percent of forecast US electricity use, and its scenarios for 2030 range from 521 to 843 TWh, or 9.5 percent to 15.3 percent ¹⁴. In its September 2026 Short-Term Energy Outlook, the Energy Information Administration expects record US electricity sales of 4,135 TWh in 2026 and 4,211 TWh in 2027, growth of almost 2 percent in each year, driven by data centers and manufacturing ¹⁵. The same outlook lowers its 2027 electricity sales forecast for the region that includes Texas by 4.7 percent from its August forecast, and it notes that Texas has paused connecting new data centers to the grid while it audits proposed projects ¹⁵.

US data center electricity use, 2024 and 2030 projection range TWH



Source: Lawrence Berkeley National Laboratory, June 2026

Chip efficiency is still improving. Google's Ironwood TPU delivers twice the performance per watt of Trillium, its previous generation ¹⁶. Energy per token,

14 Lawrence Berkeley National Laboratory LBL Publications. U.S. Department of Energy · 16 June 2026 [A](#)
energy.gov/documents/united-states-data-center-energy-usage-report-2025-update

15 September 2026 Short-Term Energy. U.S. Energy Information Administration · 8 September 2026 [A](#)
eia.gov/outlooks/steo/archives/sep26.pdf

16 Inside the Ironwood TPU codesigned AI stack. Google Cloud · 6 November 2025 [A](#) cloud.google.com/blog/products/compute/inside-the-ironwood-tpu-codesigned-ai-stack

where a token is the chunk of text a model reads or writes, can fall while total energy use still rises, if the number of tokens rises faster.

The chokepoint

Announced capacity and energized capacity are a long way apart. ERCOT, the grid operator for most of Texas, was tracking about 474 GW of large loads seeking a connection in June 2026, roughly 90 percent of it data centers ¹⁷. ERCOT's large load update of March 13, 2026, counted 9,042 MW approved to energize, but judging by peak monthly use, ERCOT believed only 3,883 MW of it was operating ¹⁸. In a preliminary review in July 2026, ERCOT found about 205 GW of the queue eligible for Batch Zero, its first study of connection requests as a group ¹⁷. On August 3, 2026, Texas Governor Greg Abbott ordered the state's Public Utility Commission and ERCOT to audit every data center in the interconnection process before any data center project moves forward ¹⁹.

Behind that queue sit the equipment lead times.

- **Large power transformers.** In 2024, 36-month lead times were commonly quoted and the worst reached 60, against under a year before the pandemic; by a Commerce Department estimate, 82 percent of the units put into US service in 2019 were imported ¹. A survey of the industry published by the IEA in 2025 found that large power transformers took up to four years to secure worldwide, and that average lead times had almost doubled since 2021 ²⁰. Measured by capacity, US factories supplied 29.2 percent of the transformers of 60 MVA and above bought in the US in 2023, and imports supplied the rest ²¹.
- **Gas turbines.** GE Vernova expects to reach 20 GW of annual gas turbine output in the third quarter of 2026, 24 GW in 2028 and 30 GW in 2030, while its gas equipment backlog and slot reservations stood at 116 GW at mid-year ¹³.
- **Firm new generation,** the kind that runs whatever the weather. The 835 MW Crane plant shut in 2019, and its restart depends on Nuclear Regulatory Commission licensing approvals ¹⁰. The NRC has approved a fuel license amendment for the plant, and Constellation expects to restart it in 2027 ²².

¹⁷ Electric Reliability Council of Texas, ERCOT update to the Senate Committee on Business and Commerce, 29 July 2026.

Electric Reliability Council of Texas · 29 July 2026 [A] ercot.com/files/docs/2026/07/29/ERCOT-Senate-July-29-Panel-1-Assessing-The-Grid.pdf

¹⁸ Electric Reliability Council of Texas, Large Load Interconnection Status Update, 13 March 2026. Electric Reliability Council of Texas · 13 March 2026 [A] ercot.com/files/docs/2026/03/12/March-TAC-Report.pdf

¹⁹ Governor Abbott Directs Comprehensive Data Center Audit. Texas [A] gov.texas.gov/news/post/governor-abbott-directs-comprehensive-data-center-audit

¹ U.S. Department of Energy Large Power Transformer Resilience Report to Congress, July 2024. U.S. Department of Energy · 10 July 2024 [A] energy.gov/sites/default/files/2024-10/EXEC-2022-001242%20-%20Large%20Power%20Transformer%20Summary.pdf

²⁰ Executive summary – Building the Future Transmission Grid. IEA [A] iea.org/reports/building-the-future-transmission-grid/executive-summary

²¹ Large Power Transformers from South Korea—Staff Report. Usitc · 6 August 2024 [A] usitc.gov/publications/701_731/pub5531.pdf

¹³ GE Vernova Inc., Form 8-K current report for the period ended 2026-07-22 (8-K). U.S. Securities and Exchange Commission (filing by GE Vernova Inc.) · 22 July 2026 [A] sec.gov/Archives/edgar/data/1996810/000199681026000147/gevpresrelease2q26.htm

¹⁰ Energy Department Closes Loan to Restart Nuclear Power Plant in Pennsylvania. U.S. Department of Energy · 17 November 2025 [A] energy.gov/articles/energy-department-closes-loan-restart-nuclear-power-plant-pennsylvania

²² Constellation Reports Second Quarter 2026 Results. Constellation Energy · 6 August 2026 [A] constellationenergy.com/news/2026/08/constellation-reports-second-quarter-2026-results.html

Memory is short too, and Micron's quarterly report for the period ended May 28, 2026, says AI-driven memory and storage growth is outpacing industry supply ²³. Power equipment takes years to arrive, and both limit how much of the 2026 capital spending turns into working compute.

Key evaluation criteria

- **Time to power** counts the months from signed lease to energized megawatt, and it is the number developers compete on.
- **Transformer and turbine lead time** covers the two queues that set the schedule. Large power transformer lead times of 36 months were commonly quoted in 2024 ¹. GE Vernova's gas backlog and slot reservations stood at 116 GW in mid-2026, against a planned 20 GW a year of output from the third quarter ¹³.
- **Rack density supported** decides what an existing hall can take. A GB300 NVL72 rack draws up to 142 kW and is liquid cooled ².
- **Firmness of supply** separates a signed interconnection agreement from a delivered transformer.
- **Energy per token** tracks how much electricity a model uses for each token it reads or writes, and chips with higher performance per watt, such as Google's Ironwood TPU, lower it ¹⁶.

FOUR THINGS TO REMEMBER

- One AI rack draws up to 142 kilowatts, too much heat for air, so racks are cooled with liquid.
- The newest AI sites are planned in gigawatts, each the output of a large power station.
- Power equipment is one of the slow parts, and in 2024 lead times of 36 months were commonly quoted for a large transformer.
- China has power to spare and is limited by the supply of AI chips.

23 MICRON TECHNOLOGY INC, Form 10-Q quarterly report for the period ended 2026-05-28 (10-Q). U.S. Securities and Exchange Commission (filing by MICRON TECHNOLOGY INC) · 25 June 2026 [\[A\]](https://sec.gov/Archives/edgar/data/723125/000072312526000015/mu-20260528.htm)

1 U.S. Department of Energy Large Power Transformer Resilience Report to Congress, July 2024. U.S. Department of Energy · 10 July 2024 [\[A\]](https://energy.gov/sites/default/files/2024-10/EXEC-2022-001242%20-%20Large%20Power%20Transformer%20Report%20to%20Congress.pdf)

13 GE Vernova Inc., Form 8-K current report for the period ended 2026-07-22 (8-K). U.S. Securities and Exchange Commission (filing by GE Vernova Inc.) · 22 July 2026 [\[A\]](https://sec.gov/Archives/edgar/data/1996810/000199681026000147/gevpressrelease2q26.htm)

2 System Hardware & Components. Nvidia [\[A\]](https://docs.nvidia.com/enterprise-reference-architectures/nvl72-ai-factory/latest/components.html)

16 Inside the Ironwood TPU codesigned AI stack. Google Cloud · 6 November 2025 [\[A\]](https://cloud.google.com/blog/products/compute/inside-the-ironwood-tpu-codesigned-ai-stack)

The Economics of AI Chips

In Epoch AI's December 2025 estimate for Nvidia's B200, the silicon is the cheap part. Memory and packaging are most of the cost.

IN PLAIN TERMS

A bill of materials is the list of parts inside a product and what each one costs to build. Epoch AI estimated in December 2025 that Nvidia's B200, a Blackwell accelerator, cost about \$6,400 to build. The processor itself, the chip that does the calculating, was the cheap part at about \$900. The stacked memory beside it accounted for about half, and the packaging that wires the two together cost more than the chip. Three firms dominate the world market for that memory and one Taiwanese firm does that packaging, so a few firms supply the costliest parts.

IN SHORT

Epoch AI estimated in December 2025 that an Nvidia B200 cost around \$6,400 to build, against a selling price of \$30,000 to \$40,000 per chip reported in March 2024 ¹. Its chip sales model, with data through October 2025, puts Nvidia's compute revenue per GPU in GB200 rack systems at \$33,000 to \$42,000 ². Memory and advanced packaging make up most of the \$6,400 build cost, and the two processor dies cost less than the packaging that joins them to the memory ¹. Three companies, SK hynix, Samsung and Micron, dominate the world market for that kind of memory ³.

In December 2025 Epoch AI estimated that building a Blackwell B200 cost about \$6,400, and reports in March 2024 put its selling price at \$30,000 to \$40,000 per chip ¹. Epoch AI's chip sales model, with data through October 2025, puts Nvidia's compute revenue per GPU in its GB200 rack systems at \$33,000 to \$42,000, a figure that leaves out the networking gear in those racks ². That \$6,400 splits into stages that are expensive because of physics, because capacity is short, or because one firm sets the price.

¹ NVIDIA's B200 costs around \$6,400 to produce. Epoch AI · 10 December 2025 [\[A\] epoch.ai/data-insights/b200-cost-breakdown](https://epoch.ai/data-insights/b200-cost-breakdown)

² AI chip sales documentation. Epoch AI · 8 January 2026 [\[A\] epoch.ai/data/ai-chip-sales-documentation/methodology#nvidia](https://epoch.ai/data/ai-chip-sales-documentation/methodology#nvidia)

³ Understanding the Biden Administration's Updated Export Controls. Center for Strategic and International Studies · 11 December 2024 [\[A\] csis.org/analysis/understanding-biden-administrations-updated-export-controls](https://csis.org/analysis/understanding-biden-administrations-updated-export-controls)

How it works

Three numbers set the cost of a die, the finished rectangle of circuitry cut out of a wafer.

- **Wafer price.** TSMC does not publish it. Nvidia makes Blackwell chips on a custom-built TSMC 4NP process ⁴. Epoch AI estimates \$17,000 for a 12-inch (300 mm) wafer on that process ¹.
- **Dies per wafer.** A wafer is a circle and dies are rectangles, so the edge of the disc goes to waste, and the bigger the die, the fewer fit. Each of the two compute dies in a B200 is about 800 mm² ¹. Nvidia calls them reticle-limited, meaning near the largest a scanner can print in one shot ⁴.
- **Yield.** Defects land at random, so a bigger die is likelier to catch one. Epoch AI models the Blackwell die at 40 to 70 percent good, centered on 60 ¹.

Those three numbers put the two dies inside a B200 at about \$900 of the roughly \$6,400 build ¹. The estimate counts only variable costs and leaves out fixed costs such as research and development ¹.

Variants and trade-offs

Memory is the largest line

The 192 GB of high-bandwidth memory beside those dies, sold as HBM3E, is the single largest line, about \$2,900 at \$14 to \$17 per gigabyte ¹. Epoch AI notes that HBM pricing is negotiated individually and can vary significantly by volume and contract length ¹. The \$14 to \$17 range dates from December 2025, before the 2026 rise in memory makers' sales and margins described below ⁵. Epoch AI says memory accounts for half of the roughly \$6,400 build ¹. Three firms, SK hynix, Samsung and Micron, dominate the world market for that memory ³. SK hynix says demand for its products has exceeded its available supply in recent quarters ⁶.

4 NVIDIA Blackwell Architecture. Nvidia · 18 December 2025 [\[A\]](https://nvidia.com/en-us/data-center/technologies/blackwell-architecture) nvidia.com/en-us/data-center/technologies/blackwell-architecture

1 NVIDIA's B200 costs around \$6,400 to produce. Epoch AI · 10 December 2025 [\[A\]](https://epoch.ai/data-insights/b200-cost-breakdown) epoch.ai/data-insights/b200-cost-breakdown

5 SK hynix Announces 2Q26 Financial Results. SK hynix [\[A\]](https://news.skhynix.com/en/q2-2026-business-results) news.skhynix.com/en/q2-2026-business-results

3 Understanding the Biden Administration's Updated Export Controls. Center for Strategic and International Studies · 11 December 2024 [\[A\]](https://csis.org/analysis/understanding-biden-administrations-updated-export-controls) csis.org/analysis/understanding-biden-administrations-updated-export-controls

6 SK hynix Inc., Form 424B4 prospectus for the period ended 2026-07-10 (424(B)(4)). U.S. Securities and Exchange Commission (filing by SK hynix Inc.) · 10 July 2026 [\[A\]](https://sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm) sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm

Packaging, substrate and test

CoWoS-L, the TSMC process that mounts dies and memory on one carrier and wires them together, adds about \$1,100, more than the logic dies it carries ¹. Epoch AI models packaging yield at 65 to 95 percent ¹. A package that fails testing loses its logic dies and memory stacks, and spreading that loss over the good units adds about \$1,000 to each B200 ¹. Power delivery hardware, the circuit board, and final assembly and testing add \$480 ¹. See Advanced packaging for why packaging capacity runs out first.

The B200 bill of materials

LINE	ESTIMATE	RANGE
HBM3E, 192 GB	\$2,900	\$2,800-3,100
CoWoS-L packaging	\$1,100	\$1,000-1,200
Packaging yield loss	\$1,000	\$430-1,700
Logic die, two on TSMC 4NP	\$900	\$720-1,200
Power delivery, board, assembly and test	\$480	\$370-600
Manufacturing cost	~\$6,400	\$5,700-7,300
Reported selling price per chip, March 2024	\$30,000-40,000	
Nvidia compute revenue per GPU in GB200 racks, data to October 2025	\$33,000-42,000	

Epoch AI models each line as a range, deriving the packaging line from TSMC's advanced packaging revenue and Nvidia's share of CoWoS capacity ¹. The estimate covers the accelerator module only and leaves out servers and rack-scale systems ¹. Epoch AI notes that most Blackwell revenue comes from those systems, which may carry lower margins, so Nvidia's realized margin on Blackwell may be lower than the gap between this cost and the reported chip price suggests ¹.

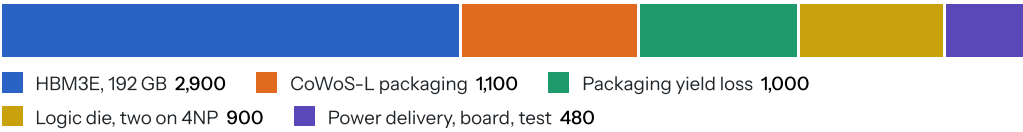
The B200 is used here because Epoch AI's line-by-line estimate covers it. In its results for the quarter to July 2026, Nvidia said its Vera Rubin platform was ramping into full production ⁷. Each Rubin GPU carries up to 288 GB of HBM4, a newer generation of the stacked memory ⁸.

1 NVIDIA's B200 costs around \$6,400 to produce. Epoch AI · 10 December 2025 epoch.ai/data-insights/b200-cost-breakdown

7 NVIDIA Announces Financial Results for Second Quarter Fiscal 2027. Nvidia · 26 August 2026 nvidianews.nvidia.com/news/nvidia-announces-financial-results-for-second-quarter-fiscal-2027

8 Inside NVIDIA Rubin GPU Architecture: Powering the Era of Agentic AI. Nvidia · 21 July 2026 developer.nvidia.com/blog/inside-nvidia-rubin-gpu-architecture-powering-the-era-of-agentic-ai

Where the ~\$6,400 of B200 manufacturing cost goes, Epoch AI estimate, December 2025 \$



Source: Epoch AI B200 cost model, from a \$17,000 4NP wafer, 40-70% die yield, \$14-17 per GB of memory, and a packaging line derived from TSMC's advanced packaging revenue

From package to rack to cluster

At rack scale the number that matters is the cost of a GPU-hour. For an operator that owns the machine, SemiAnalysis puts a Vera Rubin NVL72 at \$3.57, against \$1.84 for a GB200 and \$2.36 for a GB300 ⁹. Each generation costs its owner more per hour than the last, yet SemiAnalysis, working from early CoreWeave results on DeepSeek R1 that it has not verified, finds Rubin cheaper per token than GB200 and GB300 at every interactivity level it compared ⁹.

One level up, a 100,000 H100 cluster costs over \$4 billion in servers, needs more than 150 MW of data center capacity, uses 1.59 TWh a year, costs \$123.9 million a year in power at \$0.078 per kWh, and in a rail-optimized design links its GPUs to leaf switches with 98,304 optical transceivers ¹⁰.

Who captures the value

FIRM	STAGE	QUARTER ENDED	Gross margin
Micron	HBM and DRAM	September 2026	86.8%

9 Vera Rubin NVL72 vs GB200 NVL72? Inference TCO & Architecture Analysis. SemiAnalysis · 23 July 2026 [B](https://inference.semianalysis.com/blog/vera-rubin-nvl72-vs-gb200-nvl72-inference)
inference.semianalysis.com/blog/vera-rubin-nvl72-vs-gb200-nvl72-inference

10 100,000 H100 Clusters: Power, Network Topology, Ethernet vs InfiniBand, Reliability, Failures, Checkpointing. SemiAnalysis · 17 June 2024 [B](https://newsletter.semianalysis.com/p/100000-h100-clusters-power-network)
newsletter.semianalysis.com/p/100000-h100-clusters-power-network

Nvidia	Accelerator design	July 2026	75.0%
TSMC	Wafers and CoWoS	June 2026	67.7%
KLA	Inspection	June 2026	61.4%
ASML	Lithography	June 2026	54.0%
Lam Research	Etch	June 2026	51.7%
Applied Materials	Deposition	July 2026	50.3%
Ibiden	Substrates	June 2026	36.4%
ASE Technology	Packaging and test segment	June 2026	27.3%
Amkor	OSAT	June 2026	16.8%

Each figure comes from the firm's own earnings release; for KLA and Ibiden it is gross profit divided by revenue, since those releases give no percentage^{11 7 12 13 14 15 16 17 18 19}. For ASE the table shows its packaging and test segment; the company as a whole earned 21.0 percent, because about a third of its revenue came from electronics manufacturing services, which earned 8.9 percent¹⁸.

SK hynix's earnings release gives no gross margin. Its operating margin was 76 percent in the June quarter, on revenue up 257 percent in a year⁵.

11 Default (Micron Technology website). Micron Technology [\[A\]](https://investors.micron.com/news/press-release/2026/Micron-Technology-Inc--Reports-Record-Fiscal-...) investors.micron.com/news/press-release/2026/Micron-Technology-Inc--Reports-Record-Fiscal-...

7 NVIDIA Announces Financial Results for Second Quarter Fiscal 2027. Nvidia · 26 August 2026 [\[A\]](https://nvidianews.nvidia.com/news/nvidia-announces-financial-results-for-second-quarter-fiscal-2027) nvidianews.nvidia.com/news/nvidia-announces-financial-results-for-second-quarter-fiscal-2027

12 TSMC Reports Second Quarter EPS of NT\$27.25. TSMC · 16 July 2026 [\[A\]](https://pr.tsmc.com/english/news/3326) pr.tsmc.com/english/news/3326

13 KLA CORPORATION REPORTS FISCAL 2026 FOURTH QUARTER AND FULL YEAR RESULTS. KLA Corporation · 28 July 2026 [\[A\]](https://ir.kla.com/news-events/press-releases/detail/518/kla-corporation-reports-fiscal-2026-fourth-quarter) ir.kla.com/news-events/press-releases/detail/518/kla-corporation-reports-fiscal-2026-fourth-quarter

14 ASML reports €9.3 billion total net sales and €2.9 billion net income in Q2 2026. ASML · 15 July 2026 [\[A\]](https://asml.com/en/news/press-releases/2026/q2-2026-financial-results) asml.com/en/news/press-releases/2026/q2-2026-financial-results

15 Lam Research Corporation Reports Financial Results for the Quarter Ended June 28, 2026. Lam Research · 29 July 2026 [\[A\]](https://newsroom.lamresearch.com/2026-07-29-Lam-Research-Corporation-Reports-Financial-Results-for-...) newsroom.lamresearch.com/2026-07-29-Lam-Research-Corporation-Reports-Financial-Results-for-...

16 Applied Materials Announces Third Quarter 2026 Results. Applied Materials · 13 August 2026 [\[A\]](https://ir.appliedmaterials.com/news-releases/news-release-details/applied-materials-announces-third-quarter-2026-results) ir.appliedmaterials.com/news-releases/news-release-details/applied-materials-announces-third-quarter-2026-results

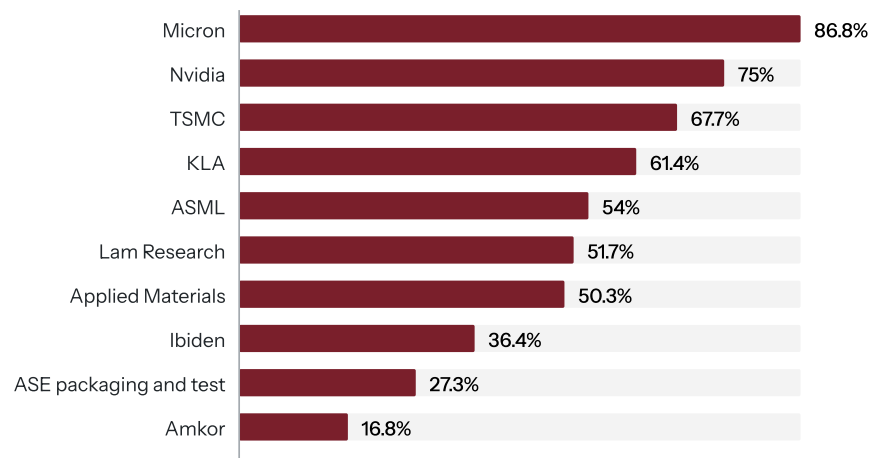
17 Note : This document has been translated from a part of the Japanese original for reference purposes only.. Ibiden · 3 August 2026 [\[A\]](https://ibiden.com/ir/items/tannshinn2026Q1.pdf) ibiden.com/ir/items/tannshinn2026Q1.pdf

18 ASE Technology Holding Co., Ltd. Reports Its Unaudited Consolidated Financial Results for the Second Quarter of 2026. PR Newswire · 30 July 2026 [\[A\]](https://prnewswire.com/news-releases/ase-technology-holding-co-ltd-reports-its-unaudited-consolidated-financial-results-for-the-second-quarter-of-2026) prnewswire.com/news-releases/ase-technology-holding-co-ltd-reports-its-unaudited-consolidated-financial-results-for-the-second-quarter-of-2026

19 AMKOR TECHNOLOGY, INC., Form 8-K current report for the period ended 2026-07-27 (8-K). U.S. Securities and Exchange Commission (filing by AMKOR TECHNOLOGY, INC.) · 27 July 2026 [\[A\]](https://sec.gov/Archives/edgar/data/0001047127/000104712726000043/amkr6302026erex-991.htm) sec.gov/Archives/edgar/data/0001047127/000104712726000043/amkr6302026erex-991.htm

5 SK hynix Announces 2Q26 Financial Results. SK hynix [\[A\]](https://news.skhynix.com/en/q2-2026-business-results) news.skhynix.com/en/q2-2026-business-results

Gross margin, each firm's most recent reported quarter %



Source: Each firm's own quarterly earnings release; quarters end between June and September 2026; ASE's bar is its packaging and test segment (TSMC shown)

In the table, design, equipment and leading-edge wafers earn gross margins of 50.3 to 75.0 percent, substrates 36.4 percent, and assembly and test 16.8 to 27.3 percent. In 2026 Micron passed all of them. Its gross margin rose from 39.8 percent for the year to August 2025 to 86.8 percent in the quarter to September 2026 ¹¹. Nvidia's was 75.0 percent in the quarter to July 2026 ⁷.

The Semiconductor Industry Association, using monthly data compiled by World Semiconductor Trade Statistics, counted \$791.7 billion of global chip sales in 2025 ²⁰. In its June 2026 forecast, World Semiconductor Trade Statistics put 2025 at \$795.6 billion and 2026 at \$1.51 trillion, with memory growing about 250 percent and logic 37 percent ²¹. Other totals include \$135.1 billion of 2025 equipment billings ²² and \$448.2 billion of 2025 capital spending at Alphabet, Amazon, Meta, Microsoft and Oracle, the sum of Epoch AI's quarterly figures, which Epoch says would reach \$770 billion in 2026 if the trend continues ²³. These totals overlap, so they cannot be added together.

11 Default (Micron Technology website). Micron Technology [\[A\]](https://investors.micron.com/news/press-release/2026/Micron-Technology-Inc--Reports-Record-Fiscal-2026) investors.micron.com/news/press-release/2026/Micron-Technology-Inc--Reports-Record-Fiscal-2026

7 NVIDIA Announces Financial Results for Second Quarter Fiscal 2027. Nvidia · 26 August 2026 [\[A\]](https://nvidianews.nvidia.com/news/nvidia-announces-financial-results-for-second-quarter-fiscal-2027) nvidianews.nvidia.com/news/nvidia-announces-financial-results-for-second-quarter-fiscal-2027

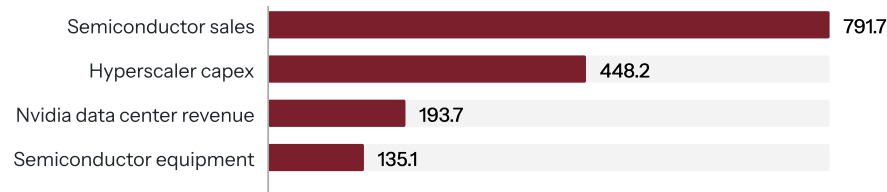
20 Global Annual Semiconductor Sales Increase 25.6% to \$791.7 Billion in 2025 - Semiconductor Industry Association. Semiconductor Industry Association · 6 February 2026 [\[A\]](https://semiconductors.org/global-annual-semiconductor-sales-increase-25-6-to-791-7-billion-in-2025) semiconductors.org/global-annual-semiconductor-sales-increase-25-6-to-791-7-billion-in-2025

21 San Jose, California - June 2, 2026, 06:00 UTC. World Semiconductor Trade Statistics · 1 June 2026 [\[A\]](https://wsts.org/esraCMS/extension/media/f/WST/7618/WSTS_FC-Release-2026-May.pdf) wsts.org/esraCMS/extension/media/f/WST/7618/WSTS_FC-Release-2026-May.pdf

22 SEMI Reports Global Semiconductor Equipment Billings Reached \$135 Billion in 2025, Up 15% Year-on-Year. SEMI · 7 April 2026 [\[A\]](https://semi.org/en/SEMI-Reports-Global-Semiconductor-Equipment-Billings-Reached-135-Billion-in-2025) semi.org/en/SEMI-Reports-Global-Semiconductor-Equipment-Billings-Reached-135-Billion-in-2025

23 Hyperscaler capex has quadrupled since GPT-4's release. Epoch AI · 26 February 2026 [\[A\]](https://epoch.ai/data-insights/hyperscaler-capex-trend) epoch.ai/data-insights/hyperscaler-capex-trend

Selected market totals, 2025 \$B



Source: Semiconductor Industry Association on chip sales; Epoch AI quarterly capital spending at Alphabet, Amazon, Meta, Microsoft and Oracle, summed for 2025; Nvidia data center revenue for its fiscal year to January 2026; SEMI on equipment billings

Where the money goes

In the B200, packaging and its scrap, \$1,100 and \$1,000 in Epoch AI's estimate, cost more than twice the \$900 of logic dies ¹. A GB300 NVL72 rack can draw up to 142 kW ²⁴.

The classes below are a judgment of whether each stage's cost falls as volume grows, drawn from the sources in this chapter and the stage chapters.

STAGE	CLASS	WHY
EUV lithography	Structurally expensive	One supplier, ASML. See Lithography.
Masks and pellicles	Structurally expensive	Every design needs its own mask set, and every EUV layer a flawless mask. See Photomasks and pellicles.
Metrology and inspection	Structurally expensive	KLA held about five times its nearest rival's share of these tools in 2025, by CSET's count. See Metrology and inspection.
HBM	Structurally expensive	SK hynix says HBM needs more wafer input than ordinary DRAM. See Memory and HBM.
Advanced packaging, CoWoS-L	Structurally expensive	Modeled packaging yield of 65 to 95 percent; a failed package loses its dies and memory.
ABF substrates	Structurally expensive	Money can add substrate lines, but Ajinomoto said in June 2026 that the insulating film it makes for these substrates has held over 95 percent of its market since launch ²⁵ . See Substrates and PCBs.
Power and cooling plant	Structurally expensive	Grid connections face lengthy queues, and GE Vernova's gas equipment backlog and slot reservations reached 116 GW in mid-2026. See Data centers and power.
Leading-edge logic wafers	Compressible with scale	A very large die yields well only once a process matures. See Transistors and the front end.
Design and EDA	Compressible with scale	A design is paid for once, and its cost is spread across every chip sold. See Chip design, EDA and IP.
Deposition and etch tools	Compressible with scale	Most deposition and etch steps have three or four established tool makers. See Deposition and etch.

1 NVIDIA's B200 costs around \$6,400 to produce. Epoch AI · 10 December 2025 [\[A\]](https://epoch.ai/data-insights/b200-cost-breakdown) epoch.ai/data-insights/b200-cost-breakdown

24 System Hardware & Components. Nvidia [\[A\]](https://docs.nvidia.com/enterprise-reference-architectures/nvl72-ai-factory/latest/components.html) docs.nvidia.com/enterprise-reference-architectures/nvl72-ai-factory/latest/components.html

25 Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto · 30 June 2026 [\[A\]](https://ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList...) ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList...

Optical transceivers	Compressible with scale	Nvidia agreed in March 2026 to invest \$2 billion each in laser makers Coherent and Lumentum, with rights to future capacity. See Systems and networking.
Test and assembly (OSAT)	Already commoditized	Gross margins of 16.8 to 27.3 percent at Amkor and ASE's packaging and test segment, in the table above.
Wafers and bulk gases	Already commoditized	Several firms make approved 300 mm wafers, and the top five served about 75 percent of the market in 2025. See Silicon and wafers.
Rack integration (ODM)	Already commoditized	Several contract manufacturers on three continents assemble racks. See Systems and networking.

Key evaluation criteria

- **Cost per good die.** The wafer price divided by the dies on that wafer that work. A larger die or a lower yield raises it.
- **Memory dollars per gigabyte, and gigabytes per part.** The largest line on the bill, set by three firms.
- **Packaging yield.** Every point lost throws away finished dies and the memory attached to them ¹.
- **Share of the bill the vendor does not control.** Nvidia sets its own margin but buys memory, packaging and substrates at another firm's price.
- **Rack watts.** A GB300 NVL72 rack can draw up to 142 kW, and the data center has to supply and cool all of it ²⁴.
- **Compressibility class.** Whether the line falls when volume doubles. If it does not, capacity is the constraint.

THREE THINGS TO REMEMBER

- Epoch AI estimated in December 2025 that a B200 cost about \$6,400 to build, against a selling price of \$30,000 to \$40,000 per chip reported in March 2024.
- The stacked memory is the most expensive part, about half of the cost.
- Packaging costs more than the logic chips, because a failed package throws away everything inside it.

¹ NVIDIA's B200 costs around \$6,400 to produce. Epoch AI · 10 December 2025 [\[A\] epoch.ai/data-insights/b200-cost-breakdown](https://epoch.ai/data-insights/b200-cost-breakdown)

²⁴ System Hardware & Components. Nvidia [\[A\] docs.nvidia.com/enterprise-reference-architectures/nvl72-ai-factory/latest/components.html](https://docs.nvidia.com/enterprise-reference-architectures/nvl72-ai-factory/latest/components.html)

CHAPTER
17
THE CONTEST

Geopolitics

Every stage in this chain sits in someone's jurisdiction. Since 2018 the United States has been converting that fact into policy, and China has been building substitutes.

IN PLAIN TERMS

An export control is a rule that makes a sale need the government's permission. The government names an item and a buyer, and from then on its own companies must hold a license before they ship that item to that buyer. The American government stretches the rule to cover goods made abroad with American technology. Few governments can use such a rule to much effect, because it works only when their own firms sell something the buyer cannot get elsewhere. The machines, software and chemicals that make an advanced chip come from a short list of firms in the United States, the Netherlands, Japan and South Korea. China can copy the simpler machines within a few years. It cannot yet copy the machine that prints the finest circuits or the chemistry that machine needs, and it has yet to show it can make high-bandwidth memory, the stacked memory beside an AI chip, in volume.

IN SHORT

Since 2022 the United States has restricted sales to China of advanced AI chips and the equipment used to make them, and Japan and the Netherlands have aligned their own controls ¹. China still cannot get extreme ultraviolet (EUV) scanners, the machines behind the most advanced chips, and in September 2025 CSIS judged that EUV remained firmly out of China's reach despite massive state investment ⁷⁴. Below that level, Chinese toolmakers supplied 35 percent of China's own chipmaking equipment market in 2025, up from 10 to 15 percent before 2022 ⁴². In 2022 Taiwan held 69 percent of the world's capacity for making logic chips on processes below 10 nanometers, by the count of the Semiconductor Industry Association and Boston Consulting Group ⁷.

Washington's control regime and Beijing's answer to it are both unfinished.

¹ Where the Chips Fall: U.S. Export Controls Under the Biden Administration from 2022 to 2024. Center for Strategic and International Studies · 12 December 2024 [\[A\] csis.org/analysis/where-chips-fall-us-export-controls-under-biden-administration-2022-2024](https://www.csis.org/analysis/where-chips-fall-us-export-controls-under-biden-administration-2022-2024)

⁷⁴ Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements | Strategic Technologies Blog. Center for Strategic and International Studies [\[A\] csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chines...](https://www.csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chines...)

⁴² China's Localization Drive in Semiconductors Gains Impetus from Allied Chip Export Controls. Center for Strategic and International Studies · 24 March 2026 [\[A\] csis.org/analysis/chinas-localization-drive-semiconductors-gains-impetus-allied-chip-expor...](https://www.csis.org/analysis/chinas-localization-drive-semiconductors-gains-impetus-allied-chip-expor...)

⁷ R AJ VA RA DA RA JA N / I ACOB KOCH -W E SE R / CH RI S RI CH A RD / JOSE P H FI TZ GE RA L D /. Semiconductor Industry Association · 9 May 2024 [\[A\] semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconduc...](https://www.semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconduc...)

The shape of the contest

In September 2022 National Security Advisor Jake Sullivan called securing "as large a lead as possible" in technologies such as AI a national security imperative, and the October rules that followed debuted his doctrine of a small yard with a high fence ¹. Those rules went beyond the old aim of staying two technology nodes ahead of China and tried to push China's capability below its current level ². Licensing once asked who was buying and why. The 2022 rules added where the item was going, with a license required for any advanced AI chip bound for China and for tools bound for Chinese fabs past set technology thresholds ³. Most applications were presumed denied, though equipment for the China fabs of firms headquartered in the United States or allied and partner countries was reviewed case by case ³.

Chokepoints and who holds them

SEGMENT	LEADER	SHARE	BASIS
EUV lithography	Netherlands	100.0%	revenue, 2025
Immersion DUV lithography	Netherlands	99.3%	revenue, 2025
Metrology and inspection	United States	71.7%	revenue, 2025
Deposition	United States	60.3%	revenue, 2025
Etch and clean	United States	52.6%	revenue, 2025
Photoresist	Japan	78%	revenue, 2023
Silicon wafers	Japan	53%	revenue, 2023
Leading-edge logic, below 10 nm	Taiwan	69%	capacity, 2022
Foundry, all nodes	Taiwan	78%	market share, 2025
HBM	South Korea	82.5%	revenue, 2025: SK hynix 63.2, Samsung 19.3, Micron 17.4
Logic chip design	United States	65%	sales, 2022
Mature logic, 28 nm and above	China	33%	capacity, 2022

¹ Where the Chips Fall: U.S. Export Controls Under the Biden Administration from 2022 to 2024. Center for Strategic and International Studies · 12 December 2024 [\[A\] csis.org/analysis/where-chips-fall-us-export-controls-under-biden-administration-2022-2024](https://www.csis.org/analysis/where-chips-fall-us-export-controls-under-biden-administration-2022-2024)

² Choking off China's Access to the Future of AI. Center for Strategic and International Studies · 11 October 2022 [\[A\] csis.org/analysis/choking-chinas-access-future-ai](https://www.csis.org/analysis/choking-chinas-access-future-ai)

³ Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification. Federal Register (Commerce Department; Industry and Security Bureau) · 13 October 2022 [\[A\] federalregister.gov/documents/2022/10/13/2022-21658/implementation-of-additional-export-co...](https://www.federalregister.gov/documents/2022/10/13/2022-21658/implementation-of-additional-export-co...)

- **Equipment.** CSET's ETO Supply Chain Explorer, TechInsights 2025 revenue by parent-company headquarters ⁴.
- **Materials.** Country shares of photoresist and silicon wafers as Japan's Ministry of Economy, Trade and Industry published them in December 2025, from Fuji Keizai's materials survey, by parent-company headquarters ⁵. Japan held 77 percent of photoresist sales in 2021 and 78 percent in 2023, and 52 percent of silicon wafer sales against 53 percent, so neither position is moving.
- **Taiwan.** The 78 percent is the Taiwan Semiconductor Industry Association's 2025 count, as the Stimson Center gives it ⁶. The 69 percent is the Semiconductor Industry Association and Boston Consulting Group's 2022 measurement of logic capacity below 10 nm, the most recent the report gives ⁷. The 92 percent quoted more often is the same measure for 2019, from the two groups' April 2021 report ⁸.
- **Memory.** SK hynix's US listing prospectus splits 2025 high-bandwidth memory revenue between SK hynix at 63.2 percent, Samsung at 19.3 and Micron at 17.4, so Korea holds 82.5; by the first quarter of 2026 Korea was down to 76.9 ⁹. The underlying figures are IDC's, relayed by the prospectus.
- **Design.** CSET's ETO Supply Chain Explorer, from WSTS and SIA figures on 2022 sales of logic chips and microprocessors, still the latest year it gives for this segment ¹⁰. On a wider measure that counts every type of chip, memory and analog included, US-headquartered firms took 53.4 percent of global chip sales in 2025 ¹¹.
- **China's mature nodes.** The 33 percent is the 2022 industry measurement of logic capacity at 28 nm and above, and the same report projects 37 percent by 2032 ⁷. In a February 2025 filing the Semiconductor Industry Association counted every type of chip made at 28 nm and above, memory and analog included, and put China's share of that capacity at 33 percent in 2023, up from 19 percent in 2015 ¹².

Advanced packaging is missing because nobody publishes a capacity split and TSMC will not give one. No country is self-sufficient, so each side's controls can hurt the other.

4 Documentation: Semiconductor Supply Chain Dataset. Tech eto.tech/dataset-docs/chipexplorer

5 METI, Semiconductor and digital industry strategy: future direction (半導体・デジタル産業戦略の今後の方向性), 23 December 2025. Ministry of Economy, Trade and Industry (Japan) · 23 December 2025 [A](https://meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/0014/handeji14-4.pdf) meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/0014/handeji14-4.pdf

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9 SK hynix Inc., Form 424B4 prospectus for the period ended 2026-07-10 (424(B)(4)). U.S. Securities and Exchange Commission (filing by SK hynix Inc.) · 10 July 2026 [A](https://sec.gov/Archives/edgar/data/0002120882/000119312526299963/d32785d424b4.htm) sec.gov/Archives/edgar/data/0002120882/000119312526299963/d32785d424b4.htm

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12 Section 301 Legacy Investigation SIA Comments. Semiconductor Industry Association · 6 February 2025 [A](https://semiconductors.org/wp-content/uploads/2025/02/USTR-2024-0024-00109674-CAT-5016-Public-Docu...) semiconductors.org/wp-content/uploads/2025/02/USTR-2024-0024-00109674-CAT-5016-Public-Docu...

The US export-control campaign, 2018 to today

Commerce built the regime one rule at a time, each closing a gap the last one left.

- **17 August 2020, the Foreign Direct Product Rule.** The Entity List, Commerce's roster of buyers that need a license, cut Huawei and 68 affiliates off from US technology in May 2019¹³, so Huawei bought foreign chips instead. Commerce then extended the rule to any foreign item made with US technology and bound for Huawei¹⁴. That reach makes American controls extraterritorial.
- **7 October 2022, the first country-wide rules.** Two new export classifications, 3A090 and 3B090, capped exportable AI chips and set fab thresholds at FinFET or 16/14 nm logic, 18 nm half-pitch DRAM and 128-layer NAND³. They also required a license for US persons to support chip development or production at those advanced Chinese fabs³.
- **17 October 2023, the density fix.** Nvidia had designed its China-specific chips around the 2022 interconnect-speed threshold, so Commerce's Bureau of Industry and Security (BIS) dropped that parameter and now identifies controlled chips by total processing performance, performance density, and whether they are designed or marketed for data centers¹⁵. A data-center chip now needs a license at 4,800 points of that performance score, or at 1,600 with a density of 5.92¹⁵.
- **2 December 2024, the widest rule.** 24 equipment types, three software tools, the first controls on high-bandwidth memory and 140 Entity List additions¹⁶.
- **15 January 2025, AI Diffusion.** A rule requiring a license for the top band of accelerators, 3A090.a and 4A090.a, to any destination worldwide, then reopening it by exception: License Exception AIA to the nineteen destinations named in supplement no. 5 to part 740, License Exception LPP in capped volumes elsewhere, nothing to China¹⁷. BIS said on 13 May that it would not enforce the framework, two days before the compliance date¹⁸. It withdrew

13 Addition of Entities to the Entity List. Federal Register (Commerce Department; Industry and Security Bureau) · 21 May 2019 [A] [federalregister.gov/documents/2019/05/21/2019-10616/addition-of-entities-to-the-entity-list](https://www.federalregister.gov/documents/2019/05/21/2019-10616/addition-of-entities-to-the-entity-list)

14 Addition of Huawei Non-U.S. Affiliates to the Entity List, the Removal of Temporary General License, and Amendments to General Prohibition Three (Foreign-Produced Direct Product Rule). Federal Register (Commerce Department; Industry and Security Bureau) · 20 August 2020 [A] [federalregister.gov/documents/2020/08/20/2020-18213/addition-of-huawei-non-us-affiliates-t...](https://www.federalregister.gov/documents/2020/08/20/2020-18213/addition-of-huawei-non-us-affiliates-t...)

3 Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification. Federal Register (Commerce Department; Industry and Security Bureau) · 13 October 2022 [A] [federalregister.gov/documents/2022/10/13/2022-21658/implementation-of-additional-export-co...](https://www.federalregister.gov/documents/2022/10/13/2022-21658/implementation-of-additional-export-co...)

15 explainer: The Commerce Department's October 2023 Export Control Update. Center for Security and Emerging Technology (CSET) · 4 December 2023 [A] cset.georgetown.edu/article/bis-2023-update-explainer

16 Commerce Strengthens Export Controls to Restrict China's Capability to Produce Advanced Semiconductors for Military Applications. U.S. Bureau of Industry and Security · 2 December 2024 [A] bis.gov/press-release/commerce-strengthens-export-controls-restrict-chinas-capability-prod...

17 Framework for Artificial Intelligence Diffusion. Federal Register (Commerce Department; Industry and Security Bureau) · 15 January 2025 [A] [federalregister.gov/documents/2025/01/15/2025-00636/framework-for-artificial-intelligence-...](https://www.federalregister.gov/documents/2025/01/15/2025-00636/framework-for-artificial-intelligence-...)

18 Department of Commerce Announces Rescission of Biden-Era Artificial Intelligence Diffusion Rule, Strengthens Chip-Related Export Controls. U.S. Bureau of Industry and Security · 13 May 2025 [A] bis.gov/press-release/department-commerce-announces-rescission-biden-era-artificial-intell...

none of the text. The worldwide license requirement, License Exceptions AIA, ACM and LPP, supplement no. 5 and the 790 million TPP per-country allocation all stand in the Code today, and BIS says it enforces the requirement only against Country Groups D:1, D:4 and D:5 and against firms headquartered in D:5 or Macau^{19,20}. No tiered replacement has appeared; bilateral deals took the place of the caps.

On 9 April 2025 the government told Nvidia it needed a license to ship the H20 to China, to the D:5 group of arms-embargoed countries, and to any company headquartered or ultimately owned there, so no Chinese buyer could route the order through a foreign subsidiary²¹. Nvidia took a \$4.5 billion charge for excess H20 inventory and purchase obligations²². Licenses came back in August 2025, and the same filing says US officials expected the government to receive 15 percent of the revenue from licensed H20 sales, though no regulation codifies that requirement²². Nvidia's annual report for the year to 25 January 2026 put its H20 revenue under those licenses at about \$60 million²³. Beijing restricted those sales, and Nvidia said in its filing for the quarter ended 26 July 2026 that it had been unable to sell its H20 inventory²⁴.

Early 2026 set the current settlement.

- **13 January 2026, effective 15 January.** BIS announced on 13 January that it would move the H200 and AMD MI325X to case-by-case review, on conditions that included independent third-party testing in the United States²⁵. The rule, at 91 FR 1684, took effect on publication two days later and caps exports to China or Macau at 50 percent of the total processing performance of the same chips shipped to US customers²⁶.
- **14 January 2026, effective 15 January.** A national-security proclamation under Section 232 put a 25 percent tariff on the same class of chips and exempted almost every American use, from data centers to startups²⁷. The H200 licenses require each China-bound chip to pass an inspection in the United States before shipment, so every licensed H200 is imported first and pays the tariff²⁴.

19 Enhanced Favorable Treatment for the United Arab Emirates Under the Export Administration Regulations. Federal Register (Commerce Department; Industry and Security Bureau) · 14 July 2026 [\[A\]](https://www.federalregister.gov/documents/2026/07/14/2026-14132/enhanced-favorable-treatment-for-the-u-...) federalregister.gov/documents/2026/07/14/2026-14132/enhanced-favorable-treatment-for-the-u-...

20 15 CFR 742.6, Regional stability. Electronic Code of Federal Regulations [\[A\]](https://www.ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-742/section-742.6) ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-742/section-742.6

21 NVIDIA CORP, Form 8-K current report for the period ended 2025-04-09 (8-K). U.S. Securities and Exchange Commission (filing by NVIDIA CORP) · 15 April 2025 [\[A\]](https://www.sec.gov/Archives/edgar/data/1045810/000104581025000082/nvda-20250409.htm) sec.gov/Archives/edgar/data/1045810/000104581025000082/nvda-20250409.htm

22 NVIDIA CORP, Form 10-Q quarterly report for the period ended 2025-07-27 (10-Q). U.S. Securities and Exchange Commission (filing by NVIDIA CORP) · 27 August 2025 [\[A\]](https://www.sec.gov/Archives/edgar/data/1045810/0001045810250000209/nvda-20250727.htm) sec.gov/Archives/edgar/data/1045810/0001045810250000209/nvda-20250727.htm

23 NVIDIA CORP, Form 10-K annual report for the period ended 2026-01-25 (10-K). U.S. Securities and Exchange Commission (filing by NVIDIA CORP) · 25 February 2026 [\[A\]](https://www.sec.gov/Archives/edgar/data/1045810/0001045810260000021/nvda-20260125.htm) sec.gov/Archives/edgar/data/1045810/0001045810260000021/nvda-20260125.htm

24 NVIDIA CORP, Form 10-Q quarterly report for the period ended 2026-07-26 (10-Q). U.S. Securities and Exchange Commission (filing by NVIDIA CORP) · 26 August 2026 [\[A\]](https://www.sec.gov/Archives/edgar/data/1045810/0001045810260000075/nvda-20260726.htm) sec.gov/Archives/edgar/data/1045810/0001045810260000075/nvda-20260726.htm

25 Department of Commerce Revises License Review Policy for Semiconductors Exported to China. U.S. Bureau of Industry and Security · 13 January 2026 [\[A\]](https://www.bis.gov/press-release/departments-commerce-revises-license-review-policy-semiconductors-exp-...) bis.gov/press-release/departments-commerce-revises-license-review-policy-semiconductors-exp-...

26 Revision to License Review Policy for Advanced Computing Commodities. Federal Register (Commerce Department; Industry and Security Bureau) · 15 January 2026 [\[A\]](https://www.federalregister.gov/documents/2026/01/15/2026-00789/revision-to-license-review-policy-for-...) federalregister.gov/documents/2026/01/15/2026-00789/revision-to-license-review-policy-for-...

27 Adjusting Imports of Semiconductors, Semiconductor Manufacturing Equipment, and Their Derivative Products Into the United States. Federal Register (Executive Office of the President) · 20 January 2026 [\[A\]](https://www.federalregister.gov/documents/2026/01/20/2026-01052/adjusting-imports-of-semiconductors-se-...) federalregister.gov/documents/2026/01/20/2026-01052/adjusting-imports-of-semiconductors-se-...

Nvidia said in its filing for the quarter ended 26 July 2026 that it had been unable to pass any of that tariff on to its customers ²⁴.

- **12 February 2026.** Applied Materials agreed to pay about \$252 million, the statutory maximum, over about \$126 million of ion implanters routed through Korea to an Entity-Listed Chinese customer ²⁸.

Eight rule changes that shaped the regime

- 2019-05-16
Huawei and 68 affiliates added to the Entity List
- 2022-10-07
First country-wide controls on AI chips and fab tools
- 2023-10-17
Performance density added; A800 and H800 captured
- 2024-12-02
24 tool types, HBM controls, 140 entity listings
- 2025-01-15
AI Diffusion rule published, three country tiers
- 2025-05-13
BIS stops enforcing the AI Diffusion rule
- 2025-08-11
US officials seek 15% of licensed H20 sales
- 2026-01-13
H200 and MI325X case-by-case review announced, effective 15 January

Source: BIS press releases, Federal Register rules, a CSET explainer and Nvidia filings, cited in the text

Cloud and remote access

Renting a chip is not exporting it. An export, at 15 CFR 734.13, is a shipment or transmission out of the United States or a release of technology or source code to a foreign person in the United States, so a Singapore data center selling time on an H200 already installed there moves nothing across a border ²⁹.

The American rules reach that trade through the firms holding the chips. A January 2026 license for China or Macau is conditioned on the applicant getting the consignee's know-your-customer procedures and its list of Infrastructure-as-a-Service customers in Belarus, China, Cuba, Iran, Macau, North Korea, Russia and Venezuela, "necessary to prevent unauthorized remote access from end users described in paragraph (dd)(1)(iv)", and on a promise that no algorithm trained on the chips is served back to those users ³⁰.

²⁴ NVIDIA CORP, Form 10-Q quarterly report for the period ended 2026-07-26 (10-Q). U.S. Securities and Exchange Commission (filing by NVIDIA CORP) · 26 August 2026 [\[A\]](https://sec.gov/Archives/edgar/data/1045810/000104581026000075/nvda-20260726.htm) sec.gov/Archives/edgar/data/1045810/000104581026000075/nvda-20260726.htm

²⁸ Applied Materials to Pay \$252 Million Penalty to BIS for Illegally Exporting Semiconductor Manufacturing Equipment. U.S. Bureau of Industry and Security · 11 February 2026 [\[A\]](https://bis.gov/press-release/applied-materials-pay-252-million-penalty-bis-illegally-exporting-se...) bis.gov/press-release/applied-materials-pay-252-million-penalty-bis-illegally-exporting-se...

²⁹ 15 CFR 734.13 -- Export.. Electronic Code of Federal Regulations [\[A\]](https://ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-734/section-734.13) ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-734/section-734.13

³⁰ Federal Register, Volume 91 Issue 10 (Thursday, January 15, 2026). U.S. Government Publishing Office [\[A\]](https://govinfo.gov/content/pkg/FR-2026-01-15/html/2026-00789.htm) govinfo.gov/content/pkg/FR-2026-01-15/html/2026-00789.htm

The diffusion rule addressed the other end, the output. It classified frontier model weights as ECCN 4E091, warned American cloud providers that training such a model for the US subsidiary of a foreign-headquartered customer raises a red flag that the weights will leave without a license, and barred its validated end users from training one outside the nineteen listed destinations without BIS authorization, while saying that API access to a model, and rented capacity for inference, "are not prohibited" ¹⁷.

So the controls reach the chip, frontier model weights, and the promises a licensed consignee signs. Compute sold by the hour on chips lawfully installed abroad sits outside them.

Allies: the Netherlands, Japan, Korea and Europe

Unilateral tool controls would only transfer the sales, so the campaign depends on The Hague and Tokyo.

- **The Netherlands.** The Dutch began licensing advanced deep-ultraviolet tools on 1 September 2023, widened that in September 2024 ³¹ and reached measurement and inspection tools on 1 April 2025 ³².
- **Japan.** Controls on advanced manufacturing equipment took effect on 23 July 2023 and apply to all destinations and name no country ³³.
- **South Korea.** BIS revoked the Validated End-User status that let Samsung's and SK hynix's China subsidiaries and Intel Semiconductor (Dalian) receive US equipment without individual licenses, effective 31 December 2025 ³⁴. BIS said it would license those fabs to keep running, but not to expand capacity or upgrade technology ³⁵. SK hynix, which bought the Dalian fab from Intel, received an annual BIS license in December 2025 to ship approved US equipment to its China fabs during 2026 ³⁶.

A BIS rule effective 29 September 2025 extended Entity List restrictions to any company at least 50 percent owned by one or more listed firms ³⁷. On 30

17 Framework for Artificial Intelligence Diffusion. Federal Register (Commerce Department; Industry and Security Bureau) · 15 January 2025 [\[A\]](https://www.federalregister.gov/documents/2025/01/15/2025-00636/framework-for-artificial-intelligence-...) federalregister.gov/documents/2025/01/15/2025-00636/framework-for-artificial-intelligence-...

31 The Netherlands expands export control measure for advanced semiconductor manufacturing equipment. Government of the Netherlands · 6 September 2024 [\[A\]](https://www.government.nl/latest/news/2024/09/06/the-netherlands-expands-export-control-measure-advanc...) government.nl/latest/news/2024/09/06/the-netherlands-expands-export-control-measure-advanc...

32 Klever: export controls on advanced semiconductor manufacturing equipment to be tightened. Government of the Netherlands · 15 January 2025 [\[A\]](https://www.government.nl/latest/news/2025/01/15/klever-export-controls-on-advanced-semiconductor-manu...) government.nl/latest/news/2025/01/15/klever-export-controls-on-advanced-semiconductor-manu...

33 CSIS Translation: Updated Japanese Export Controls on High-Performance Semiconductor Manufacturing Equipment. Center for Strategic and International Studies · 18 July 2023 [\[A\]](https://www.csis.org/analysis/csis-translation-updated-japanese-export-controls-high-performance-semic...) csis.org/analysis/csis-translation-updated-japanese-export-controls-high-performance-semic...

34 Revocation of Validated End-User Authorizations in the People's Republic of China. Federal Register (Commerce Department; Industry and Security Bureau) · 2 September 2025 [\[A\]](https://www.federalregister.gov/documents/2025/09/02/2025-16735/revocation-of-validated-end-user-autho...) federalregister.gov/documents/2025/09/02/2025-16735/revocation-of-validated-end-user-autho...

35 Department of Commerce Closes Export Controls Loophole for Foreign-Owned Semiconductor Fabs in China. U.S. Bureau of Industry and Security · 29 August 2025 [\[A\]](https://www.bis.gov/press-release/department-commerce-closes-export-controls-loophole-foreign-owned-se...) bis.gov/press-release/department-commerce-closes-export-controls-loophole-foreign-owned-se...

36 SK hynix Inc., Form 424B4 prospectus for the period ended 2026-07-10 (424(B)(4)). U.S. Securities and Exchange Commission (filing by SK hynix Inc.) · 10 July 2026 [\[A\]](https://www.sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm) sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm

37 Expansion of End-User Controls To Cover Affiliates of Certain Listed Entities. Federal Register (Commerce Department; Industry and Security Bureau) · 30 September 2025 [\[A\]](https://www.federalregister.gov/documents/2025/09/30/2025-19001/expansion-of-end-user-controls-to-cove...) federalregister.gov/documents/2025/09/30/2025-19001/expansion-of-end-user-controls-to-cove...

September the Dutch economy minister invoked the Goods Availability Act against Nexperia, the Nijmegen chipmaker that supplies European car lines, citing governance failures that risked moving technology out of Europe ³⁸. Neither lasted: BIS suspended its rule for a year on 10 November ³⁹ and the minister suspended his order on 19 November ⁴⁰. Europe holds a chokepoint at the leading edge and none at the mature nodes its car industry runs on.

The MATCH Act, introduced on 8 April 2026, would ban sales of immersion deep-ultraviolet scanners to China, name CXMT, Hua Hong, Huawei, SMIC and YMTC in statute, and give allies 150 days to match before the US extends the Foreign Direct Product Rule alone ⁴¹.

China's response

Five bodies run Beijing's side. The Ministry of Industry and Information Technology (MIIT) sets substitution targets, and in 2024 reportedly told Chinese telecom operators to strip foreign chips out of their networks by 2027 ⁴². The National Development and Reform Commission (NDRC) plans the compute build-out and co-issued the national computing-power network plan ⁴³. The Ministry of Commerce (MOFCOM) writes and administers the export controls, including the mineral rules below ⁴⁴. The State Administration for Market Regulation (SAMR) is the antitrust authority, and opened its Nvidia investigation in December 2024 ⁴⁵. The Cyberspace Administration of China (CAC) runs the security reviews, and in September 2025 told firms including ByteDance and Alibaba to cancel Nvidia orders ⁴⁶.

The retaliation itself targets the inputs. Micron was first, failing a CAC review on 21 May 2023 and losing its critical infrastructure buyers ⁴⁷. Mineral controls followed.

- **3 December 2024.** Notice 46, from MOFCOM, banned exports of gallium, germanium, antimony and superhard materials to the United States, one day

38 Minister of Economic Affairs invokes Goods Availability Act. Government of the Netherlands · 12 October 2025 [A](https://government.nl/latest/news/2025/10/12/minister-of-economic-affairs-invokes-goods-availabili...)

39 One Year Suspension of Expansion of End-User Controls for Affiliates of Certain Listed Entities. Federal Register (Commerce Department; Industry and Security Bureau) · 12 November 2025 [A](https://federalregister.gov/documents/2025/11/12/2025-19846/one-year-suspension-of-expansion-of-en...)

40 Update on invoking Goods Availability Act. Government of the Netherlands · 19 November 2025 [A](https://government.nl/documents/2025/11/19/update-on-invoking-goods-availability-act)

41 Risch, Ricketts, Kim Introduce MATCH Act; Level the Global Playing Field for U.S. Tech. U.S. Senate Committee on Foreign Relations · 8 April 2026 [A](https://foreign.senate.gov/press/rep/release/risch-ricketts-kim-introduce-match-act-level-the-glob...)

42 China's Localization Drive in Semiconductors Gains Impetus from Allied Chip Export Controls. Center for Strategic and International Studies · 24 March 2026 [A](https://csis.org/analysis/chinas-localization-drive-semiconductors-gains-impetus-allied-chip-expor...)

43 China accelerates building of national computing power network. The State Council of the People's Republic of China · 27 December 2023 [A](https://english.www.gov.cn/news/202312/27/content_WS658b72afc6d0868f4e8e28ba.html)

44 Announcement No.18 of 2025 of The Ministry of Commerce and The General Administration of Customs of The People's Republic of China Announcing the decision to implement export control on some medium and heavy rare earth related items. Ministry of Commerce of the People's Republic of China [A](https://english.mofcom.gov.cn/Policies/AnnouncementsOrders/art/2025/art_Odd87cbee7b045bf93fabe6ab2...)

45 Cyber Week in Review: December 13, 2024. Council on Foreign Relations · 13 December 2024 [A](https://cfr.org/articles/cyber-week-review-december-13-2024)

46 Beijing blocks Nvidia sales in vote of confidence for Chinese chipmakers, the White House strikes a deal for 10 percent of Intel, and Commerce voids a \$7.4B CHIPS Act grant. Center for Security and Emerging Technology (CSET) · 18 September 2025 [A](https://cset.georgetown.edu/newsletter/september-18-2025)

47 Micron Aggression: The Right Response to Beijing's Ban on the U.S. Chipmaker. Center for Strategic and International Studies · 22 June 2023 [A](https://csis.org/analysis/micron-aggression-right-response-beijings-ban-us-chipmaker)

after the American chip rules ⁴⁸.

- **4 April 2025.** Announcement 18 put seven medium and heavy rare earths under licensing, from samarium to yttrium, as metal, oxide, compound or magnet material ⁴⁴.
- **9 October 2025.** A further announcement reached foreign-made goods containing Chinese rare earths worth 0.1 percent or more of their value, putting a Chinese export license between a foreign firm and its own product ⁴⁹. MOFCOM suspended it on 7 November 2025 until 10 November 2026 ⁵⁰.
- **November 2025.** After Trump and Xi met at the Asia-Pacific summit, the ministry suspended the gallium ban for a year ⁵¹.

Nothing was repealed; the gallium ban and the October rules are paused, and the April licensing regime stands.

The blunter instrument is demand. Chinese regulators discouraged customers from buying, importing or using Nvidia's data-center products, and endorsed performance-per-watt and bandwidth standards for accelerators in Chinese data centers ²⁴. When Washington licensed H200 sales in February 2026, Beijing restricted them, and Nvidia's shipments came to less than 1 percent of data-center revenue ²⁴. That quarter's data-center revenue was \$89.0 billion, and the next quarter's guidance assumed no China compute revenue ⁵².

Chinese tool vendors held 10 to 15 percent of their home market before 2022, took 25 percent in 2024 and 35 percent in 2025, and hold about 40 percent of domestic etch and deposition ⁴². At ASML, China's share of net system sales fell from 41 percent in 2024 to 33 percent in 2025 ⁵³.

48 Ministry of Commerce Notice 2024 No. 46: Notice Concerning Strengthening Controls on Exports of Relevant Dual-Use Items to the United States. Center for Security and Emerging Technology (CSET) · 3 December 2024 [\[A\]](https://cset.georgetown.edu/publication/china-rare-earth-export-ban)
cset.georgetown.edu/publication/china-rare-earth-export-ban

44 Announcement No.18 of 2025 of The Ministry of Commerce and The General Administration of Customs of The People's Republic of China Announcing the decision to implement export control on some medium and heavy rare earth related items. Ministry of Commerce of the People's Republic of China [\[A\]](https://english.mofcom.gov.cn/Policies/AnnouncementsOrders/art/2025/art_Odd87cbee7b045bf93fabe6ab2...)
english.mofcom.gov.cn/Policies/AnnouncementsOrders/art/2025/art_Odd87cbee7b045bf93fabe6ab2...

49 Ministry of Commerce Notice 2025 No. 61: Announcement of the Decision to Implement Controls on Exports of Rare Earth-Related Items to Foreign Countries. Center for Security and Emerging Technology (CSET) · 9 October 2025 [\[A\]](https://cset.georgetown.edu/publication/mofcom-notice-2025-61)
cset.georgetown.edu/publication/mofcom-notice-2025-61

50 MOFCOM and GAC Announcement 2025 No. 70, suspending the October 2025 export-control measures, Announcements Nos. 55 to 58, 61 and 62 (商务部、海关总署公告2025年第70号). Ministry of Commerce of the People's Republic of China · 7 November 2025 [\[A\]](https://mofcom.gov.cn/zwgk/zcfb/art/2025/art_blec77dd3f0d4762952904df7cdaadec.html)
mofcom.gov.cn/zwgk/zcfb/art/2025/art_blec77dd3f0d4762952904df7cdaadec.html

51 The U.S.-China Trade Truce Has Not Solved the Gallium Problem. Center for Strategic and International Studies · 11 May 2026 [\[A\]](https://csis.org/analysis/us-china-trade-truce-has-not-solved-gallium-problem)
csis.org/analysis/us-china-trade-truce-has-not-solved-gallium-problem

24 NVIDIA CORP, Form 10-Q quarterly report for the period ended 2026-07-26 (10-Q). U.S. Securities and Exchange Commission (filing by NVIDIA CORP) · 26 August 2026 [\[A\]](https://sec.gov/Archives/edgar/data/1045810/000104581026000075/nvda-20260726.htm)
sec.gov/Archives/edgar/data/1045810/000104581026000075/nvda-20260726.htm

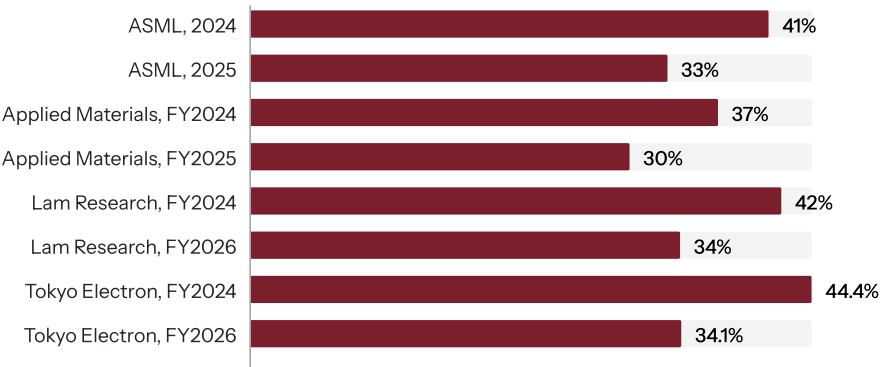
52 NVIDIA Announces Financial Results for Second Quarter Fiscal 2027. Nvidia · 26 August 2026 [\[A\]](https://nvidianews.nvidia.com/news/nvidia-announces-financial-results-for-second-quarter-fiscal-2027)
nvidianews.nvidia.com/news/nvidia-announces-financial-results-for-second-quarter-fiscal-2027

42 China's Localization Drive in Semiconductors Gains Impetus from Allied Chip Export Controls. Center for Strategic and International Studies · 24 March 2026 [\[A\]](https://csis.org/analysis/chinas-localization-drive-semiconductors-gains-impetus-allied-chip-expor...)
csis.org/analysis/chinas-localization-drive-semiconductors-gains-impetus-allied-chip-expor...

53 Presentation Investor Relations Q4 2025. ASML · 27 January 2026 [\[A\]](https://ourbrand.asml.com/m/3136300aa4999bc1/original/2026_01_28_Presentation-Investor-Relations-Q...)
ourbrand.asml.com/m/3136300aa4999bc1/original/2026_01_28_Presentation-Investor-Relations-Q...

Substitution stalls at the leading edge. Without extreme-ultraviolet scanners, SMIC's most advanced process, N+3, reaches the density of TSMC's 6 nm-class process by printing its tightest layers in several passes on deep-ultraviolet tools and by redesigning its standard cells ⁵⁴. In September 2025 SemiAnalysis expected Huawei to ship about 805,000 Ascend units in 2025, with dies made by both TSMC and SMIC ⁵⁵. It judged memory the binding constraint. By its count, a stockpile of roughly 13 million memory stacks, most bought before the December 2024 rules took effect, was enough for about 1.6 million Ascend 910C packages, and it expected CXMT, China's own memory maker, to make only about 2 million stacks in 2026, enough for 250,000 to 300,000 more ⁵⁵. Huawei said in September 2025 that its Ascend 950 chips would carry high-bandwidth memory of its own design, HiBL 1.0 on the 950PR due in the first quarter of 2026 and HiZQ 2.0 on the 950DT due in the fourth quarter, and it gave no figure for how much of that memory it would make ⁵⁶.

China's share of revenue at the four largest chip-tool makers, peak fiscal year and latest %



Source: ASML Q4 2025 investor presentation, Applied Materials and Lam Research 10-K filings, Tokyo Electron Q4 FY2026 results

Industrial policy: CHIPS, Rapidus, Big Fund and the rest

The CHIPS and Science Act authorized about \$52.7 billion ⁴². By July 2025 Commerce had awarded \$30.9 billion of direct funding to 19 companies for 40 projects, a median 14.2 percent of each project's capital cost ⁵⁷. Commerce counted a federal tax credit, the Advanced Manufacturing Investment Credit, when it sized those grants ⁵⁷. Since the One Big Beautiful Bill Act of 2025, the

54 Is SMIC N+3's Metal Pitch Smaller than Intel 18A's?. SemiAnalysis · 14 June 2026 [B] newsletter.semianalysis.com/p/steel-smic-n3-teardown

55 Huawei Ascend Production Ramp: Die Banks, TSMC Continued Production, HBM is The Bottleneck. SemiAnalysis · 8 September 2025 [B] newsletter.semianalysis.com/p/huawei-ascend-production-ramp

56 Groundbreaking SuperPoD Interconnect: Leading a New Paradigm for AI Infrastructure - Huawei. Huawei · 18 September 2025 [A] huawei.com/en/news/2025/9/hc-xu-keynote-speech

42 China's Localization Drive in Semiconductors Gains Impetus from Allied Chip Export Controls. Center for Strategic and International Studies · 24 March 2026 [A] csis.org/analysis/chinas-localization-drive-semiconductors-gains-impetus-allied-chip-expor...

57 GAO-26-107882, SEMICONDUCTORS: Information on Projects Funded to Strengthen U.S. Supply Chain. U.S. Government Accountability Office [A] files.gao.gov/reports/GAO-26-107882/index.html

credit covers 35 percent of qualified investment in an advanced chip plant placed in service after 2025, up from 25 percent ⁵⁷.

On 22 August 2025 the government converted \$5.7 billion of unpaid Intel grants and \$3.2 billion of Secure Enclave defense money into an \$8.9 billion purchase of Intel stock, equivalent to a 9.9 percent stake ⁵⁸.

Tariffs became the second instrument. The 2026 US-Taiwan trade agreement cuts the reciprocal tariff on Taiwanese goods to 15 percent in exchange for at least \$250 billion of Taiwanese investment in US chip production ⁵⁹. On 16 July 2026 TSMC announced another \$100 billion for four more Arizona fabs at 2 nm or more advanced, bringing its total Arizona investment to \$265 billion ⁶⁰.

The European Commission says the EU still depends on other countries for advanced chip manufacturing, and its Chips Act 2.0 proposal, adopted on 3 June 2026, adds measures to support advanced chip production in the EU ⁶¹. Japan backs a national champion instead. Rapidus began prototyping 2 nm gate-all-around transistors at its IIM-1 plant in July 2025 and measured their first electrical characteristics ⁶². In February 2026 it raised another 267.6 billion yen, about \$1.7 billion, from a government agency and 32 companies, aiming for 2 nm mass production by 2027 ⁶³. By June 2026 it had raised 424.95 billion yen in equity, the latest 150 billion yen from a state agency ⁶⁴.

China spends more, and differently. The latest round of its National Integrated Circuit Industry Investment Fund, the Big Fund, reached \$47 billion ⁶⁵. CSIS puts cumulative state funding since 2014 at an estimated \$150 billion and calls the CHIPS Act substantially smaller in scale ⁴². The money has produced a domestic tool industry and no leading-edge node.

57 GAO-26-107882, SEMICONDUCTORS: Information on Projects Funded to Strengthen U.S. Supply Chain. U.S. Government Accountability Office [\[A\]](https://files.gao.gov/reports/GAO-26-107882/index.html) files.gao.gov/reports/GAO-26-107882/index.html

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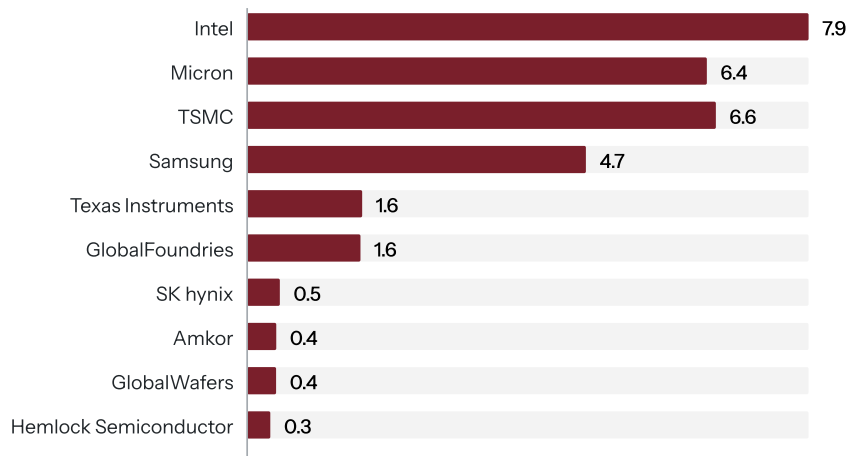
63 Rapidus Secures 267.6 Billion Yen in Funding from Japan Government and Private Sector Companies This strategic funding plan will enable Rapidus to steadily progress from its current R&D phase to mass production of 2nm logic semiconductors by 2027 - Information - Rapidus Corporation. Rapidus [\[A\]](https://www.rapidus.inc/en/news_topics/information/rapidus-secures-267-6-billion-yen-in-funding-from-j...) rapidus.inc/en/news_topics/information/rapidus-secures-267-6-billion-yen-in-funding-from-j...

64 Rapidus Completes 150 Billion Yen Funding Round from Japan Government - Information - Rapidus Corporation. Rapidus [\[A\]](https://www.rapidus.inc/en/news_topics/information/20260605-2) rapidus.inc/en/news_topics/information/20260605-2

65 China's Evolving Industrial Policy for AI. RAND Corporation · 26 June 2025 [\[A\]](https://www.rand.org/pubs/perspectives/PEA4012-1.html) rand.org/pubs/perspectives/PEA4012-1.html

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CHIPS Act direct funding awarded, by firm, as of July 2025 \$B



Source: GAO-26-107882, Semiconductors: Information on Projects Funded to Strengthen U.S. Supply Chain

Taiwan

Taiwan is the concentration risk that no policy has reduced. Its foundries hold 78 percent of the world's contract chipmaking on the industry association's 2025 count, and TSMC makes its 2 nm chips only in Taiwan ⁶. Below 10 nm the island held 69 percent of the world's logic capacity in 2022, on a 2024 count by the Semiconductor Industry Association and Boston Consulting Group ⁷. The packaging is on the island too. Asked in October 2025 how much CoWoS capacity he would add, TSMC's chairman said only that it was "working very hard to narrow the gap between the demand and supply", with wafer and packaging capacity both "very tight" ⁶⁶.

The silicon shield argument holds that this concentration deters invasion: destroying TSMC would cost an aggressor more than the island is worth. The counterargument is that staying irreplaceable gives Taipei reason to slow the diversification Washington wants. Taiwan's rules keep TSMC's newest process at home first, so what TSMC builds in Arizona has run a generation behind what it builds in Taiwan, and Stimson expected 2 nm production there in 2028 at the earliest ⁶. TSMC said in October 2025 that it was "preparing to upgrade our technologies faster to N2 and more advanced process technologies in Arizona" ⁶⁶. In July 2026 it announced four more fabs there at 2 nm or more advanced ⁶⁰.

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66 Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 October 2025 [A] investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2025-10/6860312f04fd291d0f26b...

60 TSMC Announces Additional \$100 Billion Investment In Arizona. City of Phoenix · 16 July 2026 [A] phoenix.gov/newsroom/ced-news/tsmc-announces-additional--100-billion-investment-in-arizona...

Arizona narrows the gap in wafers, and TSMC has two advanced packaging fabs planned there ⁶⁶. But a fab without its Taiwanese mask shops, chemical suppliers and trained crews is not a substitute. The shield is real and weakening, and diversification is not keeping up.

Where the chips go: the Gulf, Southeast Asia, and smuggling

The Gulf has been let inside the controls. In November 2025 Commerce authorized G42 of the United Arab Emirates and HUMAIN of Saudi Arabia to buy up to 35,000 Nvidia GB300s each under security and reporting conditions ⁶⁷. On 10 July 2026 it moved the Emirates from Country Groups D:3 and D:4 into A:5, the tier that holds Washington's close allies, and named the Emirati government alongside G42 and US-headquartered AI companies as consignees who can take controlled AI chips and systems without a license. Licenses survive for the top-tier items, 3A090.a and 4A090.a, so the favorable treatment is tied to the named buyers ¹⁹. Saudi Arabia still works license by license.

Southeast Asia is where chips get past the controls. Since 14 July 2025 Malaysia has required a permit to export, tranship or transit any high-performance US-origin AI chip, plus 30 days' notice under its Strategic Trade Act ⁶⁸. On 25 March 2026 the Justice Department announced charges against three people accused of using the names of Thai companies to order servers with export-controlled chips for China, including a \$170 million order that was never completed ⁶⁹.

The House select committee on China cites estimates that a median 140,000 chips were smuggled to China in 2024 ⁷⁰. Congress's answer, the Chip Security Act, would require location verification on controlled chips within 180 days of enactment ⁷¹. The House Foreign Affairs Committee passed it 42-0 on 26 March 2026 ⁷²; it has not become law.

Who gains and who pays

- **Taiwan and Korea.** Nothing in the policy mix moves leading-edge logic, memory stacking or advanced packaging off an island and a peninsula before 2030; reshoring adds capacity elsewhere without subtracting it there.

66 Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 October 2025 [A](https://investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2025-10/6860312f04fd291d0f26b...)

67 Statement on UAE and Saudi Chip Exports. U.S. Department of Commerce · November 2025 [A](https://commerce.gov/news/press-releases/2025/11/statement-uae-and-saudi-chip-exports)

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68 EXPORT, TRANSSHIPMENT AND TRANSIT OF HIGH-PERFORMANCE AI CHIPS OF US ORIGIN. Ministry of Investment, Trade and Industry (Malaysia) · 14 July 2025 [A](https://miti.gov.my/miti/resources/Media%20Release/%5BFINAL%5D_MITI_Press_Stmt_Malaysia_Regulates...)

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71 S.1705 – Chip Security Act, 119th Congress (2025-2026), bill text. U.S. Congress (Congress.gov, Library of Congress) [A](https://congress.gov/bill/119th-congress/senate-bill/1705/text)

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- **The Netherlands and Japan.** Their tool makers build the controlled machines, so they gain a say in who gets what, while China counts for less of their sales. Tokyo Electron's China share fell from 44.4 percent in the year to March 2024 to 34.1 percent in the year to March 2026, and the company said the share dropped to 26.8 percent in the quarter to March 2026 because spending on leading-edge chips grew faster than spending on older ones ⁷³.
- **The United States.** Its firms took 65 percent of the world's logic chip sales in 2022 ¹⁰. Counting every type of chip, they took 53.4 percent of global sales in 2025, their highest share since 1984 ¹¹. Commerce expects the CHIPS-funded projects to lift the US share of global leading-edge logic chip manufacturing from 0 percent in 2022 to 20 percent by 2030 ⁵⁷.
- **China.** Mature nodes, sub-leading-edge tools, DRAM and NAND are going domestic on a visible timetable. Extreme-ultraviolet machines, their resist and high-bandwidth memory at scale are not, and in September 2025 SemiAnalysis expected China, without smuggled memory, to make fewer Ascends in 2026 than in 2025 ⁵⁵.

The Gulf gains without making anything, since named Emirati buyers can now receive advanced computing items without a license ¹⁹. And Washington's instruments now reach past licensing. Every licensed H200 bound for China pays a 25 percent tariff on its way through US inspection ²⁴. The government agreed in August 2025 to take a 9.9 percent stake in Intel ⁵⁸. Sales of the H200 to China pass through a case-by-case queue ²⁶.

What to watch

- **November 2026.** Whether China renews the one-year suspension of its gallium ban or lets it expire ⁵¹.

73 Investor Relations / April 30, 2026. Tokyo Electron · 30 April 2026 [\[A\]](https://tel.com/ir/library/report/pjuomj00000000tf-att/fy26q4transcript-e.pdf) tel.com/ir/library/report/pjuomj00000000tf-att/fy26q4transcript-e.pdf

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- **The MATCH Act's 150-day deadline.** If it passes, allied divergence on deep-ultraviolet tools gets a statutory deadline ⁴¹.
- **CXMT's memory ramp.** In September 2025 SemiAnalysis judged that domestic memory would cap Chinese accelerator volume before logic wafers did ⁵⁵.
- **SMIC's advanced-node ramp.** In September 2025 SemiAnalysis conservatively estimated SMIC's capacity at 7 nm and below at 45,000 wafers a month by the end of 2025, 60,000 in 2026 and 80,000 in 2027 ⁵⁵. SMIC makes those wafers without extreme-ultraviolet machines, so its tightest layers need several passes ⁵⁴. Yield is the open question.
- **Arizona's lag.** How far Arizona's newest process stays behind Taiwan's as TSMC's four new fabs there, at 2 nm or more advanced, start production ⁶⁰.

FIVE THINGS TO REMEMBER

- An export control works only when a country's firms sell something the buyer cannot get elsewhere.
- US controls also cover foreign goods made with American technology.
- The controls have kept China below the leading edge, and Chinese toolmakers supplied 35 percent of their home equipment market in 2025.
- China's share of Dutch and Japanese toolmakers' sales has fallen since 2024.
- Taiwan held 69 percent of the world's logic capacity below 10 nm in 2022, and TSMC makes its 2 nm chips only there.

⁴¹ Risch, Ricketts, Kim Introduce MATCH Act; Level the Global Playing Field for U.S. Tech. U.S. Senate Committee on Foreign Relations · 8 April 2026 [\[A\]](https://foreign.senate.gov/press/rep/release/risch-ricketts-kim-introduce-match-act-level-the-glob...) foreign.senate.gov/press/rep/release/risch-ricketts-kim-introduce-match-act-level-the-glob...

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⁵⁴ Is SMIC N+3's Metal Pitch Smaller than Intel 18A's? SemiAnalysis · 14 June 2026 [\[B\]](https://newsletter.semianalysis.com/p/steel-smic-n3-teardown) newsletter.semianalysis.com/p/steel-smic-n3-teardown

⁶⁰ TSMC Announces Additional \$100 Billion Investment In Arizona. City of Phoenix · 16 July 2026 [\[A\]](https://phoenix.gov/newsroom/ced-news/tsmc-announces-additional--100-billion-investment-in-arizona...) phoenix.gov/newsroom/ced-news/tsmc-announces-additional--100-billion-investment-in-arizona...

Made by **Yashvardhan Sharma** with Claude. Corrections and questions: contact@chipsupplychain.org.

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A company filings, governments, standards bodies, universities and research institutions; **B** SemiAnalysis, Reuters, the Financial Times and Nikkei Asia.

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  note = {Accessed 2026-10-02}
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