

Chapter 11: Advanced Packaging

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3 Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip production in 2025. Epoch AI · 12 March 2026

epoch.ai/data-insights/ai-chip-supply-chain-constraints

1 Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. LSEG

StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 July 2026 · p. 10 [A](#)

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Advanced Packaging

Epoch AI estimates that in 2025 Nvidia, Google, AMD and Amazon used around 90 percent of the capacity for CoWoS, TSMC's packaging for AI chips.

IN PLAIN TERMS

Packaging joins finished chips into one component and mounts them on a small circuit board, called a substrate, wired far more coarsely than the chips themselves. A lithography machine, which prints a chip's circuits, can cover only a rectangle about the size of a postage stamp in one shot. Many leading accelerators, Nvidia's Blackwell among them, need more logic than fits in that rectangle. So they are built from several chips, called dies, set side by side on an interposer, a layer of much finer wiring that links them and sits on the substrate. Stacks of memory chips sit on the same interposer, a few millimeters away. The interposer is either one piece of silicon or layers of fine copper wiring that often carry small silicon bridges where the links are densest. Silicon expands less than the resin beneath it when heated, so the package can warp and its joints crack. Preventing that in high volume is hard. Nvidia, Google, AMD and Amazon all use TSMC's version, called CoWoS, made in Taiwan.

IN SHORT

Epoch AI estimates that in 2025 Nvidia used 60.3 percent of all capacity for CoWoS, TSMC's interposer packaging ³. On the July 2026 earnings call, TSMC's chief executive, C.C. Wei, said its packaging capacity was so tight that it limited customers' growth ¹. Asked about Intel's EMIB-T packaging, he said he hoped it would take some of the load off TSMC ¹.

In a TrendForce ranking by 2024 revenue, which CSET cites, four of the top ten outsourced firms that package and test chips are headquartered in China ¹². But in 2025 Chinese firms had 5.3 percent of the market for advanced packaging fabrication tools, against 65.8 percent for US firms, by CSET's analysis of TechInsights data ¹¹.

3 Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip production in 2025. Epoch AI · 12 March 2026

[\[A\] epoch.ai/data-insights/ai-chip-supply-chain-constraints](https://epoch.ai/data-insights/ai-chip-supply-chain-constraints)

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08/3e494f0c14dd0890f897aa044415e21d93486cc4/TSMC%202Q26%20Transcript.pdf#page=10

12 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology (CSET) · 14 July 2025 [\[A\]](#)

cset.georgetown.edu/article/inside-beijings-chipmaking-offensive/

11 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 20 October 2026 [\[A\]](#)

chipexplorer.eto.tech/?parentNode=N69&selectedNode=N109

CHOKEPOINT CARD		EXTREME CONCENTRATION
		MODERATELY HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY	
Extreme	Moderate Rated on CoWoS capacity, which TSMC said in July 2026 was so tight that it limited its customers' growth ¹ .	
	PRICE OR MARKET SIZE	
	About \$1,100 for the CoWoS-L packaging of one Nvidia B200, against about \$900 for its two logic dies, by Epoch AI's December 2025 estimate ²	
WHO LEADS	TW TSMC CoWoS packaging used by Nvidia, Google, AMD and Amazon in 2025³ US Intel Foveros 3D packaging in volume at Rio Rancho, New Mexico, since January 2024⁴ TW ASE Technology NT\$389.2B assembly, test and materials revenue, 2025⁵ US Amkor \$6.71B net sales, 2025⁶ CN JCET RMB 38.87B revenue, 2025⁷ SG ASMPT Thermocompression bonders, with \$532.1M of advanced packaging revenue in 2025⁸	
WHERE IT IS MADE	TW Taiwan TSMC advanced packaging fabs and a cluster of outsourced assembly and test firms US United States Intel Foveros packaging in volume at Rio Rancho, New Mexico CN China Four of the top ten outsourced assembly and test firms by 2024 revenue are Chinese, in a TrendForce ranking cited by CSET NL Netherlands Besi hybrid bonders JP Japan Disco grinders and dicers	
WHY SUBSTITUTION IS POSSIBLE	CoWoS packaging has been outsourced to assembly firms such as ASE and Amkor before ⁹ . Intel's EMIB is another 2.5D option, and Amazon's Trainium and Google's TPU were adopting it to different degrees as of March 2026 ⁹ . But a newcomer would have to match TSMC, which said in April 2026 that it was producing CoWoS at 5.5 times the area a scanner prints in one shot ¹⁰ .	
WHERE CHINA STANDS		WHERE THE US STANDS
Chinese firms had 5.3 percent of the market for fabrication tools built for advanced packaging in 2025, by CSET's analysis of TechInsights data ¹¹ . Between 2019 and 2024 they gained 5 percentage points of share in test tools but lost share in bonding and other conventional assembly and packaging tools ¹² .		Intel opened Fab 9 in Rio Rancho, New Mexico, in January 2024 to make its Foveros 3D packages in volume ⁴ . Amkor broke ground in October 2025 on a \$7B packaging and test campus in Peoria, Arizona, and expects production to start in early 2028 ¹³ .

¹ Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) – edited transcript. LSEG StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 July 2026 · p. 10 [A](https://investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897aa044415e21d93486cc4/TSMC%202026%20Transcript.pdf#page=10)
investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897aa044415e21d93486cc4/TSMC%202026%20Transcript.pdf#page=10

A lithography scanner prints a rectangle 26 mm by 33 mm, or 858 mm², in one exposure ¹⁴. That area is called the reticle field. Every leading AI accelerator is bigger than that. Packaging is the stage that lets an accelerator be larger than one reticle field, and the packaging method limits how much larger it can be.

How it works

A second reason for the interposer is high bandwidth memory (HBM). An HBM4 stack connects through 2,048 data signals, packed too tightly for a standard resin substrate, so the memory sits beside the logic on the interposer ¹⁵. Even Nvidia's H100, whose single logic die is 814 mm² and fits inside one reticle field, carries five HBM stacks ¹⁶. Epoch AI counts TSMC's CoWoS packaging among the three inputs the H100 needs, along with its logic die and its HBM ³.

CoWoS stands for chip on wafer on substrate, the order in which the parts are joined. For CoWoS-S, TSMC makes a silicon wafer that carries wiring and vertical copper vias but no transistors. Vias are metal-filled holes that join one layer of wiring to the next.

TSMC bonds the logic dies and memory stacks face down onto that wafer with microbumps. These are dots of solder, and each dot is one electrical joint. In Intel's version of this packaging the microbumps sit 36 microns apart, less than

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- 2 NVIDIA's B200 costs around \$6,400 to produce. Epoch AI · 10 December 2025 [\[A\]](https://epoch.ai/data-insights/b200-cost-breakdown) epoch.ai/data-insights/b200-cost-breakdown
 - 3 Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip production in 2025. Epoch AI · 12 March 2026 [\[A\]](https://epoch.ai/data-insights/ai-chip-supply-chain-constraints) epoch.ai/data-insights/ai-chip-supply-chain-constraints
 - 4 Intel Opens Fab 9 in New Mexico. Intel · 24 January 2024 [\[A\]](https://www.intel.com/content/www/us/en/newsroom/news/intel-opens-fab-9-new-mexico.html) www.intel.com/content/www/us/en/newsroom/news/intel-opens-fab-9-new-mexico.html
 - 5 ASE Technology Holding Co., Ltd. Reports Its Unaudited Consolidated Financial Results for the Fourth Quarter and the Full Year of 2025. PR Newswire · 5 February 2026 [\[A\]](https://www.prnewswire.com/news-releases/ase-technology-holding-co-ltd-reports-its-unaudited-consolidated-financial-results-for-the-fourth-quarter-and-the-full-year-of-2025-302679779.html) www.prnewswire.com/news-releases/ase-technology-holding-co-ltd-reports-its-unaudited-consolidated-financial-results-for-the-fourth-quarter-and-the-full-year-of-2025-302679779.html
 - 6 AMKOR TECHNOLOGY, INC., Form 8-K current report for the period ended 2026-02-09 (8-K). U.S. Securities and Exchange Commission (filing by AMKOR TECHNOLOGY, INC.) · 9 February 2026 [\[A\]](https://www.sec.gov/Archives/edgar/data/1047127/000104712726000007/amkr123125erex-991.htm) www.sec.gov/Archives/edgar/data/1047127/000104712726000007/amkr123125erex-991.htm
 - 7 JCET Releases 2025 Annual Report, Posts Record-High Full-Year Revenue and Higher Profit Before Tax. JCET Group · 9 April 2026 [\[A\]](https://www.jcetglobal.com/en/site/news-detail?id=2048) www.jcetglobal.com/en/site/news-detail?id=2048
 - 8 ASMT Announces 2025 Annual Results AI-Driven Structural Growth Underpins Group Performance. ASMT · 4 March 2026 [\[A\]](https://www.asmt.com/en/investor-relations/news-events/asmt-announces-2025-annual-results/) www.asmt.com/en/investor-relations/news-events/asmt-announces-2025-annual-results/
 - 9 The Great AI Silicon Shortage. SemiAnalysis · 12 March 2026 [\[B\]](https://newsletter.semianalysis.com/p/the-great-ai-silicon-shortage) newsletter.semianalysis.com/p/the-great-ai-silicon-shortage
 - 10 TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC · 23 April 2026 [\[A\]](https://pr.tsmc.com/english/news/3302) pr.tsmc.com/english/news/3302
 - 11 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 20 October 2026 [\[A\]](https://chipexplorer.eto.tech/?parentNode=N69&selectedNode=N109) chipexplorer.eto.tech/?parentNode=N69&selectedNode=N109
 - 12 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology (CSET) · 14 July 2025 [\[A\]](https://cset.georgetown.edu/article/inside-beijings-chipmaking-offensive/) cset.georgetown.edu/article/inside-beijings-chipmaking-offensive/
 - 13 Amkor Technology Breaks Ground on New Semiconductor Advanced Packaging and Test Campus in Arizona; Expands Investment to \$7 Billion. Amkor Technology · 6 October 2025 [\[A\]](https://ir.amkor.com/news-releases/news-release-details/amkor-technology-breaks-ground-new-semiconductor-advanced) ir.amkor.com/news-releases/news-release-details/amkor-technology-breaks-ground-new-semiconductor-advanced
 - 14 TWINSCAN NXE:3400C. ASML · Accessed 9 September 2026 [\[A\]](https://www.asml.com/en/products/euv-lithography-systems/twinscan-nxe3400c) www.asml.com/en/products/euv-lithography-systems/twinscan-nxe3400c
 - 15 New JEDEC® SPHBM4 Standard Enables HBM4-Class Bandwidth on Organic Substrates. JEDEC Solid State Technology Association · 13 July 2026 [\[A\]](https://www.jedec.org/news/pressreleases/new-jedec%C2%AE-sphbm4-standard-enables-hbm4-class-bandwidth-organic-substrates) www.jedec.org/news/pressreleases/new-jedec%C2%AE-sphbm4-standard-enables-hbm4-class-bandwidth-organic-substrates
 - 16 NVIDIA Hopper Architecture In-Depth. Nvidia · 22 March 2022 [\[A\]](https://developer.nvidia.com/blog/nvidia-hopper-architecture-in-depth/) developer.nvidia.com/blog/nvidia-hopper-architecture-in-depth/

half a hair's width ¹⁷. Then TSMC cuts the interposer out of the wafer and attaches it to the resin substrate, which later goes onto a circuit board.

One cracked joint can scrap a package holding eight tested HBM stacks and two large, expensive logic dies. Epoch AI estimated in December 2025 that CoWoS-L packaging added about \$1,100 to the cost of building one Nvidia B200, more than the \$900 of its two logic dies ².

Variants and trade-offs

FAMILY	CARRIER	SIZE LIMIT	USED FOR
CoWoS-S	Full silicon interposer	Up to 3.3x reticle	H100-class parts
CoWoS-R	Resin interposer with fine redistribution wiring	Above 3.3x reticle	Cost-sensitive, fewer HBM stacks
CoWoS-L	Redistribution wiring with local silicon bridges	5.5x reticle in production, 9.5x in development	Blackwell, Rubin

2.5D: silicon, RDL and bridges

In 2.5D packaging the chips sit side by side and connect through an interposer or silicon bridges beneath them. TSMC has run CoWoS in volume since 2012 ¹⁸. CoWoS-S has the finest wiring, but its interposer is one unbroken piece of silicon whose yield (the share of interposers that work) falls as the area grows. CoWoS-L replaces that piece of silicon with redistribution layers (RDL) of fine copper wiring and embeds small silicon bridges where the wiring is densest ¹⁹.

Intel's EMIB embeds similar silicon bridges in the resin substrate ¹⁷. SemiAnalysis reported in March 2026 that Amazon's Trainium and Google's TPU were adopting it to different degrees ⁹.

17 Foveros Direct 3D Technology Brief. Intel · 6 February 2026 ^[A] www.intel.com/content/dam/www/central-libraries/us/en/documents/2025-11/foveros-direct-3d-tech-brief.pdf

2 NVIDIA's B200 costs around \$6,400 to produce. Epoch AI · 10 December 2025 ^[A] epoch.ai/data-insights/b200-cost-breakdown

18 TSMC, CoWoS technology page. TSMC · Accessed 9 September 2026 ^[A] 3dfabric.tsmc.com/english/dedicatedFoundry/technology/cowos.htm

19 TSMC 2025 Annual Report, chapter 5. TSMC · 16 April 2026 · p. 3 ^[A] investor.tsmc.com/static/annualReports/2025/english/pdf/2025_tsmc_ar_e_ch5.pdf#page=3

9 The Great AI Silicon Shortage. SemiAnalysis · 12 March 2026 ^[B] newsletter.semianalysis.com/p/the-great-ai-silicon-shortage

Blackwell was the first high-volume design on CoWoS-L, and packaging problems at TSMC and in Nvidia's design limited its supply ²⁰. The bridges that carry the 10 TB/s link between the two logic dies must be placed very precisely ²⁰. The dies, bridges, interposer and substrate also expand at different rates, and that mismatch caused warpage ²⁰.

3D: SoIC and Foveros

Intel's Foveros stacks dies face to face and joins them with solder microbumps ¹⁷. Its newer Foveros Direct drops the solder and bonds the copper pads directly, a method called hybrid bonding ¹⁷. Hybrid bonding joins the insulating layer around the pads as well as the copper, with no bumps in between ²¹. That lets the connections sit far closer together than microbumps allow ¹⁷. TSMC's SoIC also uses hybrid bonding, and AMD's 3D V-Cache processors use it to bond an extra cache die to the processor die ²².

TSMC put SoIC into volume production in 2022, stacking SRAM memory chips on logic wafers ²³. Its 3 nm SoIC entered volume production in 2025 ¹⁹. An A14-on-A14 version, stacking dies made on TSMC's 1.4 nm process, is due in 2029 ¹⁰. It will carry 1.8 times the die-to-die connection density of the 2 nm version ¹⁰.

In a stack the bottom die is the hardest to cool and the top die is the hardest to power. Because of the heat, 3D designs often put cache memory underneath and compute circuits on top.

²⁰ Nvidia's Blackwell Reworked - Shipment Delays & GB200A Reworked Platforms. SemiAnalysis · 4 August 2024 ^[B]
semianalysis.com/2024/08/04/nvidias-blackwell-reworked-shipment/

¹⁷ Foveros Direct 3D Technology Brief. Intel · 6 February 2026 ^[A] www.intel.com/content/dam/www/central-libraries/us/en/documents/2025-11/foveros-direct-3d-tech-brief.pdf

²¹ [Tech Note] Hybrid Bonding: Evolving into a Foundational Technology for Improving Semiconductor Performance. SK hynix · 25 August 2026 ^[A] news.skhynix.com/en/tech-note-series-ep2/

²² Hybrid Bonding Process Flow - Advanced Packaging Part 5. SemiAnalysis · 9 February 2024 ^[B]
newsletter.semianalysis.com/p/hybrid-bonding-process-flow-advanced

²³ TSMC 2022 Annual Report, page 97. TSMC · Accessed 18 October 2026 ^[A]
investor.tsmc.com/static/annualReports/2022/english/ebook/files/basic-html/page97.html

¹⁹ TSMC 2025 Annual Report, chapter 5. TSMC · 16 April 2026 · p. 3 ^[A]
investor.tsmc.com/static/annualReports/2025/english/pdf/2025_tsmc_ar_e_ch5.pdf#page=3

¹⁰ TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC · 23 April 2026 ^[A]
pr.tsmc.com/english/news/3302

SoIC bonding also brings optics into the package. TSMC's COUPE uses SoIC to join a silicon photonics chip, which sends data as light, to its electrical control chip ¹⁹. TSMC said in April 2026 that COUPE on substrate would begin production in 2026 ¹⁰. It also said that putting COUPE inside the package gives twice the power efficiency of a pluggable version on the circuit board ¹⁰.

Two ways off the silicon interposer

Panel-level packaging replaces the round wafer with a rectangular panel, which wastes far less area. See Test and assembly. JEDEC, the semiconductor standards body, published a standard called SPHBM4 on 13 July 2026. It puts HBM4 memory on a base chip carrying 512 data signals instead of 2,048, each running four times as fast to keep the same bandwidth ¹⁵. With fewer signals, the connections can be spaced widely enough to mount the stack on a standard resin substrate instead of the silicon interposer ¹⁵.

¹⁹ TSMC 2025 Annual Report, chapter 5. TSMC · 16 April 2026 · p. 3 [\[A\]](https://investor.tsmc.com/static/annualReports/2025/english/pdf/2025_tsmc_ar_e_ch5.pdf#page=3)
investor.tsmc.com/static/annualReports/2025/english/pdf/2025_tsmc_ar_e_ch5.pdf#page=3

¹⁰ TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC · 23 April 2026 [\[A\]](https://pr.tsmc.com/english/news/3302)
pr.tsmc.com/english/news/3302

¹⁵ New JEDEC® SPHBM4 Standard Enables HBM4-Class Bandwidth on Organic Substrates. JEDEC Solid State Technology Association · 13 July 2026 [\[A\]](https://www.jedec.org/news/pressreleases/new-jedec%C2%AE-sphbm4-standard-enables-hbm4-class-bandwidth-organic-substrates)
www.jedec.org/news/pressreleases/new-jedec%C2%AE-sphbm4-standard-enables-hbm4-class-bandwidth-organic-substrates

Capacity

TSMC does not publish its CoWoS capacity ³. Industry estimates from SemiWiki and TrendForce, compiled by Epoch AI, put it at about 65,000 to 75,000 wafers a month at the end of 2025, up from 35,000 to 40,000 a year earlier ³.

At its 2024 symposium TSMC said CoWoS capacity would grow at a 60 percent compound annual rate over the next few years ²⁴. But when asked about that rate on the July 2024 earnings call, TSMC's chief executive, C.C. Wei, did not repeat it ²⁴. He said he could not yet balance supply and demand ²⁴. He also said TSMC was

³ Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip production in 2025. Epoch AI · 12 March 2026

epoch.ai/data-insights/ai-chip-supply-chain-constraints

²⁴ Q2 2024 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv

StreetEvents (transcript of a TSMC earnings call), via TSMC · 18 July 2024 · p. 6 [A](#)

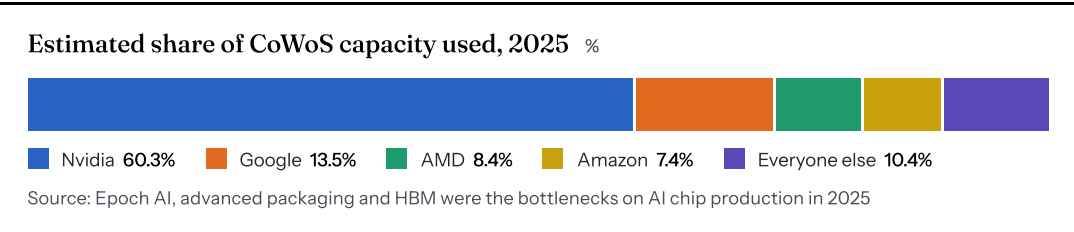
[investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2024-](https://investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2024-08/5122725a56670882d777a8e8bfe0ed247cc55330/TSMC%202Q24%20Transcript.pdf#page=6)

[08/5122725a56670882d777a8e8bfe0ed247cc55330/TSMC%202Q24%20Transcript.pdf#page=6](https://investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2024-08/5122725a56670882d777a8e8bfe0ed247cc55330/TSMC%202Q24%20Transcript.pdf#page=6)

more than doubling CoWoS capacity in 2024 and would more than double it again in 2025 ²⁴.

In October 2025 Wei would say only that TSMC was working to increase capacity in 2026 and would probably give the real number in 2026 ²⁵. He said front-end capacity (making the chips) and back-end capacity (packaging them) were both, in his words, very tight ²⁵.

Epoch AI compared each chip designer's use of components with world supply ³. It puts Nvidia at 60.3 percent of all CoWoS capacity in 2025, with a 90 percent confidence interval of 56.5 to 64.3 ³. Google took 13.5 percent, AMD 8.4 and Amazon 7.4 ³. Together those four used around 90 percent of global CoWoS capacity and HBM supply, with HBM measured by value, but only 12 percent of advanced logic die production ³.



In March 2026 the research firm SemiAnalysis judged that front-end capacity had become the dominant bottleneck and that CoWoS constraints were easing ⁹. It said TSMC was planning CoWoS capacity around how many wafers N3, its 3 nm

24 Q2 2024 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 18 July 2024 · p. 6 [\[A\]](https://investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2024-08/5122725a56670882d777a8e8bfe0ed247cc55330/TSMC%202Q24%20Transcript.pdf#page=6)

25 Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 October 2025 · p. 7 [\[A\]](https://investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2025-10/6860312f04fd291d0f26b46c1234f84e6332717e/TSMC%203Q25%20Transcript.pdf#page=7)

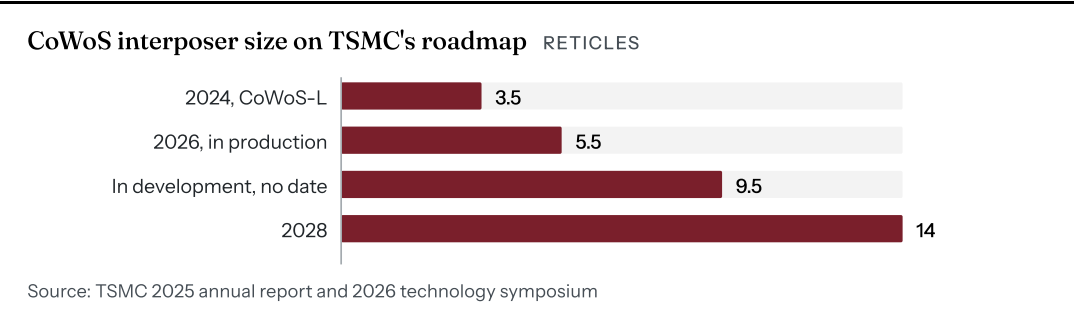
3 Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip production in 2025. Epoch AI · 12 March 2026 [\[A\]](https://epoch.ai/data-insights/ai-chip-supply-chain-constraints)

9 The Great AI Silicon Shortage. SemiAnalysis · 12 March 2026 [\[B\]](https://newsletter.semianalysis.com/p/the-great-ai-silicon-shortage)

process, could produce, because added packaging capacity is of no use without front-end wafers to fill it ⁹. It also noted that CoWoS packaging can be, and has been, outsourced to assembly firms such as ASE and Amkor ⁹.

TSMC gave a different account four months later. On the July 2026 earnings call, Wei said TSMC's packaging capacity was so tight that it limited customers' growth ¹. Asked about Intel's EMIB-T, he said he welcomed the extra flexibility and hoped it would take some of the load off TSMC ¹. Later in the call he said back-end capacity was still in shortage ²⁶.

Who makes it



Three kinds of firm package chips. TSMC, which makes chips for others, and Intel, which makes its own, do it in their own back-end fabs. Outsourced assembly and test firms do the rest. Intel opened Fab 9 in Rio Rancho, New Mexico, in January 2024 to make its Foveros 3D packages in volume ⁴. It called the plant the only US factory producing the most advanced packaging at scale ⁴.

⁹ The Great AI Silicon Shortage. SemiAnalysis · 12 March 2026 [B](https://newsletter.semianalysis.com/p/the-great-ai-silicon-shortage)

¹ Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. LSEG StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 July 2026 · p. 10 [A](https://investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897aa044415e21d93486cc4/TSMC%202Q26%20Transcript.pdf#page=10)

²⁶ Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. LSEG StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 July 2026 · p. 17 [A](https://investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897aa044415e21d93486cc4/TSMC%202Q26%20Transcript.pdf#page=17)

⁴ Intel Opens Fab 9 in New Mexico. Intel · 24 January 2024 [A](https://www.intel.com/content/www/us/en/newsroom/news/intel-opens-fab-9-new-mexico.html)

ASE Technology Holding, the leading provider of assembly and test services, had revenue of NT\$645.4 billion in 2025, about 40 percent of it from electronics manufacturing services ⁵. Its assembly, test and materials business brought in NT\$389.2 billion, up from NT\$325.9 billion in 2024 ⁵. Amkor, the largest US-headquartered assembly and test firm, had net sales of \$6.71 billion in 2025 ⁶.

The packaging tools are a narrower chokepoint than the assembly firms.

- **Thermocompression bonding.** Pressing dies together under heat and force. ASMPT's advanced packaging revenue reached \$532.1 million in 2025, with thermocompression bonder revenue up about 146 percent ⁸. ASMPT targets 35 to 40 percent of a market it puts at \$1.6 billion in 2028 ⁸.
- **Hybrid bonding.** Copper pads and the insulator around them bond directly, with no solder. Applied Materials co-developed its Kinex hybrid bonding system with Besi, which Applied calls the industry leader in hybrid bonding ²⁷.
- **Grinding and dicing.** Disco held 87 percent of the \$1.9 billion world market for dicing tools in 2025, by CSET's count from TechInsights data ²⁸. The category covers the grinders that thin wafers and the saws that cut them into chips ²⁸. See Test and assembly.

TSMC's Arizona commitment reached \$265 billion in July 2026 and covers two advanced packaging plants alongside 10 fabs ²⁹. Amkor started building a \$7 billion campus in Peoria in October 2025 and expects production from early 2028 ¹³. The Commerce Department awarded Amkor up to \$407 million in CHIPS Act funding for the site in December 2024 ³⁰. In October 2025 Wei said a large outsourced packaging partner, already breaking ground in Arizona, was on an earlier schedule than TSMC's own two packaging fabs there ³¹.

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6 AMKOR TECHNOLOGY, INC., Form 8-K current report for the period ended 2026-02-09 (8-K). U.S. Securities and Exchange Commission (filing by AMKOR TECHNOLOGY, INC.) · 9 February 2026 [A](https://www.sec.gov/Archives/edgar/data/1047127/000104712726000007/amkr123125erex-991.htm) www.sec.gov/Archives/edgar/data/1047127/000104712726000007/amkr123125erex-991.htm

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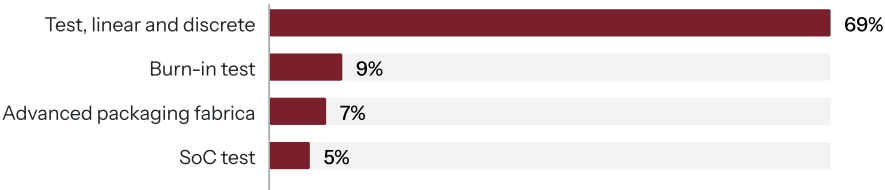
13 Amkor Technology Breaks Ground on New Semiconductor Advanced Packaging and Test Campus in Arizona; Expands Investment to \$7 Billion. Amkor Technology · 6 October 2025 [A](https://ir.amkor.com/news-releases/news-release-details/amkor-technology-breaks-ground-new-semiconductor-advanced) ir.amkor.com/news-releases/news-release-details/amkor-technology-breaks-ground-new-semiconductor-advanced

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The chokepoint

China-based suppliers' share of selected tool segments, 2024 %



Source: CSET, Inside Beijing's Chipmaking Offensive

Four of the top ten outsourced assembly and test firms by 2024 revenue are headquartered in China, by a TrendForce ranking that CSET cites ¹². JCET, a leading Chinese assembly and test firm, had record revenue of RMB 38.87 billion in 2025, up 8.1 percent ⁷. JCET says its XDFOI platform has entered high-volume manufacturing with redistribution-layer interposer, silicon interposer and silicon bridge options ³².

Between 2019 and 2024, Chinese firms gained 5 percentage points of share in test tools and 4 points in fabrication tools built for advanced packaging, by CSET's analysis of TechInsights data ¹². But they lost share in bonding and other conventional assembly and packaging tools, the category where CSET counts hybrid and thermocompression bonders ¹². Within the advanced packaging fabrication tools, Chinese firms gained 10 points in etch and clean tools and 3 points in deposition tools ¹². They lost 2 points each in lithography and polishing (CMP) tools ¹². In 2024 Chinese firms had 7 percent of the market for advanced packaging fabrication tools ¹². In 2025 they had 5.3 percent of the \$6.2 billion world market for these tools, against 65.8 percent for US firms and 15.3 percent for Japanese firms, by CSET's analysis of TechInsights data ¹¹.

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11 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 20 October 2026 [A](https://chipexplorer.eto.tech/?parentNode=N69&selectedNode=N109)
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TSMC said in April 2026 that it was producing CoWoS at 5.5 times the size of a reticle field and planning larger versions ¹⁰. Each generation on TSMC's roadmap needs a larger interposer.

- **2028.** A 14-reticle interposer, about the area of a compact disc, carrying about ten large compute dies and 20 HBM stacks ¹⁰.
- **2029.** More than 14 reticles, plus a 40-reticle System-on-Wafer ¹⁰.

FOUR THINGS TO REMEMBER

- Many leading accelerators, Nvidia's Blackwell among them, need more logic than one chip can hold, so packaging joins several chips and their memory.
- Nvidia, Google, AMD and Amazon all rely on TSMC, in Taiwan, to package their accelerators.
- Packaging was one of the main limits on AI chip output in 2025. In July 2026 TSMC said its packaging capacity was still so tight that it limited customers' growth.
- No US site yet packages Nvidia-class accelerators with HBM on CoWoS, though Intel makes its own Foveros 3D packages in volume in New Mexico.

Made by **Yashvardhan Sharma** with Claude. Corrections and questions: contact@chipsupplychain.org.

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A company filings, governments, standards bodies, universities and research institutions; **B** SemiAnalysis, Reuters, the Financial Times and Nikkei Asia.

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¹⁰ TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC · 23 April 2026 **A**
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▼ Details

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