

Chapter 1: Chip Design, EDA and IP

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CHAPTER

01

STAGE 1 OF 15

Chip Design, EDA and IP

Synopsys, Cadence and Siemens EDA sell the software used to design every leading-edge AI accelerator. In 2025 they took over 85 percent of an \$18 billion market, licensed blocks included.

IN PLAIN TERMS

Chip design turns an idea for a new chip into a complete blueprint. A chip holds billions of transistors, tiny electrical switches. The blueprint fixes where each one sits and how it is wired to the others. The chip runs on a clock, and a signal has to cross those wires within one tick, less than a billionth of a second. Software from three companies, Synopsys, Cadence and Siemens, lays out the blueprint, checks it and signs it off. A foundry, a factory that makes chips for other companies, accepts only designs that have passed that software's checks. The foundry prints each layer of the design onto silicon through a stencil called a mask. Changing the blueprint once the masks are made takes new masks and a few months ⁸.

⁸ The Dark Side Of The Semiconductor Design Renaissance – Fixed Costs Soaring Due To Photomask Sets, Verification, and Validation. SemiAnalysis · 24 July 2022 [B](https://newsletter.semianalysis.com/p/the-dark-side-of-the-semiconductor) newsletter.semianalysis.com/p/the-dark-side-of-the-semiconductor

IN SHORT

The US government required a license to sell design software to anyone in China from late May to 2 July 2025 ⁷. Since October 2022 a narrower requirement has covered software specially made for chips with gate-all-around transistors, a transistor design the rule calls key to processes at 3 nm and below ²³.

As of 2025, the think tank CSIS found Chinese design tools still far from replacing the full range of advanced capabilities US firms offer, especially for 5 nm and 3 nm chip design ⁶. But Chinese design-software companies were winning share at older manufacturing processes, the research firm SemiAnalysis reported ².

⁷ CADENCE DESIGN SYSTEMS INC, Form 8-K current report for the period ended 2025-07-02 (8-K). U.S. Securities and Exchange Commission (filing by CADENCE DESIGN SYSTEMS INC) · 3 July 2025 ^[A] www.sec.gov/Archives/edgar/data/813672/000081367225000093/cdns-20250702.htm

²³ Implementation of Certain 2021 Wassenaar Arrangement Decisions on Four Section 1758 Technologies. Federal Register (Commerce Department; Industry and Security Bureau) · 15 August 2022 ^[A] www.federalregister.gov/documents/2022/08/15/2022-17125/implementation-of-certain-2021-wassenaar-arrangement-decisions-on-four-section-1758-technologies

⁶ The Double-Edged Sword of Semiconductor Export Controls: Electronic Design Automation. Center for Strategic and International Studies · 6 October 2025 · p. 33 ^[A] csis-website-prod.s3.amazonaws.com/s3fs-public/2025-10/251006_Reinsch_Semiconductor_Export_O.pdf#page=33

² EDA Market Primer. SemiAnalysis · 21 May 2026 ^[B] newsletter.semianalysis.com/p/eda-market-primer

CHOKEPOINT CARD		EXTREME CONCENTRATION	HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY		PRICE OR MARKET SIZE
Extreme	Hard		\$18B
	Only three complete sets of chip design software exist ¹ . A fourth would have to be written from nothing and approved by a foundry ² .		world market for design software, simulation software and licensed circuit blocks in 2025 ² , SemiAnalysis put a single respin at leading-edge nodes at \$50-100M in May 2026 ²
WHO LEADS	US Synopsys 90%+ of the timing-signoff market at advanced nodes as of 2026² US Cadence 55-60% of the hardware emulator market at advanced nodes as of 2026² US Siemens EDA 85%+ of physical verification, the final layout check, at advanced nodes as of 2026² GB Arm About 50% of processor compute at the top cloud firms as of May 2026³ US Broadcom \$16.7B of AI semiconductor revenue in the third quarter of fiscal 2026, custom accelerators and networking combined⁴		
WHERE IT IS MADE	US United States Synopsys, Cadence, Broadcom, Marvell and Nvidia GB United Kingdom Arm processor and interconnect designs licensed from Cambridge, and since 2026 its own server chip TW Taiwan Alchip, Global Unichip and MediaTek: design services that carry a chip to the factory IL Israel Annapurna Labs, the AWS design house behind Trainium and Graviton IN India Nearly 20% of the world's chip design engineers, on the Indian government's count		
WHY SUBSTITUTION IS SLOW	Changing one tool, such as the synthesis tool, means re-running the later steps of the design ² . The foundry that makes the chip also specifies which signoff tools its customers must use ² .		

WHERE CHINA STANDS	WHERE THE US STANDS
China designs its own AI accelerators, but Huawei's most powerful chip in 2026, the Ascend 950, delivers about half the computing performance of Nvidia's H100 from 2022, on Epoch AI's estimate ⁵ . CSIS found that as of 2025 Chinese design tools were still far from replacing the full range of advanced capabilities US firms offer, especially for 5 nm and 3 nm chips ⁶ .	Synopsys and Cadence, the two largest design-software vendors by 2025 revenue, are American ² .

1 The Double-Edged Sword of Semiconductor Export Controls: Electronic Design Automation. Center for Strategic and International Studies · 6 October 2025 [\[A\]](#) [csis-website-prod.s3.amazonaws.com/s3fs-public/2025-10/251006_Reinsch_Semiconductor_Export_Q.pdf#page=13](#)

2 EDA Market Primer. SemiAnalysis · 21 May 2026 [\[B\]](#) [newsletter.semianalysis.com/p/eda-market-primer](#)

3 Arm delivers record-breaking quarter and full-year results. Arm · 6 May 2026 [\[A\]](#) [newsroom.arm.com/news/arm-q4-fye26-results](#)

Design is the only stage of the supply chain that happens entirely in software, and the US government has already restricted it by letter. In late May 2025 the government required a license to sell chip design software to anyone in China ⁷. Cadence cut off its Chinese customers until the government lifted the requirement on 2 July ⁷.

How it works

Design runs in five stages, all in software, and each stage's output is the next one's input.

- **Architecture.** Engineers fix the shape of the chip: the width of the block that multiplies numbers, the amount of fast on-chip memory beside it and the number of high-bandwidth memory stacks along the chip's edges. The output is a plan.
- **RTL.** Engineers write the plan as register-transfer-level code, RTL, in the hardware language SystemVerilog. A register is a small store on the chip that holds one number. On each tick of the chip's clock, every register takes its next value at the same moment. The code says what every register holds on every tick. The output is a text description of the whole chip.
- **Verification.** A large team checks that the code does what the plan says. They run it in simulation and prove parts of it correct with mathematics. They also load it into emulators, cabinets of reprogrammable chips that behave like the design, so the chip's own software can boot before any silicon exists.
- **Physical design.** Software swaps each piece of the code for a logic cell, a small ready-made circuit the foundry has already proved it can make. It then places the cells on the chip, wires them together and proves that every signal arrives in time.
- **Tape-out.** Engineers hand the finished layout to the foundry, a step called tape-out. Software then turns the layout into pattern files for the mask shop, in steps that run after tape-out ⁹. First it pre-distorts each shape so that the shape prints

⁴ Broadcom Inc., Form 8-K current report for the period ended 2026-09-02 (8-K). U.S. Securities and Exchange Commission (filing by Broadcom Inc.) · 2 September 2026 [\[A\]](https://www.sec.gov/Archives/edgar/data/0001730168/000173016826000076/avgo-08022026x8kxex99.htm) www.sec.gov/Archives/edgar/data/0001730168/000173016826000076/avgo-08022026x8kxex99.htm

² EDA Market Primer. SemiAnalysis · 21 May 2026 [\[B\]](https://newsletter.semianalysis.com/p/eda-market-primer) newsletter.semianalysis.com/p/eda-market-primer

⁵ Will Huawei catch up to Nvidia by 2030? Epoch AI · 24 September 2026 [\[A\]](https://epoch.ai/publications/huaweis-roadmap-to-2031) epoch.ai/publications/huaweis-roadmap-to-2031

⁶ The Double-Edged Sword of Semiconductor Export Controls: Electronic Design Automation. Center for Strategic and International Studies · 6 October 2025 · p. 33 [\[A\]](https://csis-website-prod.s3.amazonaws.com/s3fs-public/2025-10/251006_Reinsch_Semiconductor_Export_O.pdf#page=33) csis-website-prod.s3.amazonaws.com/s3fs-public/2025-10/251006_Reinsch_Semiconductor_Export_O.pdf#page=33

⁷ CADENCE DESIGN SYSTEMS INC, Form 8-K current report for the period ended 2025-07-02 (8-K). U.S. Securities and Exchange Commission (filing by CADENCE DESIGN SYSTEMS INC) · 3 July 2025 [\[A\]](https://www.sec.gov/Archives/edgar/data/813672/000081367225000093/cdns-20250702.htm) www.sec.gov/Archives/edgar/data/813672/000081367225000093/cdns-20250702.htm

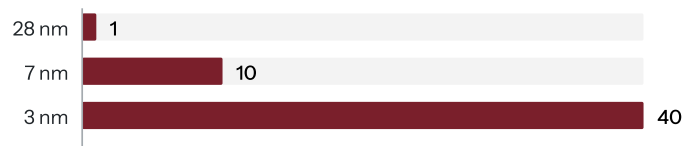
⁹ Unlocking post-tapeout flow scalability and performance with cloud computing. Siemens Digital Industries Software · 8 January 2025 [\[A\]](https://blogs.sw.siemens.com/calibre/2025/01/08/unlocking-post-tapeout-flow-scalability-and-performance-with-cloud-computing/) blogs.sw.siemens.com/calibre/2025/01/08/unlocking-post-tapeout-flow-scalability-and-performance-with-cloud-computing/

as drawn, a step called optical proximity correction. Then it cuts the layout into the files a mask writer reads, a step called mask data preparation.

All that checking exists because each revision after tape-out, called a respin, needs at least some new masks ⁸. In 2022 SemiAnalysis put a full mask set at more than \$1 million at 28 nm and more than \$10 million at 7 nm ⁸. The nanometer labels name process generations, called nodes, each finer than the last, and no longer measure anything. That year SemiAnalysis also expected 3 nm sets to push into the \$40 million range ⁸. Its May 2026 primer still puts a leading-edge mask set at \$40 million, and a single leading-edge respin at \$50 million to \$100 million ².

The same 2022 SemiAnalysis article reported that startups had taken chips on TSMC 7 nm, then a leading-edge process, from design to tape-out for \$50 million to \$75 million, everything included ⁸.

What one photomask set costs, by node, 2022 (\$M). The 28 nm and 7 nm figures are minimums \$M



Source: SemiAnalysis, The Dark Side of the Semiconductor Design Renaissance, July 2022. The 3 nm figure was a 2022 forecast. SemiAnalysis's May 2026 EDA Market Primer puts a leading-edge mask set at \$40M

Variants and trade-offs

Merchant GPU versus custom ASIC

Nvidia designs its Blackwell GPU once and sells it to everyone, so the buyer gets mature software and a resale market. A custom accelerator, an ASIC, is built for one company's own workload. It handles a narrower range of tasks and is tuned to that workload. Ironwood, the seventh-generation tensor processing unit (TPU) Google announced in April 2025, carries 192 GB of memory per chip, six times its predecessor's, and delivers twice the performance per watt ¹⁰. In April 2026 Google announced its eighth generation as two chips, the TPU 8t for training and the TPU 8i for inference, with up to twice Ironwood's performance per watt ¹¹.

⁸ The Dark Side Of The Semiconductor Design Renaissance – Fixed Costs Soaring Due To Photomask Sets, Verification, and Validation. SemiAnalysis · 24 July 2022 [\[B\]](https://newsletter.semianalysis.com/p/the-dark-side-of-the-semiconductor) newsletter.semianalysis.com/p/the-dark-side-of-the-semiconductor

² EDA Market Primer. SemiAnalysis · 21 May 2026 [\[B\]](https://newsletter.semianalysis.com/p/eda-market-primer) newsletter.semianalysis.com/p/eda-market-primer

¹⁰ Ironwood: The first Google TPU for the age of inference. Google · 9 April 2025 [\[A\]](https://blog.google/innovation-and-ai/infrastructure-and-cloud/google-cloud/ironwood-tpu-age-of-inference/) blog.google/innovation-and-ai/infrastructure-and-cloud/google-cloud/ironwood-tpu-age-of-inference/

¹¹ Our eighth generation TPUs: two chips for the agentic era. Google · 22 April 2026 [\[A\]](https://blog.google/innovation-and-ai/infrastructure-and-cloud/google-cloud/eighth-generation-tpu-agentic-era/) blog.google/innovation-and-ai/infrastructure-and-cloud/google-cloud/eighth-generation-tpu-agentic-era/

The EDA flow

Chip design software is known as electronic design automation, or EDA. Three complete EDA flows exist, each a set of tools that covers every step from code to signoff ¹. SemiAnalysis wrote in May 2026 that no startup can replicate one by writing it from scratch ². Changing the synthesis tool, which swaps the code for logic cells, means re-running the steps that follow: placing and wiring the cells, signoff and physical verification ². Foundries also specify which signoff tools their customers must use for tape-out ².

For chips at advanced nodes, 7 nm and below, one vendor holds most of the market inside some steps of the flow. Synopsys alone has more than 90 percent of the market for static timing analysis, the check that every signal arrives in time at the chip's rated speed ². In May 2026 SemiAnalysis put Siemens EDA's Calibre at more than 85 percent of physical verification, the final layout check ². It put Cadence's Palladium at 55 to 60 percent of hardware emulation ².

Each leading vendor's share of its own design-software segment at advanced nodes, 7 nm and below. Lower end of each reported range %



Source: SemiAnalysis, EDA Market Primer, May 2026, table of tool-level shares at advanced nodes

Buy the IP or build it

Design houses license ready-made circuit blocks, known as intellectual property or IP, including the processor cores, the interface controllers and the blocks that drive high-bandwidth memory. Arm licenses processor designs. In fiscal 2026 it reported \$4.92 billion of revenue, \$2.61 billion of it royalties ³. It said it held about 50 percent of processor compute at the top cloud firms ³.

In 2026 Arm also launched the Arm AGI CPU, its first production silicon product ³. By May 2026, servers built on it could be ordered from ASRock, Lenovo, Quanta and Supermicro ³.

1 The Double-Edged Sword of Semiconductor Export Controls: Electronic Design Automation. Center for Strategic and International Studies · 6 October 2025 · p. 13 [\[A\]](#) csis-website-prod.s3.amazonaws.com/s3fs-public/2025-10/251006_Reinsch_Semiconductor_Export_Q.pdf#page=13

2 EDA Market Primer. SemiAnalysis · 21 May 2026 [\[B\]](#) newsletter.semianalysis.com/p/eda-market-primer

3 Arm delivers record-breaking quarter and full-year results. Arm · 6 May 2026 [\[A\]](#) newsroom.arm.com/news/arm-q4-fye26-results

The memory interface is hard to design, because its signals have to stay on time across thousands of microscopic solder bumps into a stacked memory die.

RISC-V is an open instruction set, the basic list of commands a processor understands, and it needs no license. Small RISC-V processors handle control tasks on the chip, and Nvidia uses them in every GPU ¹².

Chipselets

The reticle limit caps the size of a single die, one piece of silicon ¹³. That limit is the largest area a scanner, the machine that prints the chip's pattern, can expose in one shot. Many large accelerators are built from chiplets, several smaller dies wired together, and UCIe is an open industry standard for the links between them inside a package ¹⁴. Version 3.0 of UCIe adds faster data rates, 48 and 64 gigatransfers per second ¹⁴. In a December 2024 presentation, Broadcom said its 3.5D XDSiP platform packs more than 6,000 mm² of silicon and 12 high-bandwidth memory stacks into one package ¹³.

Who makes it

Design software, simulation software and licensed blocks made up an \$18 billion market in 2025, on SemiAnalysis's count ². Synopsys, Cadence and Siemens EDA took more than 85 percent of it, counting Ansys as part of Synopsys ². No other vendor had more than 5 percent of any core category ². Siemens EDA is a US-based subsidiary of the German firm Siemens ¹⁵.

Synopsys is the largest. Its own results put revenue at \$7.054 billion for the fiscal year to 31 October 2025, with Ansys, bought that July, contributing \$756.6 million ¹⁶. Cadence, whose year ends in December, took \$5.297 billion in calendar 2025 ¹⁷.

The two fiscal years do not line up, so any total for this market depends on which twelve months are counted. It also depends on how much of Ansys it includes, because Ansys sells to other industries too. SemiAnalysis counts Synopsys at \$8 billion for calendar 2025 with Ansys included ². On the same count Cadence is second, at \$5.30 billion, and Siemens EDA third, at an estimated \$2.2 billion to \$2.5 billion ². It puts 31 percent of Ansys's business in semiconductors and high technology, 22 percent in aerospace and 18 percent in automotive ².

¹² Behind The Scenes of SHD Group's 2026 RISC-V Market Forecast. RISC-V International · 19 June 2026 [\[A\]](https://riscv.org/blog/shd-forecast-2026/) riscv.org/blog/shd-forecast-2026/

¹³ 3.5D XDSiP Platform Technology. Broadcom · 4 December 2024 [\[A\]](https://docs.broadcom.com/doc/3-5d-xdsip-platform-technology) docs.broadcom.com/doc/3-5d-xdsip-platform-technology

¹⁴ UCIe specifications. UCIe Consortium · Accessed 9 September 2026 [\[A\]](https://www.uciexpress.org/specifications) www.uciexpress.org/specifications

² EDA Market Primer. SemiAnalysis · 21 May 2026 [\[B\]](https://newsletter.semianalysis.com/p/eda-market-primer) newsletter.semianalysis.com/p/eda-market-primer

¹⁵ The Double-Edged Sword of Semiconductor Export Controls: Electronic Design Automation. Center for Strategic and International Studies · 6 October 2025 · p. 7 [\[A\]](https://csis-website-prod.s3.amazonaws.com/s3fs-public/2025-10/251006_Reinsch_Semiconductor_Export_O.pdf#page=7) csis-website-prod.s3.amazonaws.com/s3fs-public/2025-10/251006_Reinsch_Semiconductor_Export_O.pdf#page=7

¹⁶ SYNOPSYS INC, Form 8-K current report for the period ended 2025-12-10 (8-K). U.S. Securities and Exchange Commission (filing by SYNOPSYS INC) · 10 December 2025 [\[A\]](https://www.sec.gov/Archives/edgar/data/883241/000119312525314200/d29055dex991.htm) www.sec.gov/Archives/edgar/data/883241/000119312525314200/d29055dex991.htm

¹⁷ CADENCE DESIGN SYSTEMS INC, Form 8-K current report for the period ended 2026-02-17 (8-K). U.S. Securities and Exchange Commission (filing by CADENCE DESIGN SYSTEMS INC) · 17 February 2026 [\[A\]](https://www.sec.gov/Archives/edgar/data/813672/000081367226000013/cdns02172026ex9901.htm) www.sec.gov/Archives/edgar/data/813672/000081367226000013/cdns02172026ex9901.htm

Share of revenue from design software, simulation software and licensed blocks, 2025. Synopsys includes part of Ansys's revenue %



Source: SemiAnalysis, EDA Market Primer, May 2026, table of calendar 2025 vendor shares

Some chip firms also build custom accelerators to a customer's design and sell the finished chips. Broadcom booked \$16.7 billion of AI semiconductor revenue in the third quarter of fiscal 2026, up 221 percent year over year ⁴. That figure covers both its custom AI accelerators and its AI networking chips ⁴.

In October 2025 OpenAI and Broadcom said they would deploy 10 gigawatts of OpenAI-designed accelerators ¹⁸. Broadcom would turn the design into silicon and supply the Ethernet networking around it ¹⁸. In April 2026 Broadcom and Meta extended their partnership to multiple gigawatts of MTIA, Meta's custom chip, including what they called the industry's first 2 nm AI accelerator ¹⁹.

Marvell, another US firm, also builds custom AI chips to each customer's specifications ²⁰. Below Broadcom and Marvell are the Taiwanese design-service houses. They carry a customer's circuit list all the way to a finished mask set on TSMC's newest nodes. One of them, Alchip, reported \$992 million of revenue in 2025 ²¹.

Chip design engineers are spread across more countries than these firms are. India alone has nearly 20 percent of the world's chip design engineers, the Indian

⁴ Broadcom Inc., Form 8-K current report for the period ended 2026-09-02 (8-K). U.S. Securities and Exchange Commission (filing by Broadcom Inc.) · 2 September 2026 [\[A\]](https://www.sec.gov/Archives/edgar/data/0001730168/000173016826000076/avgo-08022026x8kxex99.htm) www.sec.gov/Archives/edgar/data/0001730168/000173016826000076/avgo-08022026x8kxex99.htm

¹⁸ OpenAI and Broadcom announce strategic collaboration to deploy 10 gigawatts of OpenAI-designed AI accelerators. Broadcom · 13 October 2025 [\[A\]](https://investors.broadcom.com/news-releases/news-release-details/openai-and-broadcom-announce-strategic-collaboration-deploy-10) investors.broadcom.com/news-releases/news-release-details/openai-and-broadcom-announce-strategic-collaboration-deploy-10

¹⁹ Broadcom Announces Extended Partnership with Meta to Deploy Technology to Support Multi-Gigawatts of Meta's Custom Silicon, MTIA. Broadcom · 14 April 2026 [\[A\]](https://investors.broadcom.com/news-releases/news-release-details/broadcom-announces-extended-partnership-meta-deploy-technology) investors.broadcom.com/news-releases/news-release-details/broadcom-announces-extended-partnership-meta-deploy-technology

²⁰ Marvell Technology, Inc., Form 10-K annual report for the period ended 2026-01-31 (10-K). U.S. Securities and Exchange Commission (filing by Marvell Technology, Inc.) · 11 March 2026 [\[A\]](https://www.sec.gov/Archives/edgar/data/1835632/000183563226000011/mrvl-20260131.htm) www.sec.gov/Archives/edgar/data/1835632/000183563226000011/mrvl-20260131.htm

²¹ Alchip Technologies, financials page. Alchip Technologies · Accessed 9 September 2026 [\[A\]](https://www.alchip.com/en/Investors/financials/) www.alchip.com/en/Investors/financials/

government said in July 2025 ²².

The chokepoint

Before the 2025 letters, a narrower control already applied. Since 14 October 2022, design software specially made for chips with gate-all-around transistors has needed a US export license for national-security reasons ²³. The rule calls that transistor design key to processes at 3 nm and below ²³. That license requirement covers exports to China ²⁴. The control carried out a December 2021 decision of the Wassenaar Arrangement, a group of countries that coordinate export controls ²³.

In late May 2025 the US Bureau of Industry and Security, the agency that issues export licenses, told the design-software vendors that sales to China now needed a license ⁷. Cadence got its letter on 23 May ⁷. The letter required a license to export design software and technology classified 3D991 and 3E991 to any party in China, or to a Chinese military end user anywhere ⁷. Synopsys got its letter on 29 May and a second letter lifting the requirement on 2 July ²⁵.

Unlike the 2022 control, the 2025 requirement came from the United States alone and took effect immediately. Synopsys's China revenue fell from 16 percent of its total in fiscal 2024 to 12 percent in fiscal 2025 ². SemiAnalysis links the decline to tighter export restrictions and to local design-software companies winning share at mature nodes ². SemiAnalysis also quoted Synopsys's management saying that

22 India's Semiconductor Vision Gathers Momentum with 3nm Chip Design and Large-Scale Talent Development Initiatives. Press Information Bureau, Government of India · 25 July 2025 ^[A] www.pib.gov.in/PressReleasePage.aspx?PRID=2148393

23 Implementation of Certain 2021 Wassenaar Arrangement Decisions on Four Section 1758 Technologies. Federal Register (Commerce Department; Industry and Security Bureau) · 15 August 2022 ^[A] www.federalregister.gov/documents/2022/08/15/2022-17125/implementation-of-certain-2021-wassenaar-arrangement-decisions-on-four-section-1758-technologies

24 Supplement No. 1 to Part 738, Title 15 -- Commerce Country Chart. Electronic Code of Federal Regulations · 30 September 2025 ^[A] www.ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-738/appendix-Supplement%20No.%201%20to%20Part%20738

7 CADENCE DESIGN SYSTEMS INC, Form 8-K current report for the period ended 2025-07-02 (8-K). U.S. Securities and Exchange Commission (filing by CADENCE DESIGN SYSTEMS INC) · 3 July 2025 ^[A] www.sec.gov/Archives/edgar/data/813672/000081367225000093/cdns-20250702.htm

25 SYNOPSYS INC, Form 8-K current report for the period ended 2025-07-02 (8-K). U.S. Securities and Exchange Commission (filing by SYNOPSYS INC) · 3 July 2025 ^[A] www.sec.gov/Archives/edgar/data/883241/000119312525155294/d80081d8k.htm

2 EDA Market Primer. SemiAnalysis · 21 May 2026 ^[B] newsletter.semianalysis.com/p/eda-market-primer

companies Synopsys cannot sell to look for alternatives, typically local design-software and licensed-block companies ².

In October 2025 CSIS found that only a few companies, Cadence, Synopsys and Siemens, make design software that supports the entire chip design flow of more than 40 steps ¹. In a January 2021 report built on 2019 market data, CSET at Georgetown University found that one Chinese firm, Empyrean, could reportedly run a complete design flow only for certain analog and mixed-signal chips ²⁶. Mixed-signal chips combine analog and digital circuits. For all other chips, Chinese designers then relied on US tools ²⁶. The report found that other Chinese tools covered only narrow parts of the design flow or supplemented US tools, and largely did not support processes at 14 nm and below ²⁶.

In its 2025 annual report, filed in April 2026, Empyrean says it now has complete design flows for analog, memory, radio-frequency and flat-panel display circuits ²⁷. It says its digital tools cover 80 percent of the main tools for digital design ²⁸. The same report lists foundry certifications for its circuit simulator at 8, 5 and 4 nm and for its physical verification tool, the final layout check, at 28 nm ²⁹. But CSIS found that as of 2025 Chinese design tools were still far from replacing the full range of advanced capabilities US firms offer, especially for 5 nm and 3 nm chip design ⁶.

China can design accelerators, but it cannot finish one at the leading edge without foreign tools, or build what it designs without foreign equipment. SMIC, China's leading foundry, makes chips for Huawei ⁵. In June 2024 CSET found that SMIC's limited 7 nm capacity forced Huawei to choose between making its most advanced phone chips and its AI chips ³⁰.

On Epoch AI's estimates, Huawei's flagship chip for 2026, the Ascend 950, delivers about half the computing performance of Nvidia's H100, which began shipping in 2022 ⁵. Epoch puts Nvidia's B300 at 6.75 times the 950's theoretical peak performance ⁵. Epoch's median estimate is that Huawei will make about 1.5

2 EDA Market Primer. SemiAnalysis · 21 May 2026 [B] newsletter.semianalysis.com/p/eda-market-primer

1 The Double-Edged Sword of Semiconductor Export Controls: Electronic Design Automation. Center for Strategic and International Studies · 6 October 2025 · p. 13 [A] csis-website-prod.s3.amazonaws.com/s3fs-public/2025-10/251006_Reinsch_Semiconductor_Export_O.pdf#page=13

26 The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology (CSET) · 21 January 2021 · p. 50 [A] cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf#page=50

27 北京华大九天科技股份有限公司2025年年度报告全文. CNINFO · 27 April 2026 · p. 18 [A] static.cninfo.com.cn/finalpage/2026-04-28/1225217315.PDF#page=18

28 北京华大九天科技股份有限公司2025年年度报告全文. CNINFO · 27 April 2026 · p. 14 [A] static.cninfo.com.cn/finalpage/2026-04-28/1225217315.PDF#page=14

29 北京华大九天科技股份有限公司2025年年度报告全文. CNINFO · 27 April 2026 · p. 15 [A] static.cninfo.com.cn/finalpage/2026-04-28/1225217315.PDF#page=15

6 The Double-Edged Sword of Semiconductor Export Controls: Electronic Design Automation. Center for Strategic and International Studies · 6 October 2025 · p. 33 [A] csis-website-prod.s3.amazonaws.com/s3fs-public/2025-10/251006_Reinsch_Semiconductor_Export_O.pdf#page=33

5 Will Huawei catch up to Nvidia by 2030?. Epoch AI · 24 September 2026 [A] epoch.ai/publications/huaweis-roadmap-to-2031

30 Pushing the Limits: Huawei's AI Chip Tests U.S. Export Controls. Center for Security and Emerging Technology (CSET) · 17 June 2024 [A] cset.georgetown.edu/publication/pushing-the-limits-huaweis-ai-chip-tests-u-s-export-controls/

million Ascend chips in 2026, against 5.9 million for Nvidia ⁵. On those estimates, Huawei's 2026 output would carry less than 4 percent of the computing power Nvidia ships that year ⁵.

Epoch puts Huawei's chips three to four years behind Nvidia's until at least 2030, for three reasons ⁵. SMIC cannot pack transistors as densely as TSMC, which makes Nvidia's. Chinese memory makers are only starting to produce high-bandwidth memory. And Huawei's software for programming its chips is far less mature than Nvidia's ⁵.

FIVE THINGS TO REMEMBER

- Chip design turns an idea into a blueprint, and a factory builds only designs checked in approved software.
- Synopsys, Cadence and Siemens EDA sell the software used to design every leading-edge AI chip.
- To compete with them, a new vendor would have to write a complete set of tools and win a foundry's approval.
- China designs its own AI chips, but in October 2025 CSIS found its design software still far from replacing US tools, especially for 5 nm and 3 nm chips.
- Huawei's best AI chip trails Nvidia's by three to four years, on Epoch AI's estimate.

Made by **Yashvardhan Sharma** with Claude. Corrections and questions: contact@chipsupplychain.org.

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A company filings, governments, standards bodies, universities and research institutions; **B** SemiAnalysis, Reuters, the Financial Times and Nikkei Asia.

HOW TO CITE THIS CHAPTER

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⁵ Will Huawei catch up to Nvidia by 2030?. Epoch AI · 24 September 2026 **A** epoch.ai/publications/huaweis-roadmap-to-2031

▼ Details

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