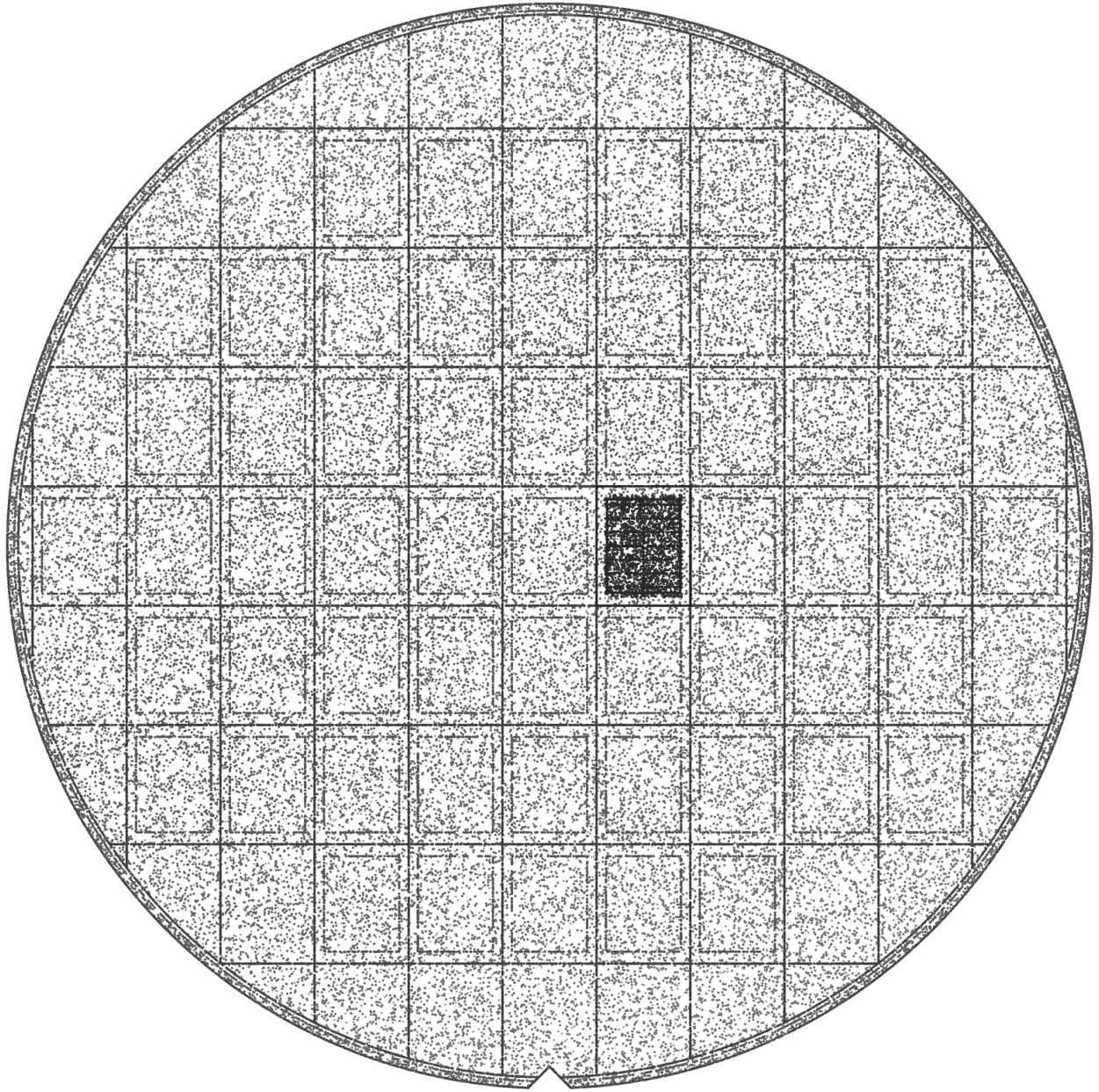




 Chip Supply Chain

How AI chips are made

Every stage of the supply chain, and who controls it.

Yashvardhan Sharma

Edition of 29 October 2026 · chipsupplychain.org

Supply Chain

This edition covers each of the fourteen stages of making an AI chip in detail, one chapter per stage, in the order a chip is made, from design software to the data center. Two more chapters at the end look across all the stages, at what a chip costs and who controls the chain. Each chapter ends with questions to answer from memory. Online, every chapter also has a 3D model, and most have an animation.

Contents

The fourteen stages of the chain

■ Extreme □ High

01	■	Chip Design, EDA and IP	3
02	□	Silicon and Wafers	14
03	□	Chemicals, Gases and Photoresist	25
04	■	Lithography	37
05	■	Photomasks and Pellicles	51
06	□	Deposition and Etch	61
07	□	Metrology and Inspection	74
08	■	Foundries and Fabs	85
09	■	Memory and HBM	101
10	■	Advanced Packaging	111
11	■	Substrates and PCBs	122
12	□	Test and Assembly	133
13	□	Systems and Networking	143
14	□	Data Centers and Power	154

Across the chain

These two chapters are not stages. They look across all fourteen, at what a chip costs and at the contest over who controls each stage.

15		The Economics of AI Chips	165
16		Who Controls the Chain	174



01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Chip Design, EDA and IP

Synopsys, Cadence and Siemens EDA make the software used to design every advanced chip. In 2025 they took over 85 percent of its \$18 billion market, licensed blocks included.

Specimen 01 · Chip Design, EDA and IP

A GPU die based on Nvidia's published H100 block diagram. It is drawn at the size of one full reticle field, 26 by 33 mm, the largest area a scanner can print in one shot. H100 is a single die. The drawing adds a copper strip on one short edge to stand for the die-to-die link that two-die designs such as Blackwell carry.

In plain terms

Chip design turns an idea for a new chip into a complete blueprint. A chip holds billions of transistors, tiny electrical switches. The blueprint fixes where each one sits and how it is wired to the others. The chip runs on a clock, and a signal has to cross those wires within one tick, less than a billionth of a second. Software from three companies, Synopsys, Cadence and Siemens, lays out the blueprint, checks it and signs it off. A foundry, a factory that makes chips for other companies, accepts only designs that have passed that software's checks. The foundry prints each layer of the design onto silicon through a stencil called a mask. Changing the blueprint once the masks are made takes new masks and a few months¹.

In short

At advanced nodes, 7 nm and below, Synopsys alone has more than 90 percent of the market for static timing analysis, the check that every signal arrives in time². SemiAnalysis wrote in May 2026 that no startup can replicate a complete design flow by writing it from scratch².

Since October 2022 a US license has been needed to export design software specially made for chips with gate-all-around transistors, a transistor design the rule calls key to processes at 3 nm and below³. As of 2025, the think tank CSIS found Chinese design tools still far from replacing the full range of advanced capabilities US firms offer, especially for 5 nm and 3 nm chip design⁴. But Chinese design-software companies were winning share

¹ The Dark Side Of The Semiconductor Design Renaissance – Fixed Costs Soaring Due... SemiAnalysis, 24 July 2022. newsletter.semianalysis.com

² EDA Market Primer. SemiAnalysis, 21 May 2026. newsletter.semianalysis.com

³ Implementation of Certain 2021 Wassenaar Arrangement Decisions on Four Section... Federal Register, 15 August 2022. [federalregister.gov](https://www.federalregister.gov)

⁴ The Double-Edged Sword of Semiconductor Export Controls: Electronic Design... Center for Strategic and International Studies, 6 October 2025, p. 33. csis-website-prod.s3.amazonaws.com

at older manufacturing processes, the research firm SemiAnalysis reported².

Design is the only stage of the supply chain that happens entirely in software. The US government has restricted it with letters to the companies that sell that software. In late May 2025 the government required a license to sell chip design software to anyone in China⁵. Cadence cut off its Chinese customers until the government lifted the requirement on 2 July⁵.

Chokepoint card		Chip Design, EDA and IP
Concentration	Substitutability	Price or market size
<div><div><div></div><div></div><div></div></div><div>Extreme</div></div> <p>Three or fewer firms could supply this stage today, or one firm holds more than half of it.</p>	<div>Hard</div> <p>Only three complete sets of chip design software exist⁶. A fourth would have to be written from nothing and approved by a foundry².</p>	<div>\$18 billion</div> <p>world market for design software, simulation software and licensed circuit blocks in 2025². SemiAnalysis put a single respin, a design revision that needs some new masks, at leading-edge nodes at \$50 million to \$100 million in May 2026²</p>
Who leads	US Synopsys	Over 90 percent of the timing-signoff market at advanced nodes as of 2026 ²
	US Cadence	55 to 60 percent of the hardware emulator market at advanced nodes as of 2026 ²
	US Siemens EDA	Over 85 percent of physical verification, the final layout check, at advanced nodes as of 2026 ²
	GB Arm	About 50 percent of processor compute at the top cloud firms as of May 2026 ⁷
	US Broadcom	\$16.7 billion of AI semiconductor revenue in the third quarter of fiscal 2026, custom accelerators and networking combined ⁸
Where it is made	US United States	Synopsys, Cadence, Broadcom, Marvell and Nvidia
	GB United Kingdom	Arm processor and interconnect designs licensed from Cambridge, and since 2026 its own server chip
	TW Taiwan	Alchip, Global Unichip and MediaTek: design services that carry a chip to the factory
	IL Israel	Annapurna Labs, the AWS design house behind Trainium and Graviton
	IN India	Nearly 20 percent of the world's chip design engineers, on the Indian government's count
Why substitution is slow	Changing one tool, such as the synthesis tool that turns a design's code into logic cells, means re-running the later steps of the design ² . The foundry that makes the chip also specifies which signoff tools its customers must use ² .	

2 EDA Market Primer. SemiAnalysis, 21 May 2026. newsletter@semianalysis.com

5 Cadence Design Systems, current report on Form 8-K dated 2 July 2025. U.S. Securities and Exchange Commission, 3 July 2025. [sec.gov](https://www.sec.gov)

6 The Double-Edged Sword of Semiconductor Export Controls: Electronic Design... Center for Strategic and International Studies, 6 October 2025, p. 13. [csis-website-prod.s3.amazonaws.com](https://www.csis-website-prod.s3.amazonaws.com)

7 Arm delivers record-breaking quarter and full-year results. Arm, 6 May 2026. newsroom.arm.com

8 Broadcom, current report on Form 8-K dated 2 September 2026. U.S. Securities and Exchange Commission, 2 September 2026. [sec.gov](https://www.sec.gov)

Where China stands

China designs its own AI accelerators, but Huawei's most powerful chip in 2026, the Ascend 950, delivers about half the computing performance of Nvidia's H100 from 2022, on Epoch AI's estimate⁹. CSIS found that as of 2025 Chinese design tools were still far from replacing the full range of advanced capabilities US firms offer, especially for 5 nm and 3 nm chips⁴.

Where the US stands

Synopsys and Cadence, the two largest design-software vendors by 2025 revenue, are American².

01

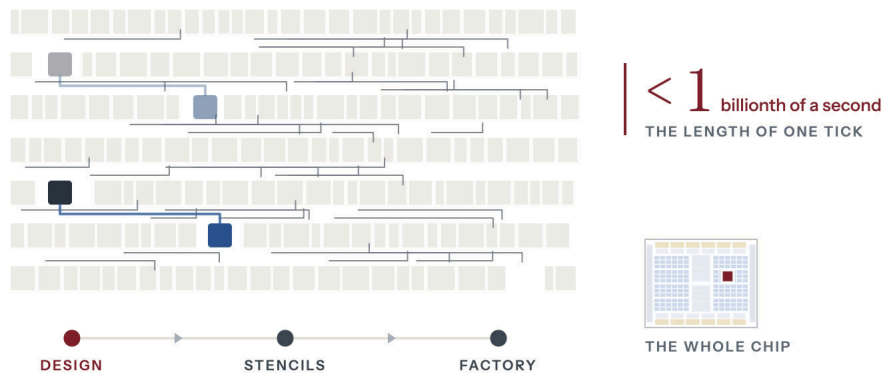
How a chip is designed

Figure 01.1 · Explainer, 23 seconds

How a chip is designed

Checked before anything is made

Only then is it printed onto silicon



1. **A blueprint.** Making a chip starts with design, which turns an idea into a complete blueprint. The blueprint fixes where each of the chip's billions of switches sits and how each one is wired to the others.
2. **One tick.** The chip works in ticks, each less than a billionth of a second. On every tick a signal leaves a register, a small store that holds one number, and it has to cross its wire to the next register before the next tick.
3. **Too far.** If the next register sits far away, the wire is long. The signal is still on its way when the next tick comes, so it arrives too late.
4. **Placed closer.** Design software from three companies, Synopsys, Cadence and Siemens, places the parts and wires them together. Here it moves the register closer, and the signal arrives in time.
5. **Checked.** The software checks that every signal arrives in time and that every shape can be printed, and a chip factory accepts only designs that pass the printing checks. The factory then prints the blueprint onto silicon through stencils, and changing it after that costs new stencils and a few months.

Note: Simplified. Not to scale. The floorplan follows a GPU die. One tick, less than a billionth of a second, is slowed to about two seconds.

² EDA Market Primer. SemiAnalysis, 21 May 2026. newsletter.semianalysis.com

⁴ The Double-Edged Sword of Semiconductor Export Controls: Electronic Design... Center for Strategic and International Studies, 6 October 2025, p. 33. csis-website-prod.s3.amazonaws.com

⁹ Will Huawei catch up to Nvidia by 2030? Epoch AI, 24 September 2026. epoch.ai

Design runs in five stages, all in software, and each stage's output is the next one's input.

- **Architecture.** Engineers fix the shape of the chip: the width of the block that multiplies numbers, the amount of fast on-chip memory beside it and the number of high-bandwidth memory stacks along the chip's edges. The output is a plan.
- **RTL.** Engineers write the plan as register-transfer-level code, RTL, in the hardware language SystemVerilog. A register is a small store on the chip that holds one number. On each tick of the chip's clock, every register takes its next value at the same moment. The code says what every register holds on every tick. The output is a text description of the whole chip.
- **Verification.** A large team checks that the code does what the plan says. They run it in simulation and prove parts of it correct with mathematics. They also load it into emulators, large machines full of reprogrammable chips that behave like the design, so the chip's own software can boot before any silicon exists.
- **Physical design.** Software swaps each piece of the code for a logic cell, a small ready-made circuit the foundry has already proved it can make. It then places the cells on the chip, wires them together and proves that every signal arrives in time.
- **Tape-out.** Engineers hand the finished layout to the foundry, a step called tape-out. After tape-out, software turns the layout into pattern files for the mask shop¹⁰. First it pre-distorts each shape so that the shape prints as drawn, a step called optical proximity correction. Then it cuts the layout into the files a mask writer reads, a step called mask data preparation.

All that checking exists because each revision after tape-out, called a respin, needs at least some new masks¹. In 2022 SemiAnalysis put a full mask set at more than \$1 million at 28 nm and more than \$10 million at 7 nm¹. The nanometer labels name process generations, called nodes, each finer than the last, and no longer measure anything. In 2022 SemiAnalysis also expected 3 nm sets to push into the \$40 million range¹. Its May 2026 primer still puts a leading-edge mask set at \$40 million, and a single leading-edge respin at \$50 million to \$100 million².

The same 2022 SemiAnalysis article reported that startups had taken chips on TSMC 7 nm, then a leading-edge process, from design to tape-out for \$50 million to \$75 million, everything included¹.

¹ The Dark Side Of The Semiconductor Design Renaissance – Fixed Costs Soaring Due... SemiAnalysis, 24 July 2022. newsletter.semianalysis.com

² EDA Market Primer. SemiAnalysis, 21 May 2026. newsletter.semianalysis.com

¹⁰ Unlocking post-tapeout flow scalability and performance with cloud computing. Siemens Digital Industries Software, 8 January 2025. blogs.sw.siemens.com

Figure 01.2

In 2022 SemiAnalysis forecast a 3 nm mask set at \$40 million

What one photomask set costs, by node, 2022. The 28 nm and 7 nm figures are minimums, and 3 nm was a forecast



Source: SemiAnalysis, The Dark Side of the Semiconductor Design Renaissance, July 2022. SemiAnalysis's May 2026 EDA Market Primer puts a leading-edge mask set at \$40 million [1]

02

GPUs, custom chips and chiplets

Merchant GPU versus custom ASIC

Nvidia designs its Blackwell GPU once and sells it to everyone, so the buyer gets mature software and a resale market. A custom accelerator, an ASIC, is built for one company's own workload. It handles a narrower range of tasks and is tuned to that workload. Google's tensor processing units (TPUs) are custom accelerators of this kind¹¹. Ironwood, the seventh generation, which Google announced in April 2025, carries 192 GB of memory per chip, six times its predecessor's, and delivers twice the performance per watt¹¹. In April 2026 Google announced its eighth generation as two chips, the TPU 8t for training and the TPU 8i for inference, with up to twice Ironwood's performance per watt¹².

The EDA flow

Chip design software is known as electronic design automation, or EDA. Three complete EDA flows exist, each a set of tools that covers every step from code to signoff⁶. SemiAnalysis wrote in May 2026 that no startup can replicate one by writing it from scratch². Changing the synthesis tool, which swaps the code for logic cells, means re-running the steps that follow: placing and wiring the cells, signoff and physical verification². Foundries also specify which signoff tools their customers must use for tape-out².

For chips at advanced nodes, 7 nm and below, one vendor holds most of the market inside some steps of the flow. Synopsys alone has more than 90 percent of the market for static timing analysis, the check that every signal arrives in time at the chip's rated speed². In May 2026 SemiAnalysis put Siemens EDA's Calibre at more than 85 percent of physical verification, the final layout check². It put Cadence's Palladium at 55 to 60 percent of hardware emulation².

1 The Dark Side Of The Semiconductor Design Renaissance – Fixed Costs Soaring Due... SemiAnalysis, 24 July 2022. newsletter.semianalysis.com

2 EDA Market Primer. SemiAnalysis, 21 May 2026. newsletter.semianalysis.com

6 The Double-Edged Sword of Semiconductor Export Controls: Electronic Design... Center for Strategic and International Studies, 6 October 2025, p. 13. csis-website-prod.s3.amazonaws.com

11 Ironwood: The first Google TPU for the age of inference. Google, 9 April 2025. blog.google

12 Our eighth generation TPUs: two chips for the agentic era. Google, 22 April 2026. blog.google

Figure 01.3

In 2026 each segment's leading tool held at least 55 percent

Share held by the leading vendor in each of four design-software segments at advanced nodes, 7 nm and below. Lower end of each reported range



Source: SemiAnalysis, EDA Market Primer, May 2026, table of tool-level shares at advanced nodes [2]

Buy the IP or build it

Design houses license ready-made circuit blocks, known as intellectual property or IP, including the processor cores, the interface controllers and the blocks that drive high-bandwidth memory. The block that drives high-bandwidth memory is hard to design, because its signals have to arrive in time across microscopic solder bumps into a stacked memory die.

Arm licenses processor designs. In fiscal 2026 it reported \$4.92 billion of revenue, \$2.61 billion of it royalties⁷. It said Arm-based designs held about 50 percent of the computing power of central processors (CPUs) at the top cloud firms⁷.

In 2026 Arm also launched the Arm AGI CPU, the first finished chip that Arm sells⁷. By May 2026, servers built on it could be ordered from ASRock, Lenovo, Quanta and Supermicro⁷.

RISC-V is an open instruction set, the basic list of commands a processor understands, and it needs no license. Small RISC-V processors handle control tasks on the chip, and Nvidia uses them in every GPU¹³.

Chiplets

The reticle limit caps the size of a single die, one piece of silicon¹⁴. That limit is the largest area a scanner, the machine that prints the chip's pattern, can expose in one shot. Many large accelerators are built from chiplets, several smaller dies wired together inside one package¹⁵. UCIE is an open industry standard for the links between them¹⁵. Version 3.0 of UCIE adds two faster data rates, 48 and 64 billion transfers per second, written GT/s for gigatransfers per second¹⁵. In a December 2024 presentation, Broadcom described its 3.5D XDSiP platform, which stacks dies face to face and sets the stacks side by side on an interposer¹⁴. It said the platform packs more than 6,000 mm² of silicon and 12 high-bandwidth memory stacks into one package¹⁴.

² EDA Market Primer. SemiAnalysis, 21 May 2026. newsletter.semianalysis.com

⁷ Arm delivers record-breaking quarter and full-year results. Arm, 6 May 2026. newsroom.arm.com

¹³ Behind The Scenes of SHD Group's 2026 RISC-V Market Forecast. RISC-V International, 19 June 2026. riscv.org

¹⁴ 3.5D XDSiP Platform Technology. Broadcom, 4 December 2024. docs.broadcom.com

¹⁵ UCIE specifications. UCIE Consortium, accessed 9 September 2026. uciexpress.org

03

Who makes the design software and custom chips

Design software, simulation software and licensed blocks made up an \$18 billion market in 2025, on SemiAnalysis's count². Synopsys, Cadence and Siemens EDA took more than 85 percent of it, counting Ansys as part of Synopsys². No other vendor had more than 5 percent of any of the main categories of design software². Siemens EDA is a US-based subsidiary of the German firm Siemens¹⁶.

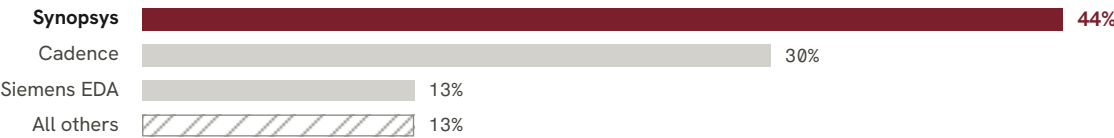
Synopsys is the largest. Its own results put revenue at \$7.054 billion for the fiscal year to 31 October 2025, with Ansys, bought that July, contributing \$756.6 million¹⁷. Cadence, whose year ends in December, took \$5.297 billion in calendar 2025¹⁸.

The two fiscal years do not line up, so any total for this market depends on which twelve months are counted. It also depends on how much of Ansys the total includes, because Ansys sells to other industries too. SemiAnalysis puts 31 percent of Ansys's business in semiconductors and high technology, 22 percent in aerospace and 18 percent in automotive². It counts Synopsys at \$8 billion for calendar 2025 with Ansys included². On the same count Cadence is second, at \$5.30 billion, and Siemens EDA third, at an estimated \$2.2 billion to \$2.5 billion².

Figure 01.4

Synopsys took 44 percent of the 2025 market, Cadence 30 percent

Share of revenue from design software, simulation software and licensed blocks, 2025. Synopsys includes part of Ansys's revenue



Source: SemiAnalysis, EDA Market Primer, May 2026, table of calendar 2025 vendor shares [2]

Chip firms such as Broadcom build custom accelerators to a customer's design and sell the finished chips. Broadcom booked \$16.7 billion of AI semiconductor revenue in the third quarter of fiscal 2026, up 221 percent year over year⁸. That figure covers both its custom AI accelerators and its AI networking chips⁸.

Broadcom's custom-chip customers include OpenAI and Meta. In October 2025 OpenAI and Broadcom said they would deploy OpenAI-designed accelerators drawing 10 gigawatts of power¹⁹. Broadcom would turn the design into silicon and supply the Ethernet networking around it¹⁹. In April 2026 Broadcom and Meta extended their

2 EDA Market Primer. SemiAnalysis, 21 May 2026. newsletter.semianalysis.com

8 Broadcom, current report on Form 8-K dated 2 September 2026. U.S. Securities and Exchange Commission, 2 September 2026. sec.gov

16 The Double-Edged Sword of Semiconductor Export Controls: Electronic Design... Center for Strategic and International Studies, 6 October 2025, p. 7. csis-website-prod.s3.amazonaws.com

17 Synopsys, current report on Form 8-K dated 10 December 2025. U.S. Securities and Exchange Commission, 10 December 2025. sec.gov

18 Cadence Design Systems, current report on Form 8-K dated 17 February 2026. U.S. Securities and Exchange Commission, 17 February 2026. sec.gov

19 OpenAI and Broadcom announce strategic collaboration to deploy 10 gigawatts of... Broadcom, 13 October 2025. investors.broadcom.com

partnership to multiple gigawatts of MTIA, Meta's custom chip, including what they called the industry's first 2 nm AI accelerator²⁰.

Marvell, another US firm, also builds custom AI chips to each customer's specifications²¹. Taiwanese design-service houses carry a customer's circuit list, the logic cells and the wires between them, all the way to a finished mask set on TSMC's newest nodes. One of them, Alchip, reported \$992 million of revenue in 2025²².

India has nearly 20 percent of the world's chip design engineers, the Indian government said in July 2025²³.

04

Design software export controls and China's own tools

In October 2025 CSIS found that only three companies, Cadence, Synopsys and Siemens, make design software that supports the entire chip design flow of more than 40 steps⁶. In late May 2025 the US Bureau of Industry and Security, the agency that issues export licenses, told the design-software vendors that sales to China now needed a license⁵. Synopsys got its letter on 29 May and a second letter lifting the requirement on 2 July²⁴. CSIS found that as of 2025 Chinese design tools were still far from replacing the full range of advanced capabilities US firms offer, especially for 5 nm and 3 nm chip design⁴.

Before the 2025 letters, a narrower control already applied. Since 14 October 2022, design software specially made for chips with gate-all-around transistors has needed a US export license for national-security reasons³. The rule calls that transistor design key to processes at 3 nm and below³. That license requirement covers exports to China²⁵. The control carried out a December 2021 decision of the Wassenaar Arrangement, a group of countries that coordinate export controls³.

Cadence got its letter on 23 May⁵. The letter required a license to export design software and technology classified 3D991 and 3E991 to any party in China, or to a Chinese military end user anywhere⁵. Unlike the 2022 control, the 2025 requirement came from the United States alone and took effect immediately.

Synopsys's China revenue fell from 16 percent of its total in fiscal 2024 to 12 percent in fiscal 2025². SemiAnalysis links the decline to tighter export restrictions and to local design-software companies winning share at mature nodes². SemiAnalysis also quoted

2 EDA Market Primer. SemiAnalysis, 21 May 2026. newsletter.semianalysis.com

3 Implementation of Certain 2021 Wassenaar Arrangement Decisions on Four Section... Federal Register, 15 August 2022. [federalregister.gov](https://www.federalregister.gov)

4 The Double-Edged Sword of Semiconductor Export Controls: Electronic Design... Center for Strategic and International Studies, 6 October 2025, p. 33. [csis-website-prod.s3.amazonaws.com](https://www.csis-website-prod.s3.amazonaws.com)

5 Cadence Design Systems, current report on Form 8-K dated 2 July 2025. U.S. Securities and Exchange Commission, 3 July 2025. sec.gov

6 The Double-Edged Sword of Semiconductor Export Controls: Electronic Design... Center for Strategic and International Studies, 6 October 2025, p. 13. [csis-website-prod.s3.amazonaws.com](https://www.csis-website-prod.s3.amazonaws.com)

20 Broadcom Announces Extended Partnership with Meta to Deploy Technology to... Broadcom, 14 April 2026. investors.broadcom.com

21 Marvell Technology, annual report on Form 10-K for the fiscal year ended 31... U.S. Securities and Exchange Commission, 11 March 2026. sec.gov

22 Alchip Technologies, financials page. Alchip Technologies, accessed 9 September 2026. alchip.com

23 India's Semiconductor Vision Gathers Momentum with 3nm Chip Design and... Press Information Bureau, Government of India, 25 July 2025. pib.gov.in

24 Synopsys, current report on Form 8-K dated 2 July 2025. U.S. Securities and Exchange Commission, 3 July 2025. sec.gov

25 Supplement No. 1 to Part 738, Title 15 -- Commerce Country Chart. Electronic Code of Federal Regulations, 30 September 2025. ecfr.gov

Synopsys's management saying that when Synopsys cannot sell to a company, that company looks for alternatives, typically local design-software and licensed-block companies².

In a January 2021 report built on 2019 market data, the Center for Security and Emerging Technology (CSET) at Georgetown University found that one Chinese firm, Empyrean, could reportedly run a complete design flow only for some analog and mixed-signal chips²⁶. Mixed-signal chips combine analog and digital circuits. For all other chips, Chinese designers then relied on US tools²⁶. The report found that other Chinese tools covered only narrow parts of the design flow or supplemented US tools, and largely did not support processes at 14 nm and below²⁶.

Empyrean says it has covered more of the design flow since then. Its 2025 annual report, filed in April 2026, says it now has complete design flows for analog, memory, radio-frequency and flat-panel display circuits²⁷. It says it offers 80 percent of the main tools used in digital design²⁸. The same report lists foundry certifications for its circuit simulator at 8, 5 and 4 nm and for its physical verification tool, the final layout check, at 28 nm²⁹.

China can design accelerators, but it cannot finish one at the leading edge without foreign tools, or build what it designs without foreign equipment. SMIC, China's leading foundry, makes chips for Huawei⁹. In June 2024 CSET found that SMIC's limited 7 nm capacity forced Huawei to choose between making its most advanced phone chips and its AI chips³⁰.

Epoch AI estimates that Huawei trails Nvidia both in what each chip can do and in how many chips it makes⁹. On Epoch's estimates, Huawei's flagship chip for 2026, the Ascend 950, delivers about half the computing performance of Nvidia's H100, which began shipping in 2022⁹. Epoch puts Nvidia's B300 at 6.75 times the 950's theoretical peak performance⁹. Epoch's median estimate is that Huawei will make about 1.5 million Ascend chips in 2026, against 5.9 million for Nvidia⁹. On those estimates, Huawei's 2026 output would carry less than 4 percent of the computing power Nvidia ships that year⁹.

Epoch puts Huawei's chips three to four years behind Nvidia's until at least 2030, for three reasons⁹. SMIC cannot pack transistors as densely as TSMC, which makes Nvidia's. Chinese memory makers are only starting to produce high-bandwidth memory. And Huawei's software for programming its chips is far less mature than Nvidia's⁹.

Four questions to answer from memory

1. What does chip design produce? see How it works
2. Who makes the software used to design chips? see How it works

² EDA Market Primer. SemiAnalysis, 21 May 2026. newsletter.semianalysis.com

⁹ Will Huawei catch up to Nvidia by 2030? Epoch AI, 24 September 2026. epoch.ai

²⁶ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 50. cset.georgetown.edu

²⁷ 北京华大九天科技股份有限公司2025年年度报告全文. CNINFO, 27 April 2026, p. 18. static.cninfo.com.cn

²⁸ 北京华大九天科技股份有限公司2025年年度报告全文. CNINFO, 27 April 2026, p. 14. static.cninfo.com.cn

²⁹ 北京华大九天科技股份有限公司2025年年度报告全文. CNINFO, 27 April 2026, p. 15. static.cninfo.com.cn

³⁰ Pushing the Limits: Huawei's AI Chip Tests U.S. Export Controls. Center for Security and Emerging Technology, 17 June 2024. cset.georgetown.edu

3. Why is that software so hard to replace? see The EDA flow
4. How do export controls reach chip design? see The chokepoint

Five things to remember

- Chip design turns an idea into a blueprint, and a factory builds only designs checked in approved software.
 - Synopsys, Cadence and Siemens EDA sell the software used to design every leading-edge AI chip.
 - To compete with them, a new vendor would have to write a complete set of tools and win a foundry's approval.
 - China designs its own AI chips, but in October 2025 CSIS found its design software still far from replacing US tools, especially for 5 nm and 3 nm chips.
 - Huawei's best AI chip trails Nvidia's by three to four years, on Epoch AI's estimate.
-

Sources (30)

1. B The Dark Side Of The Semiconductor Design Renaissance – Fixed Costs Soaring Due To Photomask Sets, Verification, and Validation. SemiAnalysis · 24 July 2022
newsletter.semianalysis.com/p/the-dark-side-of-the-semiconductor
2. B EDA Market Primer. SemiAnalysis · 21 May 2026
newsletter.semianalysis.com/p/eda-market-primer
3. A Implementation of Certain 2021 Wassenaar Arrangement Decisions on Four Section 1758 Technologies. Federal Register (Commerce Department; Industry and Security Bureau) · 15 August 2022
www.federalregister.gov/documents/2022/08/15/2022-17125/implementation-of-certain-2021-wassenaar-arrangement-decisions-on-four-section-1758-technologies
4. A The Double-Edged Sword of Semiconductor Export Controls: Electronic Design Automation. Center for Strategic and International Studies · 6 October 2025 · p. 33
csis-website-prod.s3.amazonaws.com/s3fs-public/2025-10/251006_Reinsch_Semiconductor_Export_0.pdf#page=33
5. A Cadence Design Systems, current report on Form 8-K dated 2 July 2025. U.S. Securities and Exchange Commission (filing by Cadence Design Systems) · 3 July 2025
www.sec.gov/Archives/edgar/data/813672/000081367225000093/cdns-20250702.htm
6. A The Double-Edged Sword of Semiconductor Export Controls: Electronic Design Automation. Center for Strategic and International Studies · 6 October 2025 · p. 13
csis-website-prod.s3.amazonaws.com/s3fs-public/2025-10/251006_Reinsch_Semiconductor_Export_0.pdf#page=13
7. A Arm delivers record-breaking quarter and full-year results. Arm · 6 May 2026
newsroom.arm.com/news/arm-q4-fye26-results
8. A Broadcom, current report on Form 8-K dated 2 September 2026. U.S. Securities and Exchange Commission (filing by Broadcom) · 2 September 2026
www.sec.gov/Archives/edgar/data/0001730168/000173016826000076/avgo-08022026x8kxex99.htm
9. A Will Huawei catch up to Nvidia by 2030? Epoch AI · 24 September 2026
epoch.ai/publications/huaweis-roadmap-to-2031
10. A Unlocking post-tapeout flow scalability and performance with cloud computing. Siemens Digital Industries Software · 8 January 2025
blogs.sw.siemens.com/calibre/2025/01/08/unlocking-post-tapeout-flow-scalability-and-performance-with-cloud-computing/
11. A Ironwood: The first Google TPU for the age of inference. Google · 9 April 2025
blog.google/innovation-and-ai/infrastructure-and-cloud/google-cloud/ironwood-tpu-age-of-inference/
12. A Our eighth generation TPUs: two chips for the agentic era. Google · 22 April 2026
blog.google/innovation-and-ai/infrastructure-and-cloud/google-cloud/eighth-generation-tpu-agentic-era/
13. A Behind The Scenes of SHD Group's 2026 RISC-V Market Forecast. RISC-V International · 19 June 2026
riscv.org/blog/shd-forecast-2026/
14. A 3.5D XDSiP Platform Technology. Broadcom · 4 December 2024
docs.broadcom.com/doc/3-5d-xdsip-platform-technology
15. A UCle specifications. UCle Consortium · Accessed 9 September 2026
www.uciexpress.org/specifications
16. A The Double-Edged Sword of Semiconductor Export Controls: Electronic Design Automation. Center for Strategic and International Studies · 6 October 2025 · p. 7
csis-website-prod.s3.amazonaws.com/s3fs-public/2025-10/251006_Reinsch_Semiconductor_Export_0.pdf#page=7
17. A Synopsys, current report on Form 8-K dated 10 December 2025. U.S. Securities and Exchange Commission (filing by Synopsys) · 10 December 2025
www.sec.gov/Archives/edgar/data/883241/000119312525314200/d29055dex991.htm

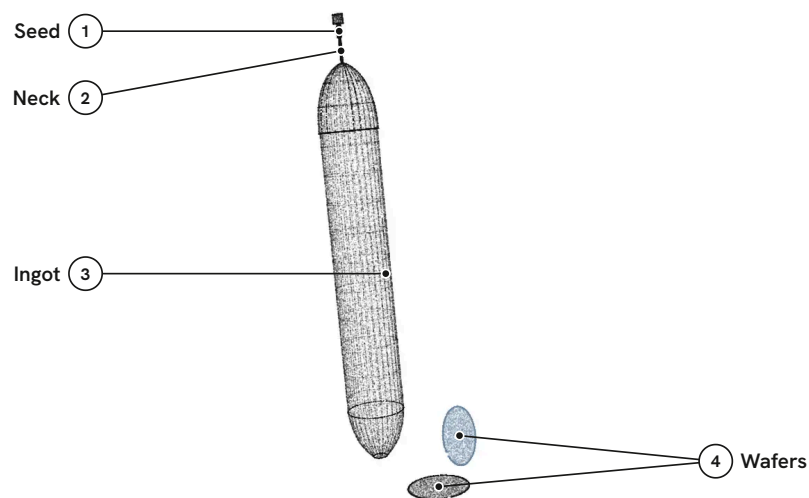
18. A **Cadence Design Systems, current report on Form 8-K dated 17 February 2026.** U.S. Securities and Exchange Commission (filing by Cadence Design Systems) · 17 February 2026
www.sec.gov/Archives/edgar/data/813672/000081367226000013/cdns02172026ex9901.htm
19. A **OpenAI and Broadcom announce strategic collaboration to deploy 10 gigawatts of OpenAI-designed AI accelerators.** Broadcom · 13 October 2025
investors.broadcom.com/news-releases/news-release-details/openai-and-broadcom-announce-strategic-collaboration-deploy-10
20. A **Broadcom Announces Extended Partnership with Meta to Deploy Technology to Support Multi-Gigawatts of Meta's Custom Silicon, MTIA.** Broadcom · 14 April 2026
investors.broadcom.com/news-releases/news-release-details/broadcom-announces-extended-partnership-meta-deploy-technology
21. A **Marvell Technology, annual report on Form 10-K for the fiscal year ended 31 January 2026.** U.S. Securities and Exchange Commission (filing by Marvell Technology) · 11 March 2026
www.sec.gov/Archives/edgar/data/1835632/000183563226000011/mrvl-20260131.htm
22. A **Alchip Technologies, financials page.** Alchip Technologies · Accessed 9 September 2026
www.alchip.com/en/Investors/financials/
23. A **India's Semiconductor Vision Gathers Momentum with 3nm Chip Design and Large-Scale Talent Development Initiatives.** Press Information Bureau, Government of India · 25 July 2025
www.pib.gov.in/PressReleasePage.aspx?PRID=2148393
24. A **Synopsys, current report on Form 8-K dated 2 July 2025.** U.S. Securities and Exchange Commission (filing by Synopsys) · 3 July 2025
www.sec.gov/Archives/edgar/data/883241/000119312525155294/d80081d8k.htm
25. A **Supplement No. 1 to Part 738, Title 15 -- Commerce Country Chart.** Electronic Code of Federal Regulations · 30 September 2025
www.ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-738/appendix-Supplement%20No.%201%20to%20Part%20738
26. A **The Semiconductor Supply Chain - Issue Brief.** Center for Security and Emerging Technology (CSET) · 21 January 2021 · p. 50
cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf#page=50
27. A **北京华大九天科技股份有限公司2025年年度报告全文.** CNINFO · 27 April 2026 · p. 18
static.cninfo.com.cn/finalpage/2026-04-28/1225217315.PDF#page=18
28. A **北京华大九天科技股份有限公司2025年年度报告全文.** CNINFO · 27 April 2026 · p. 14
static.cninfo.com.cn/finalpage/2026-04-28/1225217315.PDF#page=14
29. A **北京华大九天科技股份有限公司2025年年度报告全文.** CNINFO · 27 April 2026 · p. 15
static.cninfo.com.cn/finalpage/2026-04-28/1225217315.PDF#page=15
30. A **Pushing the Limits: Huawei's AI Chip Tests U.S. Export Controls.** Center for Security and Emerging Technology (CSET) · 17 June 2024
cset.georgetown.edu/publication/pushing-the-limits-huaweis-ai-chip-tests-u-s-export-controls/



01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Silicon and Wafers

Firms based in Japan, Taiwan, Germany and South Korea make most 300 mm wafers used for advanced chips. China makes most polysilicon, almost all of it for solar cells.



Specimen 02 · Silicon and Wafers

A silicon ingot, one crystal pulled whole from a melt, with two wafers sawn from it. It is 2.1 m long, 300 mm across and about 265 kg, taller than a door and about as heavy as three grown men. It hangs from a neck about 10 mm wide. Drawn to scale.

Parts, as numbered on the drawing

- ① Seed: lowered to the melt and drawn slowly back up
- ② Neck: keeps the seed's first flaws out of the ingot
- ③ Ingot: grown by Shin-Etsu Handotai (JP), SUMCO (JP), GlobalWafers (TW), SK Siltron (KR) and Siltronic (DE)
- ④ Wafers: sawn from the ingot, then lapped, etched and polished

In plain terms

Every chip is built on a wafer, a thin round slice of silicon about 30 centimeters across that carries hundreds of chips at once. Making one starts with quartz rock, which is silicon bound to oxygen¹. The silicon is refined until metal impurities are no more than a few parts per billion². It is then melted, and a small seed crystal is lowered to the

¹ Mineral Commodity Summaries 2026: Silicon. U.S. Geological Survey, 5 February 2026. pubs.usgs.gov

² SUMCO, production processes page. SUMCO, accessed 9 September 2026. sumcosi.com

surface and drawn slowly back up. The melt freezes onto the seed as one long cylinder, a single crystal with its atoms lined up in one unbroken pattern from end to end. Saws cut the cylinder into discs, and each disc is polished to a mirror finish and made extremely flat across its whole face². In 2025 the top five wafer makers served around 75 percent of the world market, and none of them is American or Chinese³.

In short

Japanese companies held 53 percent of the world's silicon wafer sales in 2023, by a Fuji Keizai survey that Japan's trade ministry reproduced⁴. Firms based in Taiwan, South Korea and Europe held most of the rest⁴. China's largest maker of 300 mm wafers, Eswin, says it ranked sixth in the world with about 7.7 percent of global 300 mm shipments in the first half of 2026⁵. Chips also need electronic-grade polysilicon, the raw material for wafers⁶. The German wafer maker Siltronic named five major suppliers of it for 2025, and none is Chinese⁶.

GlobalWafers of Taiwan opened a \$3.5 billion plant in Texas in May 2025, the first fully integrated plant for advanced silicon wafers built in the United States in over twenty years⁷. US Presidential Proclamation 11052 sets a minimum import price of \$100 per kilogram for polysilicon ingots and wafers from 4 December 2026⁸.

The world market for silicon wafers was \$11.4 billion in 2025, on 12,973 million square inches shipped⁹. That is a small fraction of Nvidia's data center revenue, which reached \$193.7 billion in the fiscal year to 25 January 2026¹⁰.

Chokepoint card			Silicon and Wafers
<div>Concentration</div> <div> High</div> <div>Four to six firms could supply this stage today, and the top two take most of the revenue.</div>	<div>Substitutability</div> <div>Moderate</div> <div>Several firms already make 300 mm wafers that fabs have approved, but customers have to test and approve a new wafer plant before they buy from it¹¹.</div>	<div>Price or market size</div> <div>\$11.4 billion</div> <div>world wafer market in 2025, on 12,973 million square inches shipped⁹</div>	

2 SUMCO, production processes page. SUMCO, accessed 9 September 2026. [sumcosi.com](#)

3 Investor Presentation: Foundation of Digital Life. Siltronic, April 2026, p. 6. [siltronic.com](#)

4 METI, Semiconductor and digital industry strategy: future direction... Ministry of Economy, Trade and Industry (Japan), 23 December 2025, p. 8. [meti.go.jp](#)

5 西安奕斯伟材料科技股份有限公司2026年半年度报告. CNINFO, 25 August 2026, p. 18. [static.cninfo.com.cn](#)

6 Investor Presentation: Foundation of Digital Life. Siltronic, April 2026, p. 5. [siltronic.com](#)

7 GlobalWafers America Officially Opens for Business. GlobalWafers, 15 May 2025. [sas-globalwafers.com](#)

8 Adjusting Imports of Polysilicon and Its Derivatives Into the United States. Federal Register, 11 August 2026. [federalregister.gov](#)

9 SEMI Reports 2025 Annual Worldwide Silicon Wafer Shipments and Revenue Results. PR Newswire, 10 February 2026. [prnewswire.com](#)

10 NVIDIA Announces Financial Results for Fourth Quarter and Fiscal 2026. Nvidia, 25 February 2026. [nvidianews.nvidia.com](#)

11 Investor Presentation: Foundation of Digital Life. Siltronic, April 2026, p. 12. [siltronic.com](#)

Who leads	JP	Shin-Etsu Handotai	Its parent's electronics materials segment, wafers included, had ¥1,015.7 billion of sales in the year to March 2026 ¹²
	JP	SUMCO	¥409,670 million of net sales in 2025 ¹³
	TW	GlobalWafers	NT\$60.6 billion revenue in 2025 ¹⁴
	KR	SK Siltron	One of the top five wafer makers by revenue in the first three quarters of 2025 ³
	DE	Siltronic	€1,346.7 million revenue in 2025 ¹⁵
Where it is made	JP	Japan	Shin-Etsu and SUMCO crystal growth and polishing
	TW	Taiwan	GlobalWafers headquarters and plants
	DE	Germany	Siltronic plants in Burghausen and Freiberg, and Wacker semiconductor-grade polysilicon
	KR	South Korea	SK Siltron
	US	United States	Hemlock polysilicon in Michigan, and GlobalWafers plants in Sherman, Texas and St Peters, Missouri
Why substitution is possible	Losing one of the top five wafer makers leaves four, and a new wafer plant can still be built ³ . Customer approval of a new plant is called qualification ¹¹ . Siltronic completed key customer qualifications at its new Singapore fab in July 2025 ¹¹ .		
Where China stands		Where the US stands	
China made about 93 percent of the world's polysilicon in 2023, and an estimated 98 percent of China's output was solar-grade ¹⁶ . Eswin, mainland China's largest maker of 300 mm wafers, says it had about 7.7 percent of world 300 mm shipments in the first half of 2026 ⁵ .		None of the five largest wafer makers in 2025 was American ³ . GlobalWafers of Taiwan won CHIPS awards of up to \$406 million in December 2024 for wafer plants in Texas and Missouri ¹⁷ .	

3 Investor Presentation: Foundation of Digital Life. Siltronic, April 2026, p. 6. [siltronic.com](https://www.siltronic.com)

5 西安奕斯伟材料科技股份有限公司2026年半年度报告. CNINFO, 25 August 2026, p. 18. static.cninfo.com.cn

11 Investor Presentation: Foundation of Digital Life. Siltronic, April 2026, p. 12. [siltronic.com](https://www.siltronic.com)

12 Consolidated Financial Results for the Fiscal Year Ended March 31, 2026. Shin-Etsu Chemical, 27 April 2026, p. 6. [shinetsu.co.jp](https://www.shinetsu.co.jp)

13 Notice of Convocation of the 27th Ordinary General Meeting of Shareholders. SUMCO, 6 March 2026, p. 24. [sumcosi.com](https://www.sumcosi.com)

14 GlobalWafers Reports Full Year 2025 Results. GlobalWafers, 3 March 2026. [sas-globalwafers.com](https://www.sas-globalwafers.com)

15 Siltronic AG: Robust business performance in 2025 demonstrates resilience... Siltronic, 27 August 2026. [siltronic.com](https://www.siltronic.com)

16 2023 Minerals Yearbook: China (advance release). U.S. Geological Survey, February 2026, p. 7. pubs.usgs.gov

17 Biden-Harris Administration Announces CHIPS Incentives Awards with GlobalWafers... NIST, 17 December 2024. [nist.gov](https://www.nist.gov)

01

How silicon wafers are made

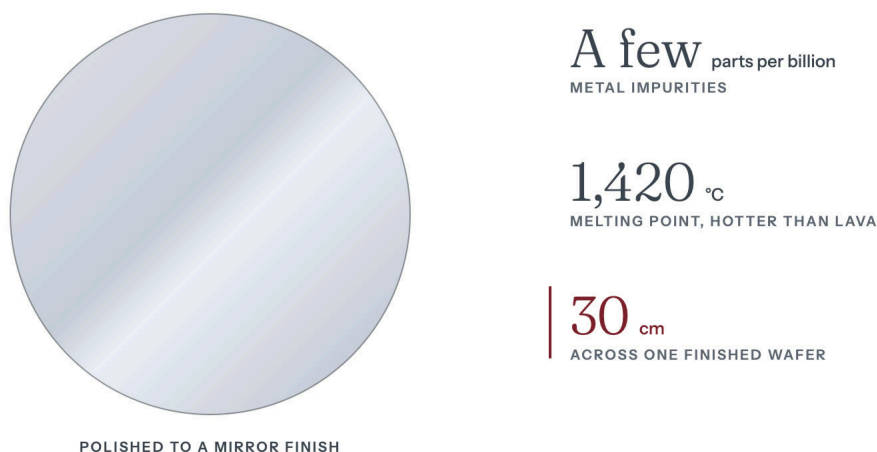
An arc furnace melts the quartz rock with carbon, and the carbon takes the oxygen away as gas, leaving rough silicon metal. Refiners turn the metal into a gas, trichlorosilane, and distill it, because the impurities boil at other temperatures and separate out.

In the next step, the Siemens process, the clean gas flows over silicon filaments heated inside a bell jar. On the hot surface the gas breaks apart and its silicon settles onto the filaments. Over days the filaments thicken into gray rods of polysilicon. Everything downstream is made from those rods. Polysilicon comes in two ultra-high-purity grades, one for semiconductors and one for solar cells, and chips use the semiconductor grade¹.

A grower melts the polysilicon at about 1,420 degrees Celsius, hotter than lava, and pulls a single crystal out of it by the Czochralski method². The grower lowers a small seed crystal on the end of a rod to the surface of the melt and draws it back up, slowly turning. Silicon freezes onto the seed in the seed's own atomic pattern, and a cylinder, the ingot, grows beneath it. The pull starts with a thin neck so that flaws from the seed's first contact with the melt stay in the neck and never reach the ingot. Boron or phosphorus is stirred into the melt, a step called doping. The added element sets how readily the wafer conducts and whether negative or positive charges carry its current.

Figure 02.1 • Explainer, 20 seconds

From sand to wafer



1. **Refine.** Silicon starts as quartz rock. It is refined into rods so pure that metal impurities are no more than a few parts per billion.
2. **Grow.** The rods are melted. A seed crystal touches the melt and is drawn slowly up, turning, and the silicon freezes onto it as one long crystal.
3. **Slice.** A wire saw slices the crystal, called an ingot, into thin discs.

¹ Mineral Commodity Summaries 2026: Silicon. U.S. Geological Survey, 5 February 2026. pubs.usgs.gov

² SUMCO, production processes page. SUMCO, accessed 9 September 2026. sumcosi.com

4. **Polish.** Each disc is ground, etched and polished to a mirror finish, flat right out to the edge.

Note: Simplified. The ingot and the machines are not drawn to scale.

A wire saw, a web of fine wire running through abrasive, slices the ingot into discs. The maker then laps each disc, grinding both faces flat between rotating plates. It etches off the damaged surface with chemicals, then polishes the disc to a mirror with colloidal silica, a slurry of silica particles far too small to see. Almost every step throws material away.

Epitaxial wafers get one more layer of near-perfect silicon, grown on top at about 1,200 degrees Celsius². That is still hot enough to glow orange.

02

Types of silicon wafers

Polished versus epitaxial

A polished wafer is a doped single crystal polished to a mirror finish². An epitaxial wafer is a polished wafer with a thin layer of single-crystal silicon grown on top². The transistors are built in that layer, so flaws in it can make them leak current. SUMCO says an epitaxial wafer suits customers who need a near-perfect crystal or layers that differ in electrical resistance². SEMI, the industry association, credits the 2025 rise in shipments to AI-driven demand for advanced epitaxial wafers for logic chips and polished wafers for high-bandwidth memory⁹.

Silicon on insulator

In a silicon-on-insulator (SOI) wafer, a buried layer of oxide, which is glass, separates a thin working layer of silicon from the bulk beneath. Soitec says nearly all SOI wafers sold worldwide are made with its Smart Cut process¹⁸. Soitec's SOI product lines include RF-SOI for radio chips and fully depleted SOI (FD-SOI)¹⁸. Its markets run from mobile communications to cloud AI¹⁸. But for logic chips, SEMI credited the AI-driven growth in 2025 to a different kind of wafer, the advanced epitaxial wafer⁹.

03

Who makes silicon wafers and polysilicon

The Center for Security and Emerging Technology (CSET) at Georgetown University named five key wafer firms in a January 2021 brief¹⁹. They were Shin-Etsu and SUMCO of Japan, GlobalWafers of Taiwan, Siltronic of Germany and SK Siltron of South Korea¹⁹. CSET also listed nine Chinese-owned producers, among them Zhonghuan, Simgui, ZingSEMI and Okmetic, a Finnish firm bought by a Chinese state investment

² SUMCO, production processes page. SUMCO, accessed 9 September 2026. sumcosi.com

⁹ SEMI Reports 2025 Annual Worldwide Silicon Wafer Shipments and Revenue Results. PR Newswire, 10 February 2026. prnewswire.com

¹⁸ Soitec, key figures. Soitec, accessed 9 September 2026. soitec.com

¹⁹ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 55. cset.georgetown.edu

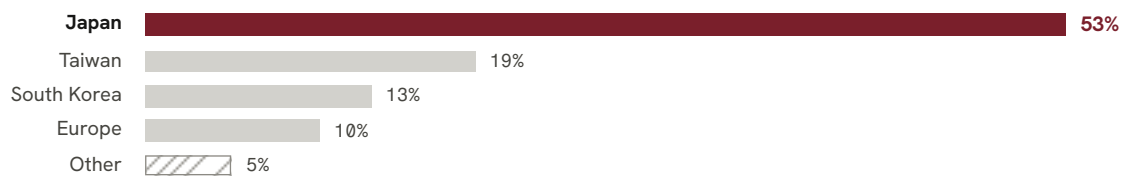
fund¹⁹. It said Chinese wafer producers made little revenue compared with the five key firms²⁰.

China's 300 mm wafer industry has grown since 2018. As of 2018, five Chinese firms were making or planning 300 mm wafers²⁰. In its October 2025 listing prospectus, Eswin, a Chinese wafer maker, counts seven Chinese firms, itself included, making 300 mm wafers at scale²¹. Their combined capacity was 2.94 million wafers a month at the end of 2024²¹.

Figure 02.2

Companies based in Japan held 53 percent of 2023 wafer sales

Silicon wafer sales by supplier headquarters, 2023. The source shows no separate share for China or the United States



Source: METI, December 2025, from Fuji Keizai data (2023). Japan's and Europe's shares are printed, and the others are read off METI's chart [4]

Japanese companies held 53 percent of the world's silicon wafer sales in 2023⁴. The shares come from a survey of 2023 sales by Fuji Keizai, a Japanese research firm⁴. Japan's Ministry of Economy, Trade and Industry reproduced the figures in a December 2025 strategy deck⁴. The ministry's chart of the survey prints only Japan's 53 percent, so the other shares are measured from its bars⁴. An earlier page of the ministry's deck prints Europe's share in the same Fuji Keizai survey as 10 percent²². The ministry's figures give no separate share to Chinese or US companies⁴.

Siltronic's April 2026 investor presentation says the top five wafer makers serve around 75 percent of the market, based on revenue in the first three quarters of 2025³. It names the five as Shin-Etsu, SUMCO, GlobalWafers, SK Siltron and Siltronic itself³. Siltronic describes itself as the only Western-based maker among the five³.

The wafer makers' 2025 results show strong AI demand and weak demand for chips made on older, mature nodes.

- **Shin-Etsu.** Shin-Etsu Chemical's electronics materials segment, which includes its wafer business, sold ¥1,015.7 billion in the year to March 2026, up 9 percent¹². AI-related demand stayed strong and demand in other sectors began to rise, lifting sales of silicon wafers, photoresist and photomask blanks¹². The segment also sells rare earth magnets and other materials, and the results release does not break out

³ Investor Presentation: Foundation of Digital Life. Siltronic, April 2026, p. 6. siltronic.com

⁴ METI, Semiconductor and digital industry strategy: future direction... Ministry of Economy, Trade and Industry (Japan), 23 December 2025, p. 8. meti.go.jp

¹² Consolidated Financial Results for the Fiscal Year Ended March 31, 2026. Shin-Etsu Chemical, 27 April 2026, p. 6. shinetsu.co.jp

¹⁹ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 55. cset.georgetown.edu

²⁰ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 57. cset.georgetown.edu

²¹ 西安奕材首次公开发行股票并在科创板上市招股说明书. CNINFO, 22 October 2025, p. 138. static.cninfo.com.cn

²² METI, Semiconductor and digital industry strategy: future direction... Ministry of Economy, Trade and Industry (Japan), 23 December 2025, p. 4. meti.go.jp

wafer sales²³. So the figure cannot be compared with the wafer revenue of the other firms listed.

- **SUMCO.** Sold ¥409,670 million²⁴. Its operating profit fell from ¥36,924 million to ¥1,342 million, and it ended the year with a net loss of ¥11,751 million²⁴. In the same year it added leading-edge 300 mm capacity and reorganized production of 200 mm and smaller wafers, where demand stayed weak¹³.
- **Siltronic.** Lost €77.9 million on €1,346.7 million of sales while investing €369.1 million, with its new Singapore fab as the focus¹⁵.
- **GlobalWafers.** NT\$60.6 billion of revenue, down 3.24 percent in local currency¹⁴.

Worldwide, the wafer area shipped rose 5.8 percent in 2025, but revenue fell 1.2 percent⁹. SEMI attributes the softer revenue mostly to traditional chip uses outside AI, where demand and pricing had yet to improve⁹.

Polysilicon is the raw material for both wafers and solar cells, and almost all of China's is made for solar cells. In 2023 China made 1.50 million metric tons of polysilicon, about 93 percent of world output¹⁶. Solar-grade material was an estimated 98 percent of that output and electronic-grade 2 percent¹⁶. The US Commerce Department found in 2026 that semiconductor-grade polysilicon makes up only 2.4 percent of global production, close to the electronic-grade share of China's output⁸. These figures do not show how much of China's electronic-grade polysilicon ends up in chips.

Figure 02.3

An estimated 98 percent of China's 2023 polysilicon was solar-grade

China's polysilicon output by grade, 2023. China made 1.50 million metric tons that year, about 93 percent of world output



Source: USGS Minerals Yearbook, China, 2023 [16]

Siltronic put the 2025 market for electronic-grade silicon at \$1.4 billion, with five major suppliers, none of them Chinese: Wacker, Hemlock, OCI, Tokuyama and Mitsubishi⁶.

GlobalWafers of Taiwan has expanded its wafer making in the United States. It opened a \$3.5 billion plant in Sherman, Texas in May 2025, the first fully integrated plant for advanced silicon wafers built in the United States in over twenty years⁷. The same day it announced another \$4 billion for phases three and four in Sherman⁷. The US government had awarded it up to \$406 million under the CHIPS incentives program for wafer plants in Texas and Missouri¹⁷.

6 Investor Presentation: Foundation of Digital Life. Siltronic, April 2026, p. 5. siltronic.com

7 GlobalWafers America Officially Opens for Business. GlobalWafers, 15 May 2025. sas-globalwafers.com

8 Adjusting Imports of Polysilicon and Its Derivatives Into the United States. Federal Register, 11 August 2026. federalregister.gov

9 SEMI Reports 2025 Annual Worldwide Silicon Wafer Shipments and Revenue Results. PR Newswire, 10 February 2026. prnewswire.com

13 Notice of Convocation of the 27th Ordinary General Meeting of Shareholders. SUMCO, 6 March 2026, p. 24. sumcosi.com

14 GlobalWafers Reports Full Year 2025 Results. GlobalWafers, 3 March 2026. sas-globalwafers.com

15 Siltronic AG: Robust business performance in 2025 demonstrates resilience... Siltronic, 27 August 2026. siltronic.com

16 2023 Minerals Yearbook: China (advance release). U.S. Geological Survey, February 2026, p. 7. pubs.usgs.gov

17 Biden-Harris Administration Announces CHIPS Incentives Awards with GlobalWafers... NIST, 17 December 2024. nist.gov

23 Consolidated Financial Results for the Fiscal Year Ended March 31, 2026. Shin-Etsu Chemical, 27 April 2026, p. 20. shinetsu.co.jp

24 Notice of Convocation of the 27th Ordinary General Meeting of Shareholders. SUMCO, 6 March 2026, p. 26. sumcosi.com

US import rules issued in 2026 on polysilicon products also cover the single-crystal wafers that chips are built on. US Presidential Proclamation 11052, signed 6 August 2026, sets a minimum import price of \$100 per kilogram for polysilicon ingots and wafers from 4 December 2026⁸. From the same date it adds an extra 15 percent duty on imported ingots and other listed products made from polysilicon⁸. A September 2026 US Commerce Department rule meant to stop stockpiling before the duties start lists tariff code 3818.00.0040 among the products it covers²⁵. That code covers round, doped, single-crystal silicon wafers²⁶.

The US Commerce Department may approve plans to build US polysilicon, ingot, wafer or solar cell plants whose construction starts by 20 January 2029⁸. Firms with approved plans can import production equipment, and polysilicon, ingots, wafers and solar cells in amounts the department sets to match their new investment, without the new duties⁸.

04

Why 300 mm wafers are a chokepoint

Almost all fab capacity for advanced chips runs on 300 mm wafers²⁰. In 2025 the top five wafer makers served around 75 percent of the world market, and none of them is American or Chinese³. Losing one of the top five would leave four, and a new wafer plant can still be built³. But customers have to qualify a new plant before they buy from it, and Siltronic completed key customer qualifications at its new Singapore fab in July 2025¹¹.

China makes most of the world's polysilicon, but as of 2019 Chinese firms held under 5 percent of the wafer market and under 1 percent of the 300 mm market¹⁹. As of 2018, Chinese producers made 12 percent of the wafers for Chinese-headquartered 300 mm fabs, against 18 percent for 100 to 200 mm fabs²⁷.

Eswin, mainland China's largest maker of 300 mm wafers, says it ranked sixth in the world with about 7.7 percent of global 300 mm shipments in the first half of 2026⁵. Its October 2025 Shanghai listing prospectus, drawing on SEMI data, estimates that the five largest makers shipped 79.08 percent of 300 mm wafers in 2024²⁸. It puts Eswin at 6.01 percent and all other makers at 14.91 percent²⁸.

Making the smoothest, high-purity 300 mm wafers takes considerable know-how that is hard to write down²⁰.

³ Investor Presentation: Foundation of Digital Life. Siltronic, April 2026, p. 6. siltronic.com

⁵ 西安奕斯伟材料科技股份有限公司2026年半年度报告. CNINFO, 25 August 2026, p. 18. static.cninfo.com.cn

⁸ Adjusting Imports of Polysilicon and Its Derivatives Into the United States. Federal Register, 11 August 2026. [federalregister.gov](https://www.federalregister.gov)

¹¹ Investor Presentation: Foundation of Digital Life. Siltronic, April 2026, p. 12. siltronic.com

¹⁹ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 55. cset.georgetown.edu

²⁰ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 57. cset.georgetown.edu

²⁵ Measures To Restrict Stockpiling of Polysilicon and Polysilicon Derivatives... Federal Register, 24 September 2026. [federalregister.gov](https://www.federalregister.gov)

²⁶ Harmonized Tariff Schedule, heading 3818.00.00. U.S. International Trade Commission, accessed 9 September 2026. hts.usitc.gov

²⁷ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 58. cset.georgetown.edu

²⁸ 西安奕材首次公开发行股票并在科创板上市招股说明书. CNINFO, 22 October 2025, p. 145. static.cninfo.com.cn

In SEMI figures from November 2020 cited by CSET, 99.7 percent of world fab capacity at 45 nm and below used 300 mm wafers²⁰. SEMI estimated that 300 mm wafers made up about 78.8 percent of all wafer area shipped worldwide in 2025, according to Eswin's 2025 annual report summary²⁹.

The last increase in wafer size, to 300 mm, happened in 2002³⁰. Wafers are still produced in diameters of up to 300 mm⁹. Bigger wafers cut the cost of deposition, etching and other steps, because those steps have to be run fewer times for the same number of chips³⁰. So printing, or photolithography, takes a bigger share of the processing cost³⁰. A 2013 University of Texas lecture cited by CSET put photolithography at half the cost of processing a 300 mm wafer, against a quarter for a 150 mm one³⁰.

Large GPU dies and the newest processes need better wafers. Some GPU dies fill the whole area a lithography tool can print in one exposure. One fatal defect on such a die ruins far more silicon than one on a small chip. Extreme-ultraviolet printing also stays in focus over only a tiny range of heights (see Lithography), so the disc has to be flat at every point. SEMI's wafer group says the move to sub-3nm processes is raising requirements for wafer quality and consistency⁹.

Five questions to answer from memory

1. What is a wafer? see How it works
 2. How is the silicon for a wafer made? see How it works
 3. Who makes most of the world's wafers? see How it works
 4. Why can a chip factory not switch wafer suppliers quickly? see Chokepoint card
 5. Why do AI chips need especially good wafers? see The chokepoint
-

Four things to remember

- Every chip starts on a wafer, a polished disc of pure silicon about 30 centimeters across.
 - The top five wafer makers, in Japan, Taiwan, Germany and South Korea, served around 75 percent of the market in 2025.
 - Customers have to test and approve a new wafer plant before they buy from it.
 - China makes most of the world's polysilicon, but none of the five major suppliers of electronic-grade silicon, the grade chips need, is Chinese.
-

Sources (30)

1. A Mineral Commodity Summaries 2026: Silicon. U.S. Geological Survey · 5 February 2026
pubs.usgs.gov/periodicals/mcs2026/mcs2026-silicon.pdf
2. A SUMCO, production processes page. SUMCO · Accessed 9 September 2026
www.sumcosi.com/english/products/process/

⁹ SEMI Reports 2025 Annual Worldwide Silicon Wafer Shipments and Revenue Results. PR Newswire, 10 February 2026.
prnewswire.com

²⁰ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 57.
cset.georgetown.edu

²⁹ 西安奕斯伟材料科技股份有限公司2025年年度报告摘要. CNINFO, 21 April 2026, p. 8. static.cninfo.com.cn

³⁰ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 80.
cset.georgetown.edu

3. A **Investor Presentation: Foundation of Digital Life.** Siltronic · April 2026 · p. 6
www.siltronic.com/fileadmin/investorrelations/2026/Q1/20260429_Siltronic_InvestorPresentation__.pdf#page=6
4. A **METI, Semiconductor and digital industry strategy: future direction (半導体・デジタル産業戦略の今後の方向性),** 23 December 2025. Ministry of Economy, Trade and Industry (Japan) · 23 December 2025 · p. 8
www.meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/0014/handeji14-4.pdf#page=8
5. A **西安奕斯伟材料科技股份有限公司2026年半年度报告.** CNINFO · 25 August 2026 · p. 18
static.cninfo.com.cn/finalpage/2026-08-26/1225503057.PDF#page=18
6. A **Investor Presentation: Foundation of Digital Life.** Siltronic · April 2026 · p. 5
www.siltronic.com/fileadmin/investorrelations/2026/Q1/20260429_Siltronic_InvestorPresentation__.pdf#page=5
7. A **GlobalWafers America Officially Opens for Business.** GlobalWafers · 15 May 2025
www.sas-globalwafers.com/en/gwc_news_en_20250516/
8. A **Adjusting Imports of Polysilicon and Its Derivatives Into the United States.** Federal Register (Executive Office of the President) · 11 August 2026
www.federalregister.gov/documents/2026/08/11/2026-16400/adjusting-imports-of-polysilicon-and-its-derivatives-into-the-united-states
9. A **SEMI Reports 2025 Annual Worldwide Silicon Wafer Shipments and Revenue Results.** PR Newswire · 10 February 2026
www.prnewswire.com/news-releases/semi-reports-2025-annual-worldwide-silicon-wafer-shipments-and-revenue-results-302683028.html
10. A **NVIDIA Announces Financial Results for Fourth Quarter and Fiscal 2026.** Nvidia · 25 February 2026
nvidianews.nvidia.com/news/nvidia-announces-financial-results-for-fourth-quarter-and-fiscal-2026
11. A **Investor Presentation: Foundation of Digital Life.** Siltronic · April 2026 · p. 12
www.siltronic.com/fileadmin/investorrelations/2026/Q1/20260429_Siltronic_InvestorPresentation__.pdf#page=12
12. A **Consolidated Financial Results for the Fiscal Year Ended March 31, 2026.** Shin-Etsu Chemical · 27 April 2026 · p. 6
www.shinetsu.co.jp/wp-content/uploads/2025/07/20260428_con_E.pdf#page=6
13. A **Notice of Convocation of the 27th Ordinary General Meeting of Shareholders.** SUMCO · 6 March 2026 · p. 24
www.sumcosi.com/english/pdf/ir/library/shareholders/27/pdf/nc_e_27.pdf#page=24
14. A **GlobalWafers Reports Full Year 2025 Results.** GlobalWafers · 3 March 2026
www.sas-globalwafers.com/en/gwc_news_en_20260303/
15. A **Siltronic AG: Robust business performance in 2025 demonstrates resilience despite challenging conditions.** Siltronic · 27 August 2026
www.siltronic.com/en/press/press-releases/siltronic-ag-robust-business-performance-in-2025-demonstrates-resilience-despite-challenging-conditions.html
16. A **2023 Minerals Yearbook: China (advance release).** U.S. Geological Survey · February 2026 · p. 7
pubs.usgs.gov/myb/vol13/2023/myb3-2023-china.pdf#page=7
17. A **Biden-Harris Administration Announces CHIPS Incentives Awards with GlobalWafers to Support Domestic Production of Silicon Wafers.** NIST · 17 December 2024
www.nist.gov/news-events/news/2024/12/biden-harris-administration-announces-chips-incentives-awards-globalwafers
18. A **Soitec, key figures.** Soitec · Accessed 9 September 2026
www.soitec.com/home/group
19. A **The Semiconductor Supply Chain - Issue Brief.** Center for Security and Emerging Technology (CSET) · 21 January 2021 · p. 55
cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf#page=55
20. A **The Semiconductor Supply Chain - Issue Brief.** Center for Security and Emerging Technology (CSET) · 21 January 2021 · p. 57
cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf#page=57
21. A **西安奕材首次公开发行股票并在科创板上市招股说明书.** CNINFO · 22 October 2025 · p. 138
static.cninfo.com.cn/finalpage/2025-10-22/1224723727.PDF#page=138
22. A **METI, Semiconductor and digital industry strategy: future direction (半導体・デジタル産業戦略の今後の方向性),** 23 December 2025. Ministry of Economy, Trade and Industry (Japan) · 23 December 2025 · p. 4
www.meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/0014/handeji14-4.pdf#page=4
23. A **Consolidated Financial Results for the Fiscal Year Ended March 31, 2026.** Shin-Etsu Chemical · 27 April 2026 · p. 20
www.shinetsu.co.jp/wp-content/uploads/2025/07/20260428_con_E.pdf#page=20
24. A **Notice of Convocation of the 27th Ordinary General Meeting of Shareholders.** SUMCO · 6 March 2026 · p. 26
www.sumcosi.com/english/pdf/ir/library/shareholders/27/pdf/nc_e_27.pdf#page=26
25. A **Measures To Restrict Stockpiling of Polysilicon and Polysilicon Derivatives Under Proclamation 11052.** Federal Register (Commerce Department; Industry and Security Bureau) · 24 September 2026
www.federalregister.gov/documents/2026/09/24/2026-19537/measures-to-restrict-stockpiling-of-polysilicon-and-polysilicon-derivatives-under-proclamation-11052
26. A **Harmonized Tariff Schedule, heading 3818.00.00.** U.S. International Trade Commission · Accessed 9 September 2026
hts.usitc.gov/search?query=3818.00.00
27. A **The Semiconductor Supply Chain - Issue Brief.** Center for Security and Emerging Technology (CSET) · 21 January 2021 · p. 58
cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf#page=58
28. A **西安奕材首次公开发行股票并在科创板上市招股说明书.** CNINFO · 22 October 2025 · p. 145
static.cninfo.com.cn/finalpage/2025-10-22/1224723727.PDF#page=145
29. A **西安奕斯伟材料科技股份有限公司2025年年度报告摘要.** CNINFO · 21 April 2026 · p. 8
static.cninfo.com.cn/finalpage/2026-04-21/1225128957.PDF#page=8

30. A **The Semiconductor Supply Chain - Issue Brief**. Center for Security and Emerging Technology (CSET) · 21 January 2021 · p. 80
cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf#page=80



01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Chemicals, Gases and Photoresist

Japanese companies held 78 percent of world photoresist sales in 2023. Supply of chip chemicals, gases and metals has been disrupted three times since 2019.

Specimen 03 · Chemicals, Gases and Photoresist

A specialty gas cabinet with its door off, and a bulk liquid cylinder standing behind it. The cabinet is about 1 m wide and 1.9 m tall and holds three gas cylinders. The drawing is to scale. The steel-gray panel on the back wall holds the valves, regulator and gauges that control the gas flow.

In plain terms

Photoresist is a coating that changes wherever light hits it. A machine spins a coat of it, thinner than a soap bubble, across the wafer. Light shines through a stencil onto the coat, and a liquid wash then takes away the parts the light reached. What remains is a pattern, and the next machine cuts that pattern into the wafer beneath, a step called etching. Hundreds of other chemicals, gases and materials lay down layers, strip them off and clean the wafer between steps¹. The cleaning chemicals are purified until metal and other impurities are down to parts per trillion, the Japanese chemical maker Sumitomo Chemical said in 2021². A chipmaker has to test and approve each new resist in its own factory before using it³. Even a resist that passes the first time takes seven to 17 months to approve, the Semiconductor Industry Association wrote in 2023³. Japanese companies held 78 percent of world photoresist sales in 2023, by a Fuji Keizai survey that Japan's trade ministry reproduced⁴.

In short

In July 2019 Japan began requiring an export license for each contract to sell photoresist, hydrogen fluoride or fluorinated polyimide to South Korea⁵. Japan's hydrogen fluoride exports to South Korea then fell 87.9 percent, but

¹ Testimony of the Semiconductor Industry Association (SIA) before the Senate... U.S. Senate Committee on Environment and Public Works, 4 March 2026, p. 6. epw.senate.gov

² Sumitomo Chemical to Expand Production Capacity for High-Purity Chemicals for... Sumitomo Chemical, 24 August 2021. sumitomo-chem.co.jp

³ PFAS-Containing Photo-Acid Generators Used in Semiconductor Manufacturing. Semiconductor Industry Association, 8 June 2023, p. 22. semiconductors.org

⁴ METI, Semiconductor and digital industry strategy: future direction... Ministry of Economy, Trade and Industry (Japan), 23 December 2025, p. 8. meti.go.jp

⁵ The impact of export controls on international trade: evidence from the... Research Institute of Economy, Trade and Industry, 8 May 2023. rieti.go.jp

its photoresist exports did not⁵. Production of all three chemicals rose inside South Korea⁵.

China banned exports of the metals gallium, germanium and antimony to the United States in December 2024⁶. In Europe, germanium metal averaged an estimated \$4,100 a kilogram in 2025, against \$1,392 in 2023, on Argus Media prices reported by the US Geological Survey⁷. In November 2025 China suspended the ban until 27 November 2026⁸.

A chip fab draws on hundreds of chemicals, gases and other materials¹. A shortage of any one of them can stop it. The French gas company Air Liquide alone supplies more than 200 different chemicals and roughly 50,000 cylinders a year⁹.

Chokepoint card

Chemicals, Gases and Photoresist

Concentration

 **High**

Four to six firms could supply this stage today, and the top two take most of the revenue.

Substitutability

Moderate

This rating is based on photoresist, the hardest input to replace at this stage¹⁰.

Price or market size

\$45.8 billion

market for wafer fabrication materials in 2025¹¹. SEMI's count includes silicon wafers and photomasks¹²

Who leads	JP	JSR	A vehicle of the state-backed Japan Investment Corporation bought 84.36 percent of JSR in April 2024 ¹³
	JP	Tokyo Ohka Kogyo	Resist maker with ¥139,668 million of sales in the first half of fiscal 2026 ¹⁴
	FR	Air Liquide	€2,465 million of electronics revenue in 2025, 9.1 percent of group sales ⁹
	US	Entegris	Bought the polishing-slurry maker CMC Materials in July 2022 ¹⁵
	JP	JX Advanced Metals	Says it holds about 65 percent of the world market for semiconductor sputtering targets as of fiscal 2026 ¹⁶
Where it is made	JP	Japan	Photoresist, ultra-pure hydrofluoric acid, sputtering targets, polishing slurries
	US	United States	Entegris polishing slurries, Qnity Electronics resist, Air Products gases
	FR	France	Air Liquide electronics gases and precursors
	KR	South Korea	Dongjin resist, with output of resist and hydrogen fluoride rising after 2019
	CN	China	Gallium, germanium and antimony refining

1 Testimony of the Semiconductor Industry Association (SIA) before the Senate... U.S. Senate Committee on Environment and Public Works, 4 March 2026, p. 6. epw.senate.gov

5 The impact of export controls on international trade: evidence from the... Research Institute of Economy, Trade and Industry, 8 May 2023. rieti.go.jp

6 商务部公告2024年第46号 关于加强相关两用物项对美国出口管制的公告. Ministry of Commerce of the People's Republic of China, 3 December 2024. mofcom.gov.cn

7 Mineral Commodity Summaries 2026: Germanium. U.S. Geological Survey, 5 February 2026. pubs.usgs.gov

8 商务部公告2025年第72号 公布调整实施商务部公告2024年第46号的决定. Ministry of Commerce of the People's Republic of China, 9 November 2025. mofcom.gov.cn

9 Air Liquide, electronics page. Air Liquide, accessed 9 September 2026. airliquide.com

10 PFAS-Containing Photo-Acid Generators Used in Semiconductor Manufacturing. Semiconductor Industry Association, 8 June 2023, p. 21. semiconductors.org

11 Global Semiconductor Materials Market Revenue Reaches Record \$73.2 Billion in... PR Newswire, 12 May 2026. prnewswire.com

12 Materials Market Data Subscription (MMDS). SEMI, accessed 20 October 2026. semi.org

13 Announcement Regarding Result of Tender Offer for JSR Corporation (Securities... Japan Investment Corporation, 17 April 2024. jiccapital.co.jp

14 Consolidated Financial Results for the Second Quarter (Interim) of the Fiscal... Tokyo Ohka Kogyo, 6 August 2026, p. 4. tok.co.jp

15 Entegris, current report on Form 8-K dated 6 July 2022. U.S. Securities and Exchange Commission, 6 July 2022. sec.gov

16 Quick Guide to JX Advanced Metals. JX Advanced Metals, accessed 9 September 2026. jx-nmm.com

Why substitution is possible

Each formula is tuned to the layers it prints and has to pass qualification in the fab¹⁰. So a new supplier has to develop its version together with the fab, one layer at a time³. When Japan required individual export licenses for resist and two other chemicals sold to South Korea in 2019, South Korea bought more hydrogen fluoride from the United States and Taiwan and more resist from Belgium⁵.

Where China stands

In March 2026 the Chinese resist maker Hubei Dinglong said China had yet to reach large-scale production of advanced resist for 248 nm, 193 nm or extreme-ultraviolet printing¹⁷. Since August 2023 China has required licenses to export gallium and germanium¹⁸.

Where the US stands

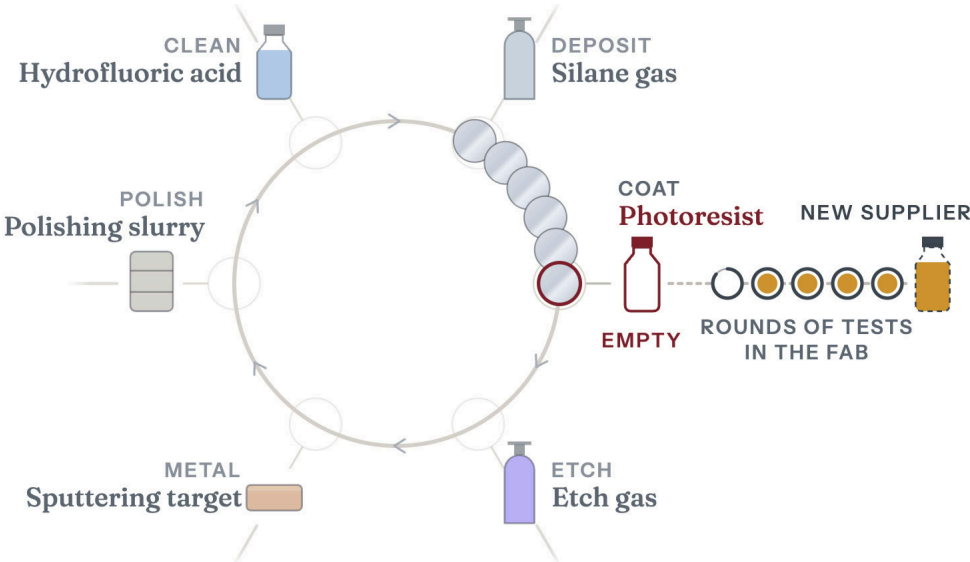
In photoresist, American companies ranked a distant second to Japanese companies by sales in 2023⁴. In 2021 JSR of Japan agreed to buy Inpria, an Oregon-based US maker of resist for extreme ultraviolet¹⁹.

01

How photoresist and chip chemicals work

Figure 03.1 · Explainer, 25 seconds

Why one missing material can stop a fab



- 1. **One layer.** A chip is built up in layers. For each layer the wafer goes around a loop of steps like this one, and each step uses its own chemical, gas or metal.
- 2. **Many wafers.** A fab runs many wafers at once, so every material is always in use. Deliveries keep each stock topped up.
- 3. **One runs out.** If one material stops arriving, the fab works through its stock.
- 4. **The fab stops.** When the stock runs out, wafers pile up at that step, and the rest of the fab stands idle.

3 PFAS-Containing Photo-Acid Generators Used in Semiconductor Manufacturing. Semiconductor Industry Association, 8 June 2023, p. 22. [semiconductors.org](https://www.semiconductors.org)

4 METI, Semiconductor and digital industry strategy: future direction... Ministry of Economy, Trade and Industry (Japan), 23 December 2025, p. 8. [meti.go.jp](https://www.meti.go.jp)

5 The impact of export controls on international trade: evidence from the... Research Institute of Economy, Trade and Industry, 8 May 2023. [rieti.go.jp](https://www.rieti.go.jp)

10 PFAS-Containing Photo-Acid Generators Used in Semiconductor Manufacturing. Semiconductor Industry Association, 8 June 2023, p. 21. [semiconductors.org](https://www.semiconductors.org)

17 湖北鼎龙控股股份有限公司2025年年度报告摘要. CNINFO, 27 March 2026, p. 2. static.cninfo.com.cn

18 商务部 海关总署公告2023年第23号 关于对镓、锗相关物项实施出口管制的公告. Ministry of Commerce of the People's Republic of China, 3 July 2023. [mofcom.gov.cn](https://www.mofcom.gov.cn)

19 JSR Agrees to Acquire EUV Pioneer Inpria Corporation. JSR Corporation, 17 September 2021. [jsr.co.jp](https://www.jsr.co.jp)

5. **A new supplier.** A new supplier's resist goes through round after round of tests in the fab. Even one that passes the first time takes seven to 17 months to approve.

Note: Simplified diagram. Six steps and their materials stand for the many a fab uses, and each real layer uses its own mix.

The resist has to change only where the light lands. It also has to work with very little light, so the scanner, the machine that projects the pattern, can expose each patch of the wafer in milliseconds.

Since the 1990s the standard has been chemically amplified resist. In resists for light with wavelengths of 248 nm and 193 nm, a photon absorbed in the film can free an acid molecule, and little more happens until the wafer is baked. In the bake, each acid molecule sets off hundreds of reactions around itself that turn the film soluble, so a little light does a lot of chemistry²⁰. The wash then takes away the exposed film and leaves the rest.

The 248 nm light comes from a krypton fluoride (KrF) laser. The 193 nm light comes from an argon fluoride (ArF) laser. Immersion scanners also pass it through a layer of water, which sharpens the image.

Chemically amplified resist works less well with extreme ultraviolet (EUV) light (see Lithography). An absorbed EUV photon instead knocks electrons loose, and a cascade of lower-energy secondary electrons makes the chemical changes in the resist²¹. A 13.5 nm EUV photon carries about fourteen times the energy of a 193 nm one, so the same dose of light arrives as far fewer photons. With fewer photons, random variation in where each one lands matters more. It shows up as ragged line edges and missing contact holes, the tiny holes that link one layer of a chip to the next.

Resist makers responded with metal-oxide resists, which are built on clusters with a tin-oxide core and absorb more of the EUV light than chemically amplified resists²². In 2021 the Japanese resist maker JSR agreed to buy Inpria, an Oregon-based US maker of these resists¹⁹.

The other chemicals and gases put material on the wafer, take it off or keep it clean. Bulk gases such as nitrogen come by pipeline or from plants built at the fab, and specialty gases come in cylinders⁹. Silane gas carries the silicon for new layers into the chamber that holds the wafer. A plasma splits nitrogen trifluoride, and the fluorine it frees scrubs the chamber walls clean between wafers. Hydrofluoric acid cleans the wafer itself. Polishing slurries grind each new layer flat before the next goes on.

Sputtering targets are slabs of pure metal. A plasma knocks atoms off them, and the atoms settle on the wafer as thin metal films, including the barrier and seed layers for copper wiring²³. Electroplating then fills in the copper wiring itself²⁴. Filters and wafer carriers keep contamination out.

⁹ Air Liquide, electronics page. Air Liquide, accessed 9 September 2026. airliquide.com

¹⁹ JSR Agrees to Acquire EUV Pioneer Inpria Corporation. JSR Corporation, 17 September 2021. jsr.co.jp

²⁰ PFAS-Containing Photo-Acid Generators Used in Semiconductor Manufacturing. Semiconductor Industry Association, 8 June 2023, p. 6. semiconductors.org

²¹ How Scientists Are Accelerating the Development of Next-Gen Microelectronics. Lawrence Berkeley National Laboratory, 21 August 2023. newscenter.lbl.gov

²² Inpria, company website. Inpria, accessed 9 September 2026. inpria.com

²³ Applied Materials, PVD technology page. Applied Materials, accessed 9 September 2026. appliedmaterials.com

²⁴ SABRE Product Family. Lam Research, 11 August 2017. lamresearch.com

02

Types of photoresist

Resist class	Wavelength	Where it is used	Limit
i-line novolak	365 nm	Packaging, mature nodes	Resolution
KrF chemically amplified	248 nm	Implant layers, thick films	Resolution
ArF immersion chemically amplified	193 nm	Most critical layers below 28 nm	Needs several exposures per layer
EUV chemically amplified	13.5 nm	Leading-edge single-exposure layers	Shot noise from too few photons
EUV metal-oxide	13.5 nm	High-NA tools, tightest pitches	Cost, defects, outgassing

Each resist class is made for one kind of lithography, such as EUV, ArF immersion, ArF, KrF or i-line²⁵.

03

Who makes photoresist, gases and chip chemicals

Japanese companies sell most of the world's photoresist, by two different counts. In a January 2021 brief, Georgetown University's Center for Security and Emerging Technology (CSET) put Japan's share of the semiconductor photoresist market at 90 percent, citing a 2019 estimate²⁵. The brief put most of the rest with US and South Korean firms²⁵. In a December 2025 strategy presentation, Japan's Ministry of Economy, Trade and Industry (METI) published figures from a separate survey by Fuji Keizai, a Japanese market research firm⁴. That survey counts sales by company nationality and puts Japanese companies at 77 percent in 2021 and 78 percent in 2023, with American and South Korean companies next⁴.

Figure 03.2

Japanese companies held 78 percent of photoresist sales in 2023

Photoresist sales share by company nationality, 2023



Source: METI, December 2025, from Fuji Keizai data [4]

CSET's January 2021 brief lists five Japanese resist makers: JSR, Tokyo Ohka Kogyo, Shin-Etsu Chemical, Fujifilm and Sumitomo Chemical²⁶. It also lists Dongjin of South Korea, four Chinese firms and three firms it counts as American: DuPont, EMD Performance Materials and Inpria²⁶. Qnity Electronics, the former DuPont electronics business, says in its 2025 annual report that it offers lithography materials for every wavelength, including EUV²⁷.

4 METI, Semiconductor and digital industry strategy: future direction... Ministry of Economy, Trade and Industry (Japan), 23 December 2025, p. 8. [meti.go.jp](https://www.meti.go.jp)

25 The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 59. cset.georgetown.edu

26 The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 56. cset.georgetown.edu

27 Qnity Electronics, annual report on Form 10-K for the fiscal year ended 31... U.S. Securities and Exchange Commission, 26 February 2026. [sec.gov](https://www.sec.gov)

In its 2025 annual report summary, the Chinese firm Hubei Dinglong said China had yet to reach large-scale production of advanced resist for 248 nm, 193 nm or EUV printing¹⁷. But it said three of its own resists for 248 nm and 193 nm printing had moved into stable volume supply²⁸.

A Japanese state-backed fund, Japan Investment Corporation, took control of JSR in April 2024. A company the fund controls bought 84.36 percent of JSR's shares at ¥4,350 each in an offer to all shareholders that closed on 16 April 2024¹³. JSR's shares were delisted from the Tokyo Stock Exchange on 25 June 2024²⁹.

Two Japanese suppliers tie their growth to demand for AI chips. Tokyo Ohka Kogyo sold ¥139,668 million in the first half of fiscal 2026, up 25.1 percent, as strong demand for AI servers in data centers raised demand for chips¹⁴. Fujifilm planned to raise its polishing-slurry capacity at Kumamoto in Japan by about 30 percent from January 2025, to meet demand driven by AI chips³⁰. It also scheduled new production and quality-evaluation equipment for EUV resist at Shizuoka in Japan and Pyeongtaek in South Korea to start in October 2025³¹.

World sales of wafer fabrication materials reached \$45.8 billion in 2025, and sales of packaging materials reached \$27.4 billion¹¹. SEMI counts silicon wafers and photomasks among wafer fabrication materials, along with resists, gases, chemicals and polishing materials¹².

In electronic gases, CSET named Merck, Air Products and Air Liquide as the market leaders in January 2021³². Air Liquide's electronics business sold €2,465 million in 2025, 9.1 percent of group revenue⁹. SK Specialty has made nitrogen trifluoride since 2001, when it became the first company to produce the gas in South Korea³³. The Japanese firm Kanto Denka Kogyo refines its own fluorine gas and turns it into specialty gases for deposition, etching and cleaning³⁴. Stella Chemifa, also Japanese, makes ultra-high-purity hydrofluoric acid for chipmaking³⁵. Another Japanese firm, Morita Chemical Industries, sells an electronic-grade hydrofluoric acid³⁶.

A few firms held most of the markets for wet chemicals and polishing slurries in 2019. CSET's January 2021 brief, drawing on a 2019 report by the market research firm Mordor Intelligence, put five firms, KMG Chemicals, BASF, Avantor, Honeywell and Kanto Chemical, at more than 60 percent of the wet chemicals market³². Citing a 2019

9 Air Liquide, electronics page. Air Liquide, accessed 9 September 2026. airliquide.com

11 Global Semiconductor Materials Market Revenue Reaches Record \$73.2 Billion in... PR Newswire, 12 May 2026. prnewswire.com

12 Materials Market Data Subscription (MMDS). SEMI, accessed 20 October 2026. semi.org

13 Announcement Regarding Result of Tender Offer for JSR Corporation (Securities... Japan Investment Corporation, 17 April 2024. jiccapiital.co.jp

14 Consolidated Financial Results for the Second Quarter (Interim) of the Fiscal... Tokyo Ohka Kogyo, 6 August 2026, p. 4. tok.co.jp

17 湖北鼎龙控股股份有限公司2025年年度报告摘要. CNINFO, 27 March 2026, p. 2. static.cninfo.com.cn

28 湖北鼎龙控股股份有限公司2025年年度报告摘要. CNINFO, 27 March 2026, p. 8. static.cninfo.com.cn

29 Announcement of Delisting of Shares of JSR Corporation. JSR Corporation, 24 June 2024. jsr.co.jp

30 Fujifilm to Enhance its Production Capacity of Advanced Semiconductor Material... Fujifilm, 5 December 2024. fujifilm.com

31 Fujifilm Launches EUV Resist and EUV Developer. Fujifilm, 29 October 2024. fujifilm.com

32 The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 60. cset.georgetown.edu

33 SK specialty, company website. SK specialty, accessed 18 October 2026. skspecialty.com

34 Specialty Gases. Kanto Denka Kogyo, accessed 18 October 2026. kantodenka.co.jp

35 High-purity Chemical Business. Stella Chemifa, accessed 18 October 2026. stella-chemifa.co.jp

36 Electronic grade Hydrofluoric acid. Morita Chemical Industries, accessed 18 October 2026. morita-kagaku.co.jp

report by the market research firm Market Reports World, it put DuPont and Cabot Microelectronics at about 56 percent of a \$790 million market for polishing slurries²⁵. Counting by company nationality, the same Fuji Keizai survey, as published by METI, puts Japanese companies at 51 percent of polishing-slurry sales and 59 percent of high-purity cleaning-liquid sales in 2023⁴. Both shares were 49 percent in 2021⁴.

The slurry businesses of both leaders CSET named have since moved to other companies. Cabot Microelectronics renamed itself CMC Materials in October 2020³⁷. The American firm Entegris completed its purchase of CMC Materials on 6 July 2022¹⁵. DuPont separated its electronics business into an independent company, Qnity Electronics, on 1 November 2025³⁸. Qnity sells polishing slurries and pads³⁹.

In sputtering targets for semiconductors, JX Advanced Metals puts its own share of the world market at about 65 percent as of fiscal 2026¹⁶.

04

Supply risks for chip chemicals, gases and metals

Supply at this stage has been disrupted three times since 2019, twice by governments and once by a war.

In July 2019 Japan put photoresist, hydrogen fluoride and fluorinated polyimide under individual export licenses for South Korea, so each export contract needed its own license⁵. South Korea's chip industry depended heavily on Japan for all three chemicals, and Japanese firms supplied more than 90 percent of South Korea's imports of two of them⁵. Japan's hydrogen fluoride exports to South Korea then fell 87.9 percent⁵. Japanese photoresist exports to South Korea did not fall, possibly in part because Japan allowed three-year bulk licenses for some resist sales in December 2019⁵.

South Korea bought more hydrogen fluoride from the United States and Taiwan and more photoresist from Belgium⁵. Production of all three chemicals rose inside South Korea⁵. The rise came both from South Korean firms and from Japanese companies' affiliates in South Korea⁵.

Researchers at Japan's Research Institute of Economy, Trade and Industry (RIETI) found that Japanese hydrogen fluoride exports to the United States rose⁵. They say some Japanese supply may have reached South Korea by way of the United States⁵. Japan ended the individual licenses on 23 March 2023, when it put exports of the three chemicals to South Korea under its bulk export license system⁴⁰.

⁴ METI, Semiconductor and digital industry strategy: future direction... Ministry of Economy, Trade and Industry (Japan), 23 December 2025, p. 8. [meti.go.jp](https://www.meti.go.jp)

⁵ The impact of export controls on international trade: evidence from the... Research Institute of Economy, Trade and Industry, 8 May 2023. [rieti.go.jp](https://www.rieti.go.jp)

¹⁵ Entegris, current report on Form 8-K dated 6 July 2022. U.S. Securities and Exchange Commission, 6 July 2022. [sec.gov](https://www.sec.gov)

¹⁶ Quick Guide to JX Advanced Metals. JX Advanced Metals, accessed 9 September 2026. [jx-nmm.com](https://www.jx-nmm.com)

²⁵ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 59. [cset.georgetown.edu](https://www.cset.georgetown.edu)

³⁷ CMC Materials, current report on Form 8-K dated 28 September 2020. U.S. Securities and Exchange Commission, 1 October 2020. [sec.gov](https://www.sec.gov)

³⁸ DuPont Completes Separation of Qnity Electronics. DuPont, 3 November 2025. investors.dupont.com

³⁹ Chemical Mechanical Planarization (CMP) Materials for Semiconductor. Qnity Electronics, accessed 9 September 2026. qnityelectronics.com

⁴⁰ Circular Notice on Partial Amendment to the Circular Notice on the Operation of... Ministry of Economy, Trade and Industry (Japan), 23 March 2023. [web.archive.org](https://www.web.archive.org)

Russia's invasion of Ukraine in 2022 put chipmakers' supply of neon at risk. Before the invasion, Ukraine supplied about 70 percent of the world's neon and 90 percent of the semiconductor-grade neon used by US industry⁴¹. The fighting forced at least two of Ukraine's three major gas producers, Cryoin and Ingas, to shut their operations in Odesa and Mariupol⁴¹. That halted a significant part of the world's exports of neon, krypton and xenon⁴¹. Gas mixtures containing neon fill the lasers used in lithography, but EUV scanners use a tin light source instead⁴². Many chipmakers had added to their gas stockpiles after Russia annexed Crimea in 2014⁴¹. Samsung, SK hynix, Renesas and Rohm reported adequate neon supplies from China⁴¹.

For chipmaking materials, China's export controls cover metals. On 3 July 2023 China announced that exports of gallium and germanium would need licenses from 1 August¹⁸. On 3 December 2024 it said it would in principle grant no licenses to export gallium, germanium, antimony or superhard materials to the United States⁶. On 9 November 2025 it suspended that ban until 27 November 2026⁸. In February 2026 the US Geological Survey put China's share of world production of primary low-purity gallium at 99 percent⁴³.

The White House set out a trade deal with China on 1 November 2025⁴⁴. It said that under the deal China would issue general licenses for exports of gallium, germanium and antimony for the benefit of US end users and their suppliers⁴⁴.

Most gallium used in the United States goes into chips, and both metals are recovered as byproducts of processing other minerals. Of the gallium used in the United States in 2025, 73 percent went into integrated circuits built on gallium arsenide or gallium nitride⁴³. Another 26 percent went into optoelectronic devices such as LEDs and laser diodes⁴³. In the United States, germanium goes mainly into fiber optics, infrared optics, semiconductors and solar cells, and radiation detectors⁷. Gallium is recovered mostly as a byproduct of processing bauxite, the ore that aluminum is made from⁴³. Germanium is recovered from certain zinc smelter residues and from coal ash⁴⁵. Because both metals are economical to produce only as byproducts, their supply may not rise much when their prices do⁴⁵.

In Europe, germanium metal averaged an estimated \$4,100 a kilogram in 2025, against \$1,392 in 2023, on Argus Media prices reported by the US Geological Survey⁷. US imports of the metal fell an estimated 67 percent in 2025 because of China's ban⁷. In October 2024 the US Geological Survey estimated that a total Chinese ban on gallium and germanium exports could cut US GDP by \$3.4 billion⁴⁶.

6 商务部公告2024年第46号 关于加强相关两用物项对美国出口管制的公告. Ministry of Commerce of the People's Republic of China, 3 December 2024. mofcom.gov.cn

7 Mineral Commodity Summaries 2026: Germanium. U.S. Geological Survey, 5 February 2026. pubs.usgs.gov

8 商务部公告2025年第72号 公布调整实施商务部公告2024年第46号的决定. Ministry of Commerce of the People's Republic of China, 9 November 2025. mofcom.gov.cn

18 商务部 海关总署公告2023年第23号 关于对镓、锗相关物项实施出口管制的公告. Ministry of Commerce of the People's Republic of China, 3 July 2023. mofcom.gov.cn

41 Russia's Invasion of Ukraine Impacts Gas Markets Critical to Chip Production. Center for Strategic and International Studies, 14 March 2022. csis.org

42 The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 97. cset.georgetown.edu

43 Mineral Commodity Summaries 2026: Gallium. U.S. Geological Survey, 5 February 2026. pubs.usgs.gov

44 Fact Sheet: President Donald J. Trump Strikes Deal on Economic and Trade... The White House, 1 November 2025. whitehouse.gov

45 Quantifying Potential Effects of China's Gallium and Germanium Export... U.S. Geological Survey, 15 October 2024, p. 11. pubs.usgs.gov

46 Quantifying Potential Effects of China's Gallium and Germanium Export... U.S. Geological Survey, 15 October 2024, p. 9. pubs.usgs.gov

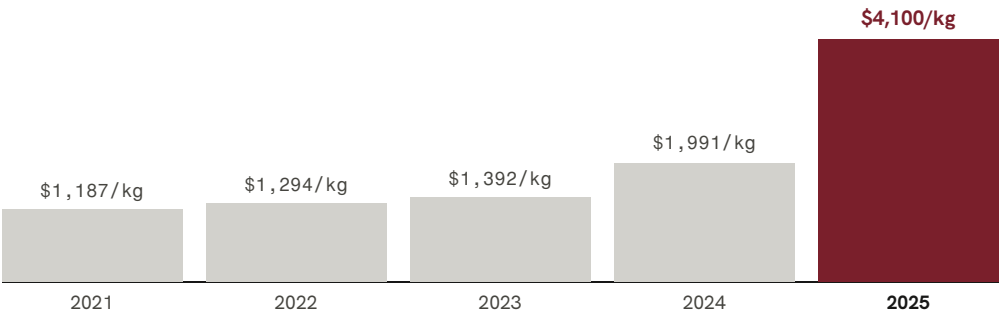
A slower risk is the European Union's proposed restriction on PFAS, the long-lived fluorinated chemicals. These chemicals are used throughout a fab, from some etch gases to seals, filters and the plastic linings of chemical tanks and pipes. Most of the photoacid generators that free the acid in resist contain PFAS too⁴⁷.

Each resist made without PFAS would need full qualification in the chipmaker's fab³. The Semiconductor Industry Association wrote in 2023 that photoresist needs the most rigorous qualification of any chemical a chipmaker uses, because each resist is tuned to the layers it prints¹⁰. The resist maker adjusts its formula over rounds of tests in the fab³. A fab could not qualify all the new resists at once, mainly because testing several together can muddle the yield results³. So some would have to be qualified one after another³.

Figure 03.3

Germanium in Europe rose to an estimated \$4,100 a kilogram in 2025

Germanium metal, annual average price in Europe. China required export licenses from August 2023, banned shipments to the US in December 2024 and suspended the ban from November 2025 to 27 November 2026



Source: USGS Mineral Commodity Summaries, February 2026 (Argus Media European prices, 2025 estimated) [7]

The EU proposal may still let chipmakers keep using PFAS where the risks can be controlled. The national authorities of Denmark, Germany, the Netherlands, Norway and Sweden prepared the proposal and updated it after evaluating more than 5,600 comments⁴⁸. ECHA, the EU chemicals agency, published the updated proposal on 20 August 2025⁴⁸. The updated proposal assessed options that would let electronics and semiconductor makers keep using PFAS where the risks can be controlled⁴⁸.

In March 2026 ECHA's two scientific committees backed an EU-wide restriction with targeted derogations, or exemptions⁴⁹. One committee gave its backing in a final opinion and the other in a draft⁴⁹. Their evaluation is due to finish by the end of 2026⁴⁹. The European Commission will decide in consultation with the member states⁴⁸.

3 PFAS-Containing Photo-Acid Generators Used in Semiconductor Manufacturing. Semiconductor Industry Association, 8 June 2023, p. 22. [semiconductors.org](https://www.semiconductors.org)

7 Mineral Commodity Summaries 2026: Germanium. U.S. Geological Survey, 5 February 2026. pubs.usgs.gov

10 PFAS-Containing Photo-Acid Generators Used in Semiconductor Manufacturing. Semiconductor Industry Association, 8 June 2023, p. 21. [semiconductors.org](https://www.semiconductors.org)

47 PFAS-Containing Photo-Acid Generators Used in Semiconductor Manufacturing. Semiconductor Industry Association, 8 June 2023, p. 4. [semiconductors.org](https://www.semiconductors.org)

48 ECHA publishes updated PFAS restriction proposal. European Chemicals Agency, 20 August 2025. echa.europa.eu

49 ECHA supports PFAS restriction with targeted derogations. European Chemicals Agency, 26 March 2026. echa.europa.eu

Four questions to answer from memory

1. **What does photoresist do?** see How it works
 2. **Why is it slow to switch to a new photoresist?** see How it works
 3. **Which country's companies sell most of the world's photoresist?** see Who makes it
 4. **What happened when Japan limited chemical sales to South Korea in 2019?**
see The chokepoint
-

Four things to remember

- Photoresist holds the pattern printed by light so the next step can etch it into the wafer.
 - Japanese companies held 77 percent of world photoresist sales in 2021 and 78 percent in 2023.
 - A chipmaker has to approve each new resist in its own fab, and even one that passes the first time takes seven to 17 months.
 - China has required licenses to export gallium and germanium since August 2023.
-

Sources (49)

1. A **Testimony of the Semiconductor Industry Association (SIA) before the Senate Committee on Environment & Public Works**. U.S. Senate Committee on Environment and Public Works · 4 March 2026 · p. 6
www.epw.senate.gov/public/_cache/files/a/c/ac4552ff-551b-40d5-bea6-19dd17a1cfea/1F7BCD91016CBE352434701BE58395874BEA6A892A23ABEE1D7214EC924EC0EB.03-04-2026-isaacs-testimony.pdf#page=6
2. A **Sumitomo Chemical to Expand Production Capacity for High-Purity Chemicals for Semiconductors at its Ehime Works and in South Korea**. Sumitomo Chemical · 24 August 2021
www.sumitomo-chem.co.jp/english/news/detail/20210824e_1.html
3. A **PFAS-Containing Photo-Acid Generators Used in Semiconductor Manufacturing**. Semiconductor Industry Association (Semiconductor PFAS Consortium Photolithography Working Group) · 8 June 2023 · p. 22
www.semiconductors.org/wp-content/uploads/2023/06/FINAL-PAG-Case-Study.pdf#page=22
4. A **METI, Semiconductor and digital industry strategy: future direction (半導体・デジタル産業戦略の今後の方向性)**, 23 December 2025. Ministry of Economy, Trade and Industry (Japan) · 23 December 2025 · p. 8
www.meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/0014/handeji14-4.pdf#page=8
5. A **The impact of export controls on international trade: evidence from the Japan-Korea trade dispute in the semiconductor industry**. Research Institute of Economy, Trade and Industry (Japan) · 8 May 2023
www.rieti.go.jp/en/columns/v01_0201.html
6. A **商务部公告2024年第46号 关于加强相关两用物项对美国出口管制的公告**. Ministry of Commerce of the People's Republic of China · 3 December 2024
www.mofcom.gov.cn/zwgk/zcfb/art/2024/art_3d5e990b43424e60828030f58a547b60.html
7. A **Mineral Commodity Summaries 2026: Germanium**. U.S. Geological Survey · 5 February 2026
pubs.usgs.gov/periodicals/mcs2026/mcs2026-germanium.pdf
8. A **商务部公告2025年第72号 公布调整实施商务部公告2024年第46号的决定**. Ministry of Commerce of the People's Republic of China · 9 November 2025
www.mofcom.gov.cn/zwgk/zcfb/art/2025/art_5c68985a6b1a46778e2e8dbff1bb1601.html
9. A **Air Liquide, electronics page**. Air Liquide · Accessed 9 September 2026
www.airliquide.com/group/activities/electronics
10. A **PFAS-Containing Photo-Acid Generators Used in Semiconductor Manufacturing**. Semiconductor Industry Association (Semiconductor PFAS Consortium Photolithography Working Group) · 8 June 2023 · p. 21
www.semiconductors.org/wp-content/uploads/2023/06/FINAL-PAG-Case-Study.pdf#page=21
11. A **Global Semiconductor Materials Market Revenue Reaches Record \$73.2 Billion in 2025, SEMI Reports**. PR Newswire · 12 May 2026
www.prnewswire.com/news-releases/global-semiconductor-materials-market-revenue-reaches-record-73-2-billion-in-2025--semi-reports-302768700.html
12. A **Materials Market Data Subscription (MMDS)**. SEMI · Accessed 20 October 2026
www.semi.org/en/products-services/market-data/mmids
13. A **Announcement Regarding Result of Tender Offer for JSR Corporation (Securities Code: 4185)**. Japan Investment Corporation · 17 April 2024
www.jicccapital.co.jp/en/news/assets/E_20240417_JIC_JICC_PressRelease.pdf

14. A **Consolidated Financial Results for the Second Quarter (Interim) of the Fiscal Year Ending December 31, 2026 [J-GAAP]**. Tokyo Ohka Kogyo · 6 August 2026 · p. 4
www.tok.co.jp/application/files/7417/8598/0069/q2_2612_en.pdf#page=4
15. A **Entegris, current report on Form 8-K dated 6 July 2022**. U.S. Securities and Exchange Commission (filing by Entegris) · 6 July 2022
www.sec.gov/Archives/edgar/data/1101302/000114036122025275/ny20004647x3_ex99-1.htm
16. A **Quick Guide to JX Advanced Metals**. JX Advanced Metals · Accessed 9 September 2026
www.jx-nmm.com/english/company/glance/
17. A **湖北鼎龙控股股份有限公司2025年年度报告摘要**. CNINFO · 27 March 2026 · p. 2
static.cninfo.com.cn/finalpage/2026-03-27/1225036148.PDF#page=2
18. A **商务部 海关总署公告2023年第23号 关于对镓、锗相关物项实施出口管制的公告**. Ministry of Commerce of the People's Republic of China · 3 July 2023
www.mofcom.gov.cn/zcfb/dwmygl/art/2023/art_52b9a321087f402bb3d310d18b07967e.html
19. A **JSR Agrees to Acquire EUV Pioneer Inpria Corporation**. JSR Corporation · 17 September 2021
www.jsr.co.jp/jsr_e/news/2021/20210917.html
20. A **PFAS-Containing Photo-Acid Generators Used in Semiconductor Manufacturing**. Semiconductor Industry Association (Semiconductor PFAS Consortium Photolithography Working Group) · 8 June 2023 · p. 6
www.semiconductors.org/wp-content/uploads/2023/06/FINAL-PAG-Case-Study.pdf#page=6
21. A **How Scientists Are Accelerating the Development of Next-Gen Microelectronics**. Lawrence Berkeley National Laboratory · 21 August 2023
newscenter.lbl.gov/2023/08/21/how-scientists-are-accelerating-next-gen-microelectronics/
22. A **Inpria, company website**. Inpria · Accessed 9 September 2026
www.inpria.com/
23. A **Applied Materials, PVD technology page**. Applied Materials · Accessed 9 September 2026
www.appliedmaterials.com/eu/en/semiconductor/semiconductor-technologies/pvd.html
24. A **SABRE Product Family**. Lam Research · 11 August 2017
www.lamresearch.com/product/sabre/
25. A **The Semiconductor Supply Chain - Issue Brief**. Center for Security and Emerging Technology (CSET) · 21 January 2021 · p. 59
cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf#page=59
26. A **The Semiconductor Supply Chain - Issue Brief**. Center for Security and Emerging Technology (CSET) · 21 January 2021 · p. 56
cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf#page=56
27. A **Qnity Electronics, annual report on Form 10-K for the fiscal year ended 31 December 2025**. U.S. Securities and Exchange Commission (filing by Qnity Electronics) · 26 February 2026
www.sec.gov/Archives/edgar/data/2058873/000205887326000010/q-20251231.htm
28. A **湖北鼎龙控股股份有限公司2025年年度报告摘要**. CNINFO · 27 March 2026 · p. 8
static.cninfo.com.cn/finalpage/2026-03-27/1225036148.PDF#page=8
29. A **Announcement of Delisting of Shares of JSR Corporation**. JSR Corporation · 24 June 2024
www.jsr.co.jp/jsr_e/news/assets/pdf/20240624_01_e.pdf
30. A **Fujifilm to Enhance its Production Capacity of Advanced Semiconductor Material CMP Slurries at the Kumamoto Site**. Fujifilm · 5 December 2024
www.fujifilm.com/jp/en/news/hq/11942
31. A **Fujifilm Launches EUV Resist and EUV Developer**. Fujifilm · 29 October 2024
www.fujifilm.com/jp/en/news/hq/11842
32. A **The Semiconductor Supply Chain - Issue Brief**. Center for Security and Emerging Technology (CSET) · 21 January 2021 · p. 60
cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf#page=60
33. A **SK specialty, company website**. SK specialty · Accessed 18 October 2026
www.skspecialty.com/new/eng/html/main/
34. A **Specialty Gases**. Kanto Denka Kogyo · Accessed 18 October 2026
www.kantodenka.co.jp/english/product/gas/
35. A **High-purity Chemical Business**. Stella Chemifa · Accessed 18 October 2026
www.stella-chemifa.co.jp/english/business/chemical/
36. A **Electronic grade Hydrofluoric acid**. Morita Chemical Industries · Accessed 18 October 2026
www.morita-kagaku.co.jp/en/products/hafce/9/
37. A **CMC Materials, current report on Form 8-K dated 28 September 2020**. U.S. Securities and Exchange Commission (filing by CMC Materials) · 1 October 2020
www.sec.gov/Archives/edgar/data/1102934/000110293420000048/ccmp-20201001xex991.htm
38. A **DuPont Completes Separation of Qnity Electronics**. DuPont · 3 November 2025
www.investors.dupont.com/news-and-media/press-release-details/2025/DuPont-Completes-Separation-of-Qnity-Electronics/default.aspx
39. A **Chemical Mechanical Planarization (CMP) Materials for Semiconductor**. Qnity Electronics · Accessed 9 September 2026
www.qnityelectronics.com/semiconductor-cmp.html
40. A **Circular Notice on Partial Amendment to the Circular Notice on the Operation of the Cabinet Order on Export Trade Control and other circular notices (Review of Export Control to South Korea)**. Ministry of Economy, Trade and Industry (Japan) · 23 March 2023
web.archive.org/web/20250408171837/https://www.meti.go.jp/english/press/2023/0323_001.html

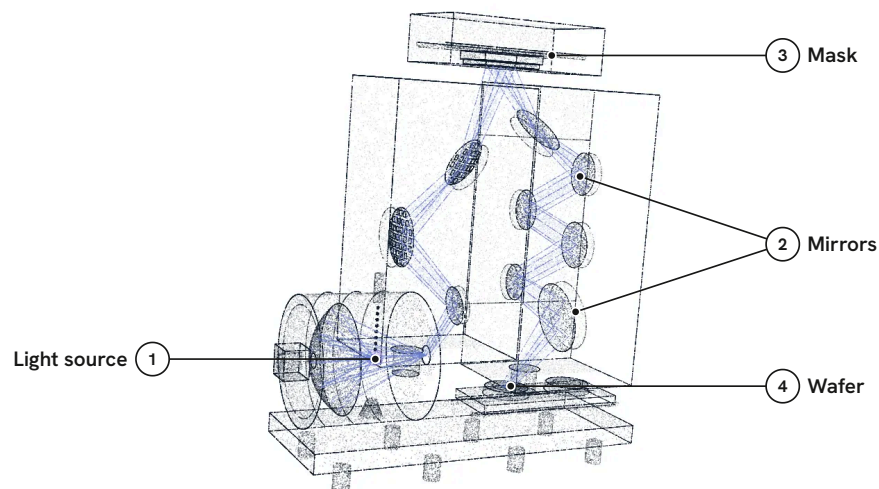
41. A **Russia's Invasion of Ukraine Impacts Gas Markets Critical to Chip Production.** Center for Strategic and International Studies · 14 March 2022
www.csis.org/blogs/perspectives-innovation/russias-invasion-ukraine-impacts-gas-markets-critical-chip-production
42. A **The Semiconductor Supply Chain - Issue Brief.** Center for Security and Emerging Technology (CSET) · 21 January 2021 · p. 97
cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf#page=97
43. A **Mineral Commodity Summaries 2026: Gallium.** U.S. Geological Survey · 5 February 2026
pubs.usgs.gov/periodicals/mcs2026/mcs2026-gallium.pdf
44. A **Fact Sheet: President Donald J. Trump Strikes Deal on Economic and Trade Relations with China.** The White House · 1 November 2025
www.whitehouse.gov/fact-sheets/2025/11/fact-sheet-president-donald-j-trump-strikes-deal-on-economic-and-trade-relations-with-china/
45. A **Quantifying Potential Effects of China's Gallium and Germanium Export Restrictions on the U.S. Economy (Open-File Report 2024-1057).** U.S. Geological Survey · 15 October 2024 · p. 11
pubs.usgs.gov/of/2024/1057/ofr20241057.pdf#page=11
46. A **Quantifying Potential Effects of China's Gallium and Germanium Export Restrictions on the U.S. Economy (Open-File Report 2024-1057).** U.S. Geological Survey · 15 October 2024 · p. 9
pubs.usgs.gov/of/2024/1057/ofr20241057.pdf#page=9
47. A **PFAS-Containing Photo-Acid Generators Used in Semiconductor Manufacturing.** Semiconductor Industry Association (Semiconductor PFAS Consortium Photolithography Working Group) · 8 June 2023 · p. 4
www.semiconductors.org/wp-content/uploads/2023/06/FINAL-PAG-Case-Study.pdf#page=4
48. A **ECHA publishes updated PFAS restriction proposal.** European Chemicals Agency · 20 August 2025
echa.europa.eu/-/echa-publishes-updated-pfas-restriction-proposal
49. A **ECHA supports PFAS restriction with targeted derogations.** European Chemicals Agency · 26 March 2026
echa.europa.eu/-/echa-supports-pfas-restriction-with-targeted-derogations

01	Chip Design, EDA and IP	■■■
02	Silicon and Wafers	■■■
03	Chemicals, Gases and Photoresist	■■■
04	Lithography	■■■
05	Photomasks and Pellicles	■■■
06	Deposition and Etch	■■■
07	Metrology and Inspection	■■■
08	Foundries and Fabs	■■■
09	Memory and HBM	■■■
10	Advanced Packaging	■■■
11	Substrates and PCBs	■■■
12	Test and Assembly	■■■
13	Systems and Networking	■■■
14	Data Centers and Power	■■■
15	The Economics of AI Chips	
16	Who Controls the Chain	



Lithography

ASML, a Dutch firm, is the only maker of extreme ultraviolet scanners, the machines that print the finest layers of a chip. It sold 48 of them in 2025.



Specimen 04 · Lithography

An extreme ultraviolet scanner cut open along its light path. The machine is the size of a bus and weighs about 180 metric tons. The blue-violet thread is the 13.5 nm light. The mask and the wafer are drawn about twice their true size.

Parts, as numbered on the drawing

- ① Light source: ASML San Diego (US), laser by Trumpf (DE)
- ② Mirrors: Zeiss SMT (DE)
- ③ Mask: [see stage 05, Photomasks and Pellicles](#)
- ④ Wafer: [see stage 02, Silicon and Wafers](#)

In plain terms

Lithography prints the pattern of a circuit onto the wafer. A machine holds a stencil of one layer of the circuit up to a light source and projects the image, four times smaller, onto the silicon. The shorter the wavelength of the light, the finer the lines a machine can print. Even so, a machine can print lines narrower than its light's wavelength. Immersion scanners, for example, shine the light through a layer of water between lens and wafer, which lets them print smaller features with the same light¹. ASML rates one of its immersion scanners, the

¹ Lenses & mirrors - Lithography principles. ASML, accessed 9 September 2026. [asml.com](https://www.asml.com)

NXT:2150i, at features of 38 nanometers or less, printed with argon fluoride laser light at 193 nanometers². Air soaks up extreme ultraviolet light, the shortest in use, so machines that print with it work in a vacuum. Only ASML, a Dutch company, makes them. Export controls are government rules on who a company may sell to. Every advanced chip passes through ASML's machines, so export controls on ASML affect all advanced chipmaking.

In short

Beyond extreme ultraviolet (EUV), ASML holds above 80 percent of the market for deep ultraviolet (DUV) lithography, which uses light of longer wavelength³. In July 2026 ASML put its capacity for 2026 at around 65 standard EUV scanners, which caps how many fabs anywhere can add that year⁴. ASML says the production capacity of Zeiss, its sole supplier of optics, limits how many lithography systems it can build⁵.

Export controls set up by the United States with allies including the Netherlands block EUV scanners from Chinese chip foundries⁶. In December 2025 Reuters reported a Chinese prototype that had made EUV light but had printed no chip⁷. In July 2026 Reuters reported, citing one unnamed source, that a Shanghai firm with two state shareholders has started producing immersion DUV tools, which shine their light through water⁸.

ASML sold 327 lithography systems in 2025⁹. Tools shipped to China made up 33 percent of its net system sales that year, more than any other region¹⁰.

Chokepoint card		Lithography	
Concentration		Substitutability	Price or market size
 Extreme Three or fewer firms could supply this stage today, or one firm holds more than half of it.		Very hard ASML is the only maker of EUV scanners, and Zeiss is its sole supplier of their mirrors ⁵ .	About \$200 million for a standard EUV scanner, an estimated \$350 million to \$400 million for the newer High-NA version and roughly \$60 million for a tool in the DUV segment, according to Reuters in July 2026 ³
Who leads	NL ASML	327 lithography systems sold in 2025, including all 48 EUV (extreme ultraviolet) systems ⁹	
	JP Canon	234 chip lithography systems sold in 2025 ¹¹	
	JP Nikon	22 new chip lithography systems sold in the year to March 2026 ¹²	

2 TWINSKAN NXT:2150i. ASML, accessed 18 October 2026. [asml.com](#)

3 Explainer: The \$400 million ASML 'printers' key for the AI chip boom. Reuters, 28 July 2026. [reuters.com](#)

4 Press Release Financial Results Q2 2026. ASML, 15 July 2026. [ourbrand.asml.com](#)

5 ASML Holding, 2025 annual report, filed on Form 6-K. U.S. Securities and Exchange Commission, 25 February 2026. [sec.gov](#)

6 Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements. Center for Strategic and International Studies, 24 September 2025. [csis.org](#)

7 How China built its 'Manhattan Project' to rival the West in AI chips. Reuters, 17 December 2025. [reuters.com](#)

8 China starts production of home-grown immersion DUV chipmaking tools, source... Reuters, 28 July 2026. [reuters.com](#)

9 Financial performance: From ASML's Annual Report 2025. ASML, 24 February 2026, p. 5. [ourbrand.asml.com](#)

10 ASML 2025 fourth-quarter and full-year results (investor presentation). ASML, 28 January 2026, p. 9. [ourbrand.asml.com](#)

11 Canon Inc. FY 2025 Results. Canon, 29 January 2026, p. 22. [global.canon](#)

12 Financial Results: The Year Ended March 31, 2026. Nikon, 8 May 2026, p. 8. [nikon.com](#)

Where it is made	NL	Netherlands	ASML, the Dutch maker of every EUV scanner
	DE	Germany	Zeiss SMT optics, Oberkochen, and Trumpf carbon dioxide drive lasers, Ditzingen
	US	United States	ASML light-source research and manufacturing, San Diego
	JP	Japan	Nikon and Canon lithography scanners and steppers
Why substitution is slow	A newcomer would first have to make mirrors a meter wide, polished smooth to within tens of picometers, a picometer being a trillionth of a meter ¹ . It would also need a light source that hits tin droplets with a laser 50,000 times a second ¹³ .		
Where China stands		Where the US stands	
In July 2026 Reuters reported, citing one unnamed source, that a Shanghai firm with two state shareholders had started producing immersion DUV tools ⁸ . The Center for Technology & Statecraft found in September 2026 that Chinese firms had begun small-batch production of such scanners, but none had yet been shown fit for producing advanced chips ¹⁴ . Its central estimate in 2026 was that China would have a commercially viable immersion scanner for 7 nm chips in the mid-2030s, with the early 2030s plausible, and EUV not before the second half of the 2030s ¹⁴ . Meanwhile Chinese fabs had built a stockpile of more than 330 immersion DUV systems by the first quarter of 2026, most of them ASML's NXT:1980i ¹⁴ .		CSET found in 2021 that no American firm made lithography scanners ¹⁵ . In September 2026 the Center for Technology & Statecraft found that ASML held about 99 percent of the market for immersion DUV scanners and Japan's Nikon the rest ¹⁴ . But every immersion DUV scanner holds a light source from Cymer, a US company now part of ASML, or from Japan's Gigaphoton, so the two governments could stop sales by controlling those parts, the Center for Technology & Statecraft found in September 2026 ¹⁴ . A US rule published in October 2023 already covers immersion scanners with an alignment error between 1.5 nm and 2.4 nm bound for advanced chipmaking if they hold any American-made parts ¹⁶ . The US entity list also requires a license to supply the firms it names ¹⁷ .	

01

How lithography prints a chip's pattern

The stencil is called a photomask, and the machine a scanner (see Photomasks and pellicles).

The wafer is coated with photoresist, a film that changes wherever light touches it. The mask holds one layer of the circuit as a pattern of clear and dark areas, drawn at four times its size on the chip. The machine shines light through the mask, shrinks the image four times with a lens, and lands it on the film.

A wash then removes the film where the light hit, or, with some films, where it did not, leaving the pattern standing on the wafer¹⁸. The film then serves as a stencil for the next step, which either etches the pattern into the layer beneath or fires ions into the open areas to change how the silicon conducts¹⁸. Then the film is stripped and the next mask goes in. Chips are made up of dozens of layers, ASML says¹⁸. Photronics, a US mask maker, says masks are typically sold in sets, with each layer's pattern on a different mask¹⁹.

1 Lenses & mirrors - Lithography principles. ASML, accessed 9 September 2026. [asml.com](#)

8 China starts production of home-grown immersion DUV chipmaking tools, source... Reuters, 28 July 2026. [reuters.com](#)

13 All about light and lasers in lithography. ASML, accessed 9 September 2026. [asml.com](#)

14 DUV Immersion Lithography: The Foundation of the US AI Advantage. Center for Technology & Statecraft, September 2026. [techstatecraft.org](#)

15 The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 4. [cset.georgetown.edu](#)

16 Export Controls on Semiconductor Manufacturing Items. Federal Register, 25 October 2023. [federalregister.gov](#)

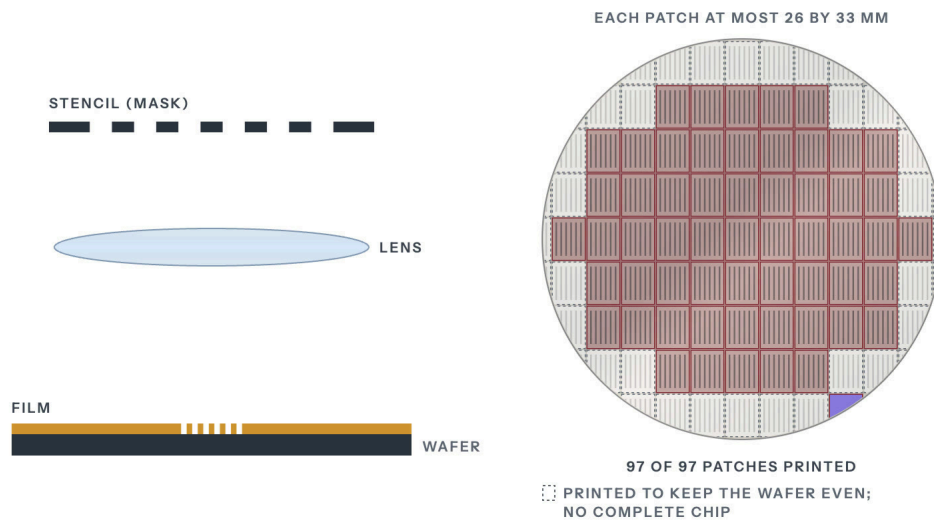
17 Expansion of End-User Controls To Cover Affiliates of Certain Listed Entities. Federal Register, 30 September 2025. [federalregister.gov](#)

18 6 crucial steps in semiconductor manufacturing. ASML, 4 October 2023. [asml.com](#)

19 Photronics, annual report on Form 10-K for the fiscal year ended 31 October 2025. U.S. Securities and Exchange Commission, 17 December 2025. [sec.gov](#)

Figure 04.1 · Explainer, 19 seconds

How lithography prints a chip



1. **Coat.** The wafer is coated with a thin film that changes wherever light touches it.
2. **Stencil.** A stencil, called a mask, holds the pattern for one layer of the chip, drawn four times larger than life.
3. **Shrink.** Light shines through the stencil, and a lens shrinks the image four times and lands it on the film.
4. **Wash.** A wash removes the film wherever the light landed, and the pattern is left on the wafer.
5. **Repeat.** The machine steps across the wafer, printing one patch at a time, each about the size of a postage stamp.

Note: Simplified. The newest machines, which use extreme ultraviolet light, carry the image with mirrors in place of a lens.

The image from one mask covers a patch of up to 26 by 33 mm²⁰. The wafer moves under the optics one patch at a time, close to a hundred patches per wafer. ASML's own wafers-per-hour rating for an EUV scanner assumes 96 of them²⁰. Before the wafer is exposed, the machine measures alignment marks printed in earlier layers so the new layer lines up with them²⁰. For its NXE:3400B EUV scanner, ASML rates the matched-machine overlay, a measure of that alignment, at 2 nm²⁰. That model first shipped in 2017²¹.

Finer lines need shorter light. Glass and air both absorb the shortest light in use, at 13.5 nm²². So an EUV scanner works in a vacuum and uses mirrors instead of lenses, and its masks are mirrors too²². Deep ultraviolet (DUV) machines use light with a wavelength more than fourteen times longer¹³. ASML calls its immersion DUV scanners the workhorses of the industry, used in high-volume manufacturing of the most advanced logic and memory chips²³.

¹³ All about light and lasers in lithography. ASML, accessed 9 September 2026. [asml.com](https://www.asml.com)

²⁰ TWINSCAN NXE:3400B: EUV lithography systems. ASML, accessed 27 September 2026. [asml.com](https://www.asml.com)

²¹ Stronger than expected demand drives ASML Q1 sales. U.S. Securities and Exchange Commission, 19 April 2017. [sec.gov](https://www.sec.gov)

²² ASML EUV lithography systems. ASML, accessed 9 September 2026. [asml.com](https://www.asml.com)

²³ See ASML's DUV lithography systems. ASML, accessed 9 September 2026. [asml.com](https://www.asml.com)

When one exposure cannot draw a pattern finely enough, chipmakers use multipatterning. In the litho-etch kind, the pattern is split between two or more masks printed in turn²⁴. Each added mask brings more process steps, more cost and a risk that the parts of the pattern misalign²⁵. Self-aligned double and quadruple patterning (SADP and SAQP) print the lines with one exposure and then multiply them with deposition and etch steps²⁴. In SAQP each printed line ends up as four²⁴. Because one exposure places all those lines, they cannot misalign with each other²⁴. A later exposure still prints blocks that break them where the circuit needs gaps²⁴. ASML says one EUV exposure per layer cuts masks and process steps and lowers cost²⁶.

Figure 04.2 · Explainer, 26 seconds

How several passes turn one line into four



1. **Print.** A deep ultraviolet scanner shines light through a mask and prints a row of lines, called cores, in one exposure. The chip needs lines four times as dense, closer than one exposure can draw.
2. **Coat.** A thin film is deposited over everything, covering the top and both sides of every core.
3. **Etch back.** An etch straight down clears the film from the tops and the floor and leaves it on the sides of each core. These strips are the spacers, and the edges of the cores set where they stand.
4. **Two lines.** An etch removes the cores and leaves the spacers standing, two for each printed line. All of them trace back to one exposure, so they cannot misalign with each other.
5. **Four lines.** The spacers now serve as cores. The same deposition and etch steps give each of them spacers of its own, so every printed line ends up as four, at a quarter of the spacing.
6. **Cut.** A later exposure prints blocks that break the lines where the circuit needs gaps. ASML says one EUV exposure per layer cuts masks and process steps and lowers cost.

²⁴ EUV lithography: weighing the options. Imec, 6 June 2019. imec-int.com

25 **Applied Materials' Innovative Pattern-Shaping Technology Reduces the Cost...** Applied Materials, 28 February 2023. [ir.appliedmaterials.com](https://www.appliedmaterials.com)

26 Strategic report: From ASML's Annual Report 2025. ASML, 24 February 2026, p. 16. ourbrand.asml.com

Note: Simplified. Drawn in cross-section, as if the wafer were cut across the lines. The deep ultraviolet mask is drawn at the size of the pattern it prints.

02

DUV and EUV scanners compared

Deep ultraviolet

Deep ultraviolet (DUV) light comes from gas lasers called excimer lasers: 248 nanometers from krypton fluoride (KrF), 193 from argon fluoride (ArF), shone through air or water¹³. Cymer, an independently run ASML business in San Diego, makes these excimer lasers, which generate the light that scanners use to print patterns on wafers²⁷. Gigaphoton, a Komatsu company in Japan, also makes excimer lasers for lithography tools²⁸.

Of the systems ASML sold in 2025, 131 were ArF immersion, 78 KrF and 16 ArF dry, all deep ultraviolet, and another 54 were older i-line tools¹⁰. The i-line tools use 365 nm light from a mercury lamp, and ASML says they print features as small as 220 nm¹³.

Reuters gives one price for the whole DUV segment, with tools costing roughly \$60 million each³. ASML's own figures split its DUV sales by tool type. In 2025 the 131 ArF immersion tools it sold made up 42 percent of its system sales, and the 78 KrF tools only 4 percent¹⁰. In DUV, ASML competes with Nikon and Canon, and it still holds above 80 percent of that market³.

Chipmakers without EUV build their finest layers on immersion DUV scanners, in several passes per layer (figure 04.2)²⁶. From 1 September 2023, Dutch export licensing covered the most advanced of these scanners, ASML's NXT:2000i and later models²⁹.

Extreme ultraviolet

The 13.5 nm light comes from molten tin droplets shot from a generator¹³. A laser hits each droplet twice, first with a low-intensity pulse that flattens it and then with a more powerful one that vaporizes it into plasma¹³. The process repeats 50,000 times a second¹³. Mirrors made by Zeiss, a German optics company, carry the light to the wafer¹. The largest are a meter across and smooth to within tens of picometers, a picometer being a thousandth of a nanometer¹.

Brighter light means more wafers an hour, and ASML demonstrated the first 1,000-watt EUV source in April 2025³⁰. Its TWINSCAN NXE:3800E ships at its full 220 wafers an hour, 37 percent more than the NXE:3600D³¹.

¹ Lenses & mirrors - Lithography principles. ASML, accessed 9 September 2026. [asml.com](https://www.asml.com)

³ Explainer: The \$400 million ASML 'printers' key for the AI chip boom. Reuters, 28 July 2026. [reuters.com](https://www.reuters.com)

¹⁰ ASML 2025 fourth-quarter and full-year results (investor presentation). ASML, 28 January 2026, p. 9. [ourbrand.asml.com](https://www.ourbrand.asml.com)

¹³ All about light and lasers in lithography. ASML, accessed 9 September 2026. [asml.com](https://www.asml.com)

²⁶ Strategic report: From ASML's Annual Report 2025. ASML, 24 February 2026, p. 16. [ourbrand.asml.com](https://www.ourbrand.asml.com)

²⁷ Explore ASML San Diego. ASML, accessed 9 September 2026. [asml.com](https://www.asml.com)

²⁸ Gigaphoton, company profile. Gigaphoton, accessed 9 September 2026. [gigaphoton.com](https://www.gigaphoton.com)

²⁹ Statement regarding export control regulations Dutch government. ASML, 30 June 2023. [asml.com](https://www.asml.com)

³⁰ Strategic report: From ASML's Annual Report 2025. ASML, 24 February 2026, p. 30. [ourbrand.asml.com](https://www.ourbrand.asml.com)

³¹ Strategic report: From ASML's Annual Report 2025. ASML, 24 February 2026, p. 17. [ourbrand.asml.com](https://www.ourbrand.asml.com)

High-NA EUV

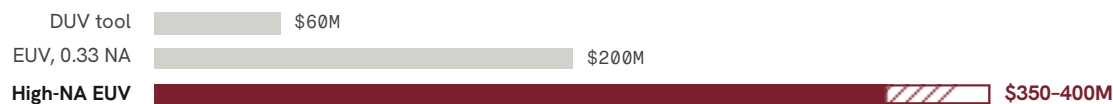
High-NA scanners raise the numerical aperture (NA), a measure of how well the optics collect and focus light, from 0.33 to 0.55³². That cuts the smallest printable feature from 13 nm to 8 nm³². Their optics shrink the mask image four times in one direction and eight in the other, halving the patch of wafer one exposure covers and doubling the exposures per wafer³². The second-generation TWINSCAN EXE:5200B runs at 175 wafers an hour, 60 percent above the EXE:5000²⁶.

Reuters puts a standard EUV tool at around \$200 million and a High-NA machine at an estimated \$350 to \$400 million³.

Figure 04.3

High-NA EUV scanners cost an estimated \$350 million to \$400 million in 2026

What one lithography system costs. The DUV bar is one figure for the whole segment



Source: Reuters explainer on ASML's lithography machines, first published 28 January 2026 and updated 28 July 2026 [3]

ASML sold four High-NA (EXE) systems in 2025, against two in 2024³³. In its 2025 annual report, filed in February 2026, ASML said it expected High-NA to start supporting high-volume manufacturing in 2027⁵.

Intel and TSMC have chosen differently on High-NA:

- **Intel Foundry** says it uses High-NA in volume production for select layers of some Intel 18A products³⁴. It installed the first EXE:5200B³⁵. By September 2026 it had run more than one million wafers on High-NA tools, a count that includes tool testing and research as well as volume production³⁴.
- **TSMC** waited, and in September 2026 said it will use High-NA in high-volume manufacturing from 2030³⁶.

On 8 September 2026 ASML and TSMC announced a move from 6-inch photomasks to 12-inch ones, to remove stitching constraints³⁶. Stitching constraints are the design limits that come from printing a large chip in two halves. ASML and TSMC aim for a pilot line for the new masks by 2031 and for High-NA systems that use them to enter production by 2033³⁶.

³ Explainer: The \$400 million ASML 'printers' key for the AI chip boom. Reuters, 28 July 2026. [reuters.com](https://www.reuters.com)

⁵ ASML Holding, 2025 annual report, filed on Form 6-K. U.S. Securities and Exchange Commission, 25 February 2026. [sec.gov](https://www.sec.gov)

²⁶ Strategic report: From ASML's Annual Report 2025. ASML, 24 February 2026, p. 16. [ourbrand.asml.com](https://www.asml.com)

³² 5 things you should know about High NA in EUV. ASML, 25 January 2024. [asml.com](https://www.asml.com)

³³ Financial performance: From ASML's Annual Report 2025. ASML, 24 February 2026, p. 7. [ourbrand.asml.com](https://www.asml.com)

³⁴ Intel Foundry and ASML Accelerate Industry Readiness for High-NA EUV. Intel, 7 September 2026. [intel.com](https://www.intel.com)

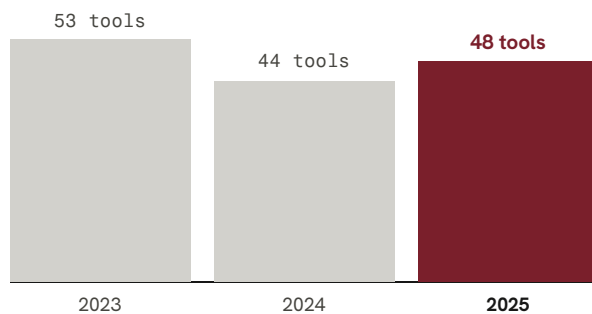
³⁵ High NA EUV reaches new readiness milestone with first high-volume Logic product. ASML, 15 July 2026. [asml.com](https://www.asml.com)

³⁶ ASML and TSMC Announce Initiative to Pioneer Industry Transition to... TSMC, 8 September 2026. [pr.tsmc.com](https://www.tsmc.com)

Figure 04.4

ASML sold 48 EUV systems in 2025, up from 44 in 2024

EUV systems ASML sold each year



Source: ASML 2025 annual report for 2024 and 2025, and ASML's Q4 2023 investor presentation for 2023 [9]

03

Who makes lithography machines

ASML's net sales were EUR 32.7 billion in 2025, at a 52.8 percent gross margin⁹. In October 2026 it expected 2026 net sales of EUR 44 to 45 billion, at a gross margin of around 56 percent³⁷. Its 2025 annual report lists 5,100 suppliers⁵. Three of them and ASML's own San Diego site make the main parts of the EUV machine:

- **Zeiss SMT**, Oberkochen, Germany, makes the illumination system and the six-mirror projection optics³⁸.
- **Trumpf**, Ditzingen, Germany, makes the carbon dioxide drive laser that hits the tin droplets³⁹. It amplifies a few watts to 40 kilowatts³⁹.
- **ASML San Diego**, which includes the light-source maker Cymer that ASML bought in 2013, designs the source where the laser turns tin into plasma, and builds the droplet generator²⁷.
- **VDL ETG** builds the frames that suspend and position the mirrors⁴⁰.

ASML says the production capacity of Zeiss, its sole supplier of optics, limits how many lithography systems it can build⁵.

Lithography is the stage of the chain that European firms lead, with ASML the only maker of EUV scanners²⁶. The bulk of ASML's suppliers are in the Netherlands and the rest of Europe, the Middle East and Africa, the company says⁴¹.

⁵ ASML Holding, 2025 annual report, filed on Form 6-K. U.S. Securities and Exchange Commission, 25 February 2026. [sec.gov](#)

⁹ Financial performance: From ASML's Annual Report 2025. ASML, 24 February 2026, p. 5. [ourbrand.asml.com](#)

²⁶ Strategic report: From ASML's Annual Report 2025. ASML, 24 February 2026, p. 16. [ourbrand.asml.com](#)

²⁷ Explore ASML San Diego. ASML, accessed 9 September 2026. [asml.com](#)

³⁷ ASML reports €11.7 billion total net sales and €5.0 billion net income in Q3... U.S. Securities and Exchange Commission, 14 October 2026. [sec.gov](#)

³⁸ EUV lithography and technology. Carl Zeiss, accessed 9 September 2026. [zeiss.com](#)

³⁹ Good things come in ever-smaller packages. TRUMPF, accessed 9 September 2026. [trumpf.com](#)

⁴⁰ VDL ETG builds complex frames for Zeiss. VDL Groep, 22 March 2019. [web.archive.org](#)

⁴¹ Sourcing & Supply Chain. ASML, accessed 27 October 2026. [asml.com](#)

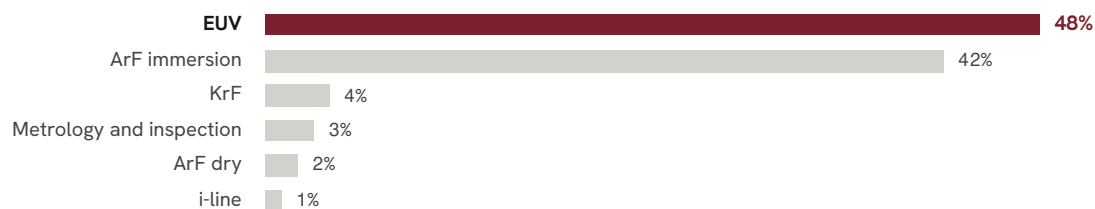
In Japan, Nikon and Canon also make lithography tools. Nikon sold 22 new chip lithography systems in the year to March 2026, in a market it sizes at 570 units for 2025¹². Its Precision Equipment business made an operating loss in the year to March 2026⁴². Canon sold 234 chip lithography systems in 2025, 188 of them i-line and 46 KrF¹¹. Its range runs from KrF scanners to i-line steppers, including some built for advanced packaging⁴³. Canon also makes a nanoimprint system, the FPA-1200NZ2C, which stamps the pattern instead of projecting it and can print lines down to 14 nm wide⁴⁴. Canon delivered one in 2024 to the Texas Institute for Electronics, to be used for research and prototypes⁴⁴.

In January 2021 CSET, a research center at Georgetown University, found that the United States lacked firms in a few key parts of the chip supply chain, above all lithography tools¹⁵.

Figure 04.5

EUV made up 48 percent of ASML's 2025 system sales

ASML net system sales by technology, 2025



Source: ASML Q4 2025 investor presentation [10]

04

Lithography export controls and China's own scanners

Export controls set up by the United States with allies including the Netherlands block ASML from shipping EUV scanners to Chinese foundries⁶. In September 2025 CSIS judged that EUV remained "firmly out of reach" for China despite massive state investment⁶. For DUV scanners and other tools, the restrictions came in this order:

- **Dutch national licensing** of advanced DUV took effect on 1 September 2023⁴⁵.
- **A US rule** published on 25 October 2023 covered immersion scanners that print features of 45 nm or smaller with an alignment error between 1.5 nm and 2.4 nm¹⁶. If such a scanner was bound for advanced chipmaking, the rule put it under US export rules when it held any American content at all¹⁶. The rule did not apply to

⁶ Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements. Center for Strategic and International Studies, 24 September 2025. [csis.org](https://www.csis.org)

¹⁰ ASML 2025 fourth-quarter and full-year results (investor presentation). ASML, 28 January 2026, p. 9. [ourbrand.asml.com](https://www.asml.com)

¹¹ Canon Inc. FY 2025 Results. Canon, 29 January 2026, p. 22. [global.canon](https://www.canon.com)

¹² Financial Results: The Year Ended March 31, 2026. Nikon, 8 May 2026, p. 8. [nikon.com](https://www.nikon.com)

¹⁵ The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 4. [cset.georgetown.edu](https://www.cset.georgetown.edu)

¹⁶ Export Controls on Semiconductor Manufacturing Items. Federal Register, 25 October 2023. [federalregister.gov](https://www.federalregister.gov)

⁴² Financial Results: The Year Ended March 31, 2026. Nikon, 8 May 2026, p. 6. [nikon.com](https://www.nikon.com)

⁴³ Semiconductor Lithography Equipment. Canon, accessed 18 October 2026. [global.canon](https://www.canon.com)

⁴⁴ Canon delivers FPA-1200NZ2C nanoimprint lithography system for semiconductor... Canon, 26 September 2024. [global.canon](https://www.canon.com)

⁴⁵ The Netherlands expands export control measure for advanced semiconductor... Government of the Netherlands, 6 September 2024. [government.nl](https://www.government.nl)

scanners first exported from a country that lists them on its own export control list¹⁶.

- **A partial license revocation** by the Dutch government, disclosed by ASML on 1 January 2024, stopped shipments of NXT:2050i and NXT:2100i immersion scanners to a few Chinese customers⁴⁶.
- **The Netherlands widened its licensing** to more types of deep ultraviolet lithography equipment from 7 September 2024⁴⁵. On 15 January 2025 it announced that from 1 April 2025 the license requirement would also cover a very limited number of further goods, among them specific measuring and inspection equipment⁴⁷.
- **The BIS Affiliates Rule**, issued by the US Bureau of Industry and Security, extended entity-list controls to affiliates owned 50 percent or more by listed entities from 29 September 2025¹⁷. BIS then suspended it until 9 November 2026⁴⁸. Exporting goods covered by US export rules to a firm on the entity list needs a US license¹⁷.
- **The EU added certain Dutch controls** to the EU Control List in November 2025⁵. ASML says this changed nothing for its immersion tools, because they already needed a Dutch license⁵.

China's share of ASML's net system sales fell from 41 percent in 2024 to 33 percent in 2025¹⁰.

On DUV, Reuters reported in July 2026, citing one unnamed source, that Shanghai Aishengna Electronic Technology Group has started producing home-grown immersion DUV tools⁸. The firm was registered in August 2023 with 7 billion yuan of capital and two state shareholders, Shanghai Electric Holding and a Shanghai International Trust subsidiary⁸. It has no website and has taken in teams from SMEE, China's older scanner maker, and the startup Yuliangsheng⁸. SMEE is strongest in i-line, the coarsest kind of lithography tool, and even there holds only four percent of the world market⁶.

The Center for Technology & Statecraft, a research group, found in September 2026 that none of China's home-grown immersion scanners had yet been shown fit for producing advanced chips¹⁴. Its central estimate was a commercially viable Chinese immersion scanner for 7 nm chips in the mid-2030s, and EUV not before the second half of the 2030s¹⁴. Until then Chinese fabs rely on imported tools, and by the first quarter of 2026 they had built a stockpile of more than 330 immersion DUV systems, most of them ASML's NXT:1980i¹⁴.

5 ASML Holding, 2025 annual report, filed on Form 6-K. U.S. Securities and Exchange Commission, 25 February 2026. sec.gov

6 Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements. Center for Strategic and International Studies, 24 September 2025. csis.org

8 China starts production of home-grown immersion DUV chipmaking tools, source... Reuters, 28 July 2026. reuters.com

10 ASML 2025 fourth-quarter and full-year results (investor presentation). ASML, 28 January 2026, p. 9. ourbrand.asml.com

14 DUV Immersion Lithography: The Foundation of the US AI Advantage. Center for Technology & Statecraft, September 2026. techstatecraft.org

16 Export Controls on Semiconductor Manufacturing Items. Federal Register, 25 October 2023. federalregister.gov

17 Expansion of End-User Controls To Cover Affiliates of Certain Listed Entities. Federal Register, 30 September 2025. federalregister.gov

45 The Netherlands expands export control measure for advanced semiconductor... Government of the Netherlands, 6 September 2024. government.nl

46 Statement regarding partial revocation export license. ASML, 1 January 2024. asml.com

47 Klever: export controls on advanced semiconductor manufacturing equipment to be... Government of the Netherlands, 15 January 2025. government.nl

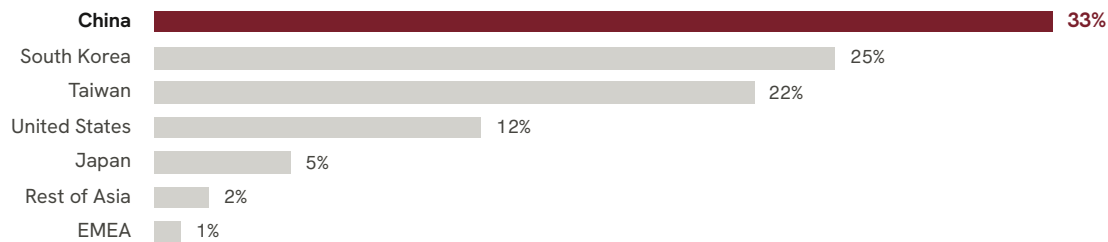
48 One Year Suspension of Expansion of End-User Controls for Affiliates of Certain... Federal Register, 12 November 2025. federalregister.gov

There is less evidence of Chinese progress on EUV. Reuters reported in December 2025 that a Shenzhen team of former ASML engineers had built a prototype that made extreme ultraviolet light but had printed no chip⁷. To print a chip, a machine also needs mirrors that carry that light to the wafer, and ASML's sole supplier of those mirrors is Zeiss⁵.

Figure 04.6

China took 33 percent of ASML's 2025 system sales, the largest share

ASML net system sales by the region tools shipped to, 2025



Source: ASML Q4 2025 investor presentation [10]

Note: Net system sales leave out service and field option sales, which ASML counts in its total net sales. The Export Controls page measures China's share against total net sales.

05

Why ASML's EUV scanners are a chokepoint

No other company makes EUV scanners, so every fab that adds EUV capacity buys it from ASML²⁶. The scanners already in fabs keep printing only as long as they are serviced. ASML has around 10,000 customer support employees who maintain and upgrade those machines around the clock⁴⁹. Serviced this way, ASML's machines stay in use for a long time. In its 2025 annual report ASML said about 95 percent of the systems it had sold in the previous 30 years were still in use⁵. The same report warned that export controls may limit the service ASML can provide for machines already installed⁵⁰.

ASML has a chokepoint of its own. Zeiss SMT is its only supplier of lenses, mirrors and other critical optics⁵¹. ASML says that if Zeiss could not supply them for a long period, ASML would effectively be unable to run its business⁵¹.

ASML's capacity caps how many EUV scanners fabs anywhere can add each year. In July 2026 ASML put its 2026 capacity at around 65 standard (low-NA) EUV scanners and said it plans to add 30 percent for 2027⁴.

Leading-edge AI accelerators are made with EUV, which prints their finest layers, the ones that set how densely transistors and wires pack²². TSMC expects the number of

4 Press Release Financial Results Q2 2026. ASML, 15 July 2026. [ourbrand.asml.com](#)

5 ASML Holding, 2025 annual report, filed on Form 6-K. U.S. Securities and Exchange Commission, 25 February 2026. [sec.gov](#)

7 How China built its 'Manhattan Project' to rival the West in AI chips. Reuters, 17 December 2025. [reuters.com](#)

10 ASML 2025 fourth-quarter and full-year results (investor presentation). ASML, 28 January 2026, p. 9. [ourbrand.asml.com](#)

22 ASML EUV lithography systems. ASML, accessed 9 September 2026. [asml.com](#)

26 Strategic report: From ASML's Annual Report 2025. ASML, 24 February 2026, p. 16. [ourbrand.asml.com](#)

49 Strategic report: From ASML's Annual Report 2025. ASML, 24 February 2026, p. 40. [ourbrand.asml.com](#)

50 Strategic report: From ASML's Annual Report 2025. ASML, 24 February 2026, p. 65. [ourbrand.asml.com](#)

51 Strategic report: From ASML's Annual Report 2025. ASML, 24 February 2026, p. 68. [ourbrand.asml.com](#)

layers needing High-NA to rise, driven mainly by the more complex transistors that AI chips need³⁶.

Four questions to answer from memory

1. What does lithography do? see How it works
 2. Why do chipmakers print the finest layers with extreme ultraviolet (EUV) light?
see How it works
 3. Who makes EUV machines? see Controls and China's answer
 4. What limits how many EUV machines chip factories can add each year?
see The chokepoint
-

Four things to remember

- Lithography prints each layer of a chip's circuit onto the wafer.
 - Extreme-ultraviolet (EUV) light prints the finest layers in fewer steps than deep ultraviolet, but air and glass absorb it, so EUV machines work in a vacuum and use mirrors.
 - ASML of the Netherlands is the only maker of EUV machines, and Zeiss alone supplies their mirrors.
 - Export controls block EUV sales to Chinese chipmakers, and a Chinese prototype reported in December 2025 had printed no chip.
-

Sources (51)

1. A Lenses & mirrors - Lithography principles. ASML · Accessed 9 September 2026
www.asml.com/en/technology/lithography-principles/lenses-and-mirrors
2. A TWINSCAN NXT:2150i. ASML · Accessed 18 October 2026
www.asml.com/en/products/duv-lithography-systems/twincan-nxt-2150i
3. B Explainer: The \$400 million ASML 'printers' key for the AI chip boom. Reuters · 28 July 2026
www.reuters.com/world/asia-pacific/250-million-asml-printer-behind-nvidias-chips-2026-07-28/
4. A Press Release Financial Results Q2 2026. ASML · 15 July 2026
ourbrand.asml.com/asset/c8dbf3fc-4c5e-4406-83f6-27694b138245/Press-Release-Financial-Results-Q2-2026.pdf
5. A ASML Holding, 2025 annual report, filed on Form 6-K. U.S. Securities and Exchange Commission (filing by ASML Holding) · 25 February 2026
www.sec.gov/Archives/edgar/data/937966/000162828026011377/asml-2025xannualxreportx.htm
6. A Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements. Center for Strategic and International Studies · 24 September 2025
www.csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chinese-lithography
7. B How China built its 'Manhattan Project' to rival the West in AI chips. Reuters · 17 December 2025
www.reuters.com/world/china/how-china-built-its-manhattan-project-rival-west-ai-chips-2025-12-17/
8. B China starts production of home-grown immersion DUV chipmaking tools, source says. Reuters · 28 July 2026
www.reuters.com/world/china/china-starts-production-home-grown-immersion-duv-chipmaking-tools-source-2026-07-28/
9. A Financial performance: From ASML's Annual Report 2025. ASML · 24 February 2026 · p. 5
ourbrand.asml.com/m/419103cb23dfeaa4/original/asml-2025-annual-report-financial-performance-section.pdf#page=5
10. A ASML 2025 fourth-quarter and full-year results (investor presentation). ASML · 28 January 2026 · p. 9
ourbrand.asml.com/m/3136300aa4999bc1/original/2026_01_28_Presentation-Investor-Relations-Q4-2025.pdf#page=9
11. A Canon Inc. FY 2025 Results. Canon · 29 January 2026 · p. 22
global.canon/en/ir/conference/pdf/conf2025e.pdf#page=22
12. A Financial Results: The Year Ended March 31, 2026. Nikon · 8 May 2026 · p. 8
www.nikon.com/content/dam/web-assets/nikoncom/company/local/global/en/ir/ir_library/result/pdf/2026/26_all_e.pdf#page=8

36 ASML and TSMC Announce Initiative to Pioneer Industry Transition to... TSMC, 8 September 2026. pr.tsmc.com

13. A **All about light and lasers in lithography.** ASML · Accessed 9 September 2026
www.asml.com/en/technology/lithography-principles/light-and-lasers
14. A **DUV Immersion Lithography: The Foundation of the US AI Advantage.** Center for Technology & Statecraft · September 2026
techstatecraft.org/duv/
15. A **The Semiconductor Supply Chain - Issue Brief.** Center for Security and Emerging Technology (CSET) · 21 January 2021 · p. 4
cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf#page=4
16. A **Export Controls on Semiconductor Manufacturing Items.** Federal Register (Commerce Department; Industry and Security Bureau) · 25 October 2023
www.federalregister.gov/documents/2023/10/25/2023-23049/export-controls-on-semiconductor-manufacturing-items
17. A **Expansion of End-User Controls To Cover Affiliates of Certain Listed Entities.** Federal Register (Commerce Department; Industry and Security Bureau) · 30 September 2025
www.federalregister.gov/documents/2025/09/30/2025-19001/expansion-of-end-user-controls-to-cover-affiliates-of-certain-listed-entities
18. A **6 crucial steps in semiconductor manufacturing.** ASML · 4 October 2023
www.asml.com/en/news/stories/2021/semiconductor-manufacturing-process-steps
19. A **Photronics, annual report on Form 10-K for the fiscal year ended 31 October 2025.** U.S. Securities and Exchange Commission (filing by Photronics) · 17 December 2025
www.sec.gov/Archives/edgar/data/810136/000114036125045801/ef20057458_10k.htm
20. A **TWINSCAN NXE:3400B: EUV lithography systems.** ASML · Accessed 27 September 2026
www.asml.com/en/products/euv-lithography-systems/twinscan-nxe3400b
21. A **Stronger than expected demand drives ASML Q1 sales.** U.S. Securities and Exchange Commission (filing by ASML Holding) · 19 April 2017
www.sec.gov/Archives/edgar/data/937966/000093796617000010/pressreleasequarterlyresul.htm
22. A **ASML EUV lithography systems.** ASML · Accessed 9 September 2026
www.asml.com/en/products/euv-lithography-systems
23. A **See ASML's DUV lithography systems.** ASML · Accessed 9 September 2026
www.asml.com/en/products/duv-lithography-systems
24. A **EUV lithography: weighing the options.** imec · 6 June 2019
www.imec-int.com/en/imec-magazine/imec-magazine-june-2019/euv-lithography-weighing-the-options-for-future-logic-and-memory-applications
25. A **Applied Materials' Innovative Pattern-Shaping Technology Reduces the Cost, Complexity and Environmental Impact of Advanced Chip Manufacturing.** Applied Materials · 28 February 2023
ir.appliedmaterials.com/news-releases/news-release-details/applied-materials-innovative-pattern-shaping-technology-reduces
26. A **Strategic report: From ASML's Annual Report 2025.** ASML · 24 February 2026 · p. 16
ourbrand.asml.com/m/8ab959d4926657b/original/asml-2025-annual-report-strategic-report-section.pdf#page=16
27. A **Explore ASML San Diego.** ASML · Accessed 9 September 2026
www.asml.com/en/company/about-asml/locations/san-diego
28. A **Gigaphoton, company profile.** Gigaphoton · Accessed 9 September 2026
www.gigaphoton.com/company
29. A **Statement regarding export control regulations Dutch government.** ASML · 30 June 2023
www.asml.com/en/news/press-releases/2023/statement-regarding-export-control-regulations-dutch-government
30. A **Strategic report: From ASML's Annual Report 2025.** ASML · 24 February 2026 · p. 30
ourbrand.asml.com/m/8ab959d4926657b/original/asml-2025-annual-report-strategic-report-section.pdf#page=30
31. A **Strategic report: From ASML's Annual Report 2025.** ASML · 24 February 2026 · p. 17
ourbrand.asml.com/m/8ab959d4926657b/original/asml-2025-annual-report-strategic-report-section.pdf#page=17
32. A **5 things you should know about High NA in EUV.** ASML · 25 January 2024
www.asml.com/en/company/stories/2024/5-things-high-na-euv
33. A **Financial performance: From ASML's Annual Report 2025.** ASML · 24 February 2026 · p. 7
ourbrand.asml.com/m/419103cb23dfeaa4/original/asml-2025-annual-report-financial-performance-section.pdf#page=7
34. A **Intel Foundry and ASML Accelerate Industry Readiness for High-NA EUV.** Intel · 7 September 2026
www.intel.com/content/www/us/en/newsroom/news/intel-foundry/intel-foundry-asml-accelerate-industry-readiness-for-high-na-euv.html
35. A **High NA EUV reaches new readiness milestone with first high-volume Logic product.** ASML · 15 July 2026
www.asml.com/en/news/press-releases/2026/high-na-euv-reaches-new-readiness-milestone
36. A **ASML and TSMC Announce Initiative to Pioneer Industry Transition to Large-Format Photomasks for High NA EUV.** TSMC · 8 September 2026
pr.tsmc.com/english/news/3338
37. A **ASML reports €11.7 billion total net sales and €5.0 billion net income in Q3 2026.** U.S. Securities and Exchange Commission (filing by ASML Holding) · 14 October 2026
www.sec.gov/Archives/edgar/data/937966/000162828026065813/pressreleasefinancialresul.htm
38. A **EUV lithography and technology.** Carl Zeiss · Accessed 9 September 2026
www.zeiss.com/semiconductor-manufacturing-technology/inspiring-technology/euv-lithography.html
39. A **Good things come in ever-smaller packages.** TRUMPF · Accessed 9 September 2026
www.trumpf.com/en_US/products/lasers/euv-drive-laser/
40. A **VDL ETG builds complex frames for Zeiss.** VDL Groep · 22 March 2019
web.archive.org/web/20240726075938/https://www.vdlgroep.com/en/news/vdl-etg-builds-complex-frames-for-zeiss

41. A **Sourcing & Supply Chain.** ASML · Accessed 27 October 2026
www.asml.com/en/careers/teams/sourcing-and-supply-chain
42. A **Financial Results: The Year Ended March 31, 2026.** Nikon · 8 May 2026 · p. 6
www.nikon.com/content/dam/web-assets/nikoncom/company/local/global/en/ir/ir_library/result/pdf/2026/26_all_e.pdf#page=6
43. A **Semiconductor Lithography Equipment.** Canon · Accessed 18 October 2026
global.canon/en/product/indtech/semicon/
44. A **Canon delivers FPA -1200NZ2C nanoimprint lithography system for semiconductor manufacturing to the Texas Institute for Electronics.** Canon · 26 September 2024
global.canon/en/news/2024/20240926.html
45. A **The Netherlands expands export control measure for advanced semiconductor manufacturing equipment.** Government of the Netherlands · 6 September 2024
www.government.nl/latest/news/2024/09/06/the-netherlands-expands-export-control-measure-advanced-semiconductor-manufacturing-equipment
46. A **Statement regarding partial revocation export license.** ASML · 1 January 2024
www.asml.com/en/news/press-releases/2023/statement-regarding-partial-revocation-export-license
47. A **Klever: export controls on advanced semiconductor manufacturing equipment to be tightened.** Government of the Netherlands · 15 January 2025
www.government.nl/latest/news/2025/01/15/klever-export-controls-on-advanced-semiconductor-manufacturing-equipment-to-be-tightened
48. A **One Year Suspension of Expansion of End-User Controls for Affiliates of Certain Listed Entities.** Federal Register (Commerce Department; Industry and Security Bureau) · 12 November 2025
www.federalregister.gov/documents/2025/11/12/2025-19846/one-year-suspension-of-expansion-of-end-user-controls-for-affiliates-of-certain-listed-entities
49. A **Strategic report: From ASML's Annual Report 2025.** ASML · 24 February 2026 · p. 40
ourbrand.asml.com/m/8ab959d4926657b/original/asml-2025-annual-report-strategic-report-section.pdf#page=40
50. A **Strategic report: From ASML's Annual Report 2025.** ASML · 24 February 2026 · p. 65
ourbrand.asml.com/m/8ab959d4926657b/original/asml-2025-annual-report-strategic-report-section.pdf#page=65
51. A **Strategic report: From ASML's Annual Report 2025.** ASML · 24 February 2026 · p. 68
ourbrand.asml.com/m/8ab959d4926657b/original/asml-2025-annual-report-strategic-report-section.pdf#page=68

01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Photomasks and Pellicles

Only three firms in the world make the blank plates for the masks used to print the finest layers of leading-edge chips. Japan's AGC and Hoya are two of them.

Specimen 05 · Photomasks and Pellicles

An EUV photomask, or reticle, with its pellicle dust cover. The glass plate is drawn to scale. It is a 152 mm square, 6.35 mm thick, about the size of a small floor tile. The dark blue band around the top edge is the mirror coating. The real coating is about forty pairs of layers, each pair 7 nm thick, far thinner than drawn.

In plain terms

A photomask is the stencil that lithography prints from, at least one for each layer of a chip¹. The same mask prints its layer on wafer after wafer, so one mask shapes millions of chips. The most complicated layers are printed with extreme ultraviolet (EUV) light, and the rest can often be printed with deep ultraviolet light². For deep ultraviolet the mask is a quartz plate that the light shines through. No glass lets EUV light through, so the mask for EUV layers is a mirror. The mirror is built up from about forty pairs of thin layers, and the light bounces off it. Japan's AGC and Hoya are two of the three firms that make these mirrors. A dark pattern drawn on top of the mirror soaks up the light wherever no line should print. Any speck of dust on the mask repeats on every wafer it prints. So a thin membrane on a frame, called a pellicle, sits just above the mask and catches dust where it is too far out of focus to print.

In short

On CSET's count from TechInsights data, Austria's IMS Nanofabrication held 46.6 percent of the 2025 world market for electron-beam mask writers, which draw the pattern onto a mask³. Hoya says its share of the mask blank market is exceptionally high⁴.

SemiAnalysis put a full set of masks for a leading-edge chip at \$40 million in May 2026⁵. In July 2022 it wrote that more companies will lack the volume

1 Photronics, annual report on Form 10-K for the fiscal year ended 31 October 2025. U.S. Securities and Exchange Commission, 17 December 2025. sec.gov

2 See ASML's DUV lithography systems. ASML, accessed 9 September 2026. asm1.com

3 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

4 HOYA, Information Technology business, review of operations, Integrated Report... HOYA, accessed 9 September 2026. hoya.com

5 EDA Market Primer. SemiAnalysis, 21 May 2026. newsletter.semianalysis.com

to spread the fixed cost of mask sets⁶. On 8 September 2026 ASML and TSMC announced a plan to move from 6-inch to 12-inch masks⁷. They expect the change to raise fab productivity and lower chipmaking costs⁷.

Each EUV layer of an AI accelerator is printed from a mask built on a blank plate. Only three companies worldwide supply those plates, and Japan's AGC is one of them⁸. Hoya, also Japanese, is another⁴. AGC says it is the only company in the world that takes an EUV blank all the way from the glass to the finished coating⁹.

Checkpoint card		Photomasks and Pellicles	
Concentration		Substitutability	Price or market size
<div><div><div></div><div></div><div></div></div><div>Extreme</div><div>Three or fewer firms could supply this stage today, or one firm holds more than half of it.</div></div>		<div><div>Hard</div><div>AGC said in December 2024 that only three firms supply the blank plates for EUV masks⁸.</div></div>	<div><div>\$40 million</div><div>for a leading-edge mask set, SemiAnalysis's May 2026 figure⁵. In July 2022 it put a 7 nm set above \$10 million⁶</div></div>
Who leads	JP	AGC	Ranks itself No.2 worldwide in EUV mask blanks on its own fiscal 2026 estimates ¹⁰
	JP	Hoya	Said in its 2026 report that its share of mask blanks is exceptionally high ⁴
	JP	Lasertec	Launched the world's first tool that inspects patterned EUV masks at the scanner's own wavelength in 2019 ¹¹
	AT	IMS Nanofabrication	CSET puts its 2025 share of the market for all electron-beam mask writers at 46.6 percent, using TechInsights data ³
	US	Photronics	\$849.3 million of revenue in fiscal 2025 ¹²
Where it is made	JP	Japan	Mask blanks (AGC, Hoya), DUV blanks (Shin-Etsu), inspection (Lasertec), writers (NuFlare), pellicles (Mitsui Chemicals)
	AT	Austria	IMS Nanofabrication multi-beam mask writers
	DE	Germany	Zeiss mask checking in EUV light (AIMS EUV) and mask repair
	US	United States	Photronics merchant mask shops, KLA inspection
	TW	Taiwan	TSMC, which held 10 percent of IMS at the end of 2024
Why substitution is slow	AGC says it spent more than a decade meeting the EUV blank's requirements, such as near-zero thermal expansion, and began mass production only in 2017 ⁸ . Germany's Zeiss calls its AIMS the only system that tests how a mask will print under conditions equivalent to the scanner's ¹³ .		

3 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. [chipexplorer.eto.tech](#)

4 HOYA, Information Technology business, review of operations, Integrated Report... HOYA, accessed 9 September 2026. [hoya.com](#)

5 EDA Market Primer. SemiAnalysis, 21 May 2026. [newsletter.semianalysis.com](#)

6 The Dark Side Of The Semiconductor Design Renaissance – Fixed Costs Soaring Due... SemiAnalysis, 24 July 2022. [newsletter.semianalysis.com](#)

7 ASML and TSMC Announce Initiative to Pioneer Industry Transition to... TSMC, 8 September 2026. [pr.tsmc.com](#)

8 The Japanese glass behind next-generation chips. AGC, 13 December 2024. [agc.com](#)

9 AGC to Boost Production Capacity of EUVL Photomask Blanks. AGC, 27 April 2023. [agc.com](#)

10 AGC Data Book. AGC Inc., 29 May 2026, p. 8. [agc.com](#)

11 Lasertec Releases ACTIS A200HiT Series Actinic EUV Patterned Mask Inspection... Lasertec, 31 October 2025. [lasertec.co.jp](#)

12 Photronics Reports Full Year and Fourth Quarter Fiscal 2025 Results. GlobeNewswire (release by Photronics), 10 December 2025. [globenewswire.com](#)

13 Mask Qualification Solutions by ZEISS SMT. Carl Zeiss, accessed 9 September 2026. [zeiss.com](#)

Where China stands

As of 2026 SMIC runs two mask shops of its own in Shanghai¹⁴. No Chinese firm appears in CSET's 2025 market shares for electron-beam mask writers, the machines that draw the pattern onto a mask³.

Where the US stands

In December 2025 Photronics called itself a leading worldwide maker of photomasks¹². As of 2026 KLA sells tools that inspect EUV masks and optical masks, the quartz masks used with deep ultraviolet light¹⁵.

01

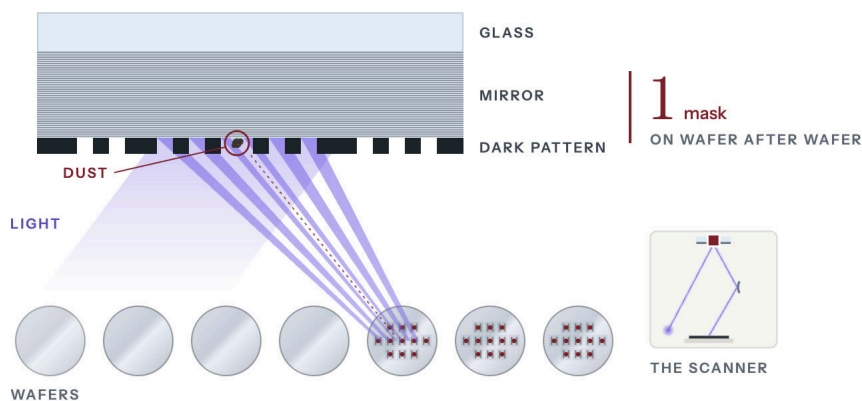
How photomasks are made and used

Figure 05.1 · Explainer, 23 seconds

How a photomask prints its pattern

A speck of dust on the mask

It prints on every wafer that follows



1. **The scanner.** A photomask is the stencil that lithography prints from, at least one for each layer of a chip. Inside the scanner, light bounces off the mask and carries its pattern down to the wafer.
2. **A mirror.** No glass lets extreme ultraviolet (EUV) light through. So the mask for EUV layers is a mirror, built up from about forty pairs of very thin layers laid on glass, and the light bounces off it.
3. **The pattern.** A dark pattern drawn on the mirror soaks up the light wherever no line should print. The light that bounces back carries the pattern of one layer.
4. **Wafer after wafer.** The same mask prints its layer on wafer after wafer, so one plate shapes millions of chips.
5. **One speck.** A speck of dust on the mask prints on every wafer, until someone finds it. So a thin membrane on a frame, called a pellicle, covers the mask's patterned side and catches dust where it is too far out of focus to print.

Note: Simplified. The mask is drawn face down, as it sits in the scanner. The mirror layers and the dark pattern are drawn far thicker than they are, and the light's path through the scanner's mirrors is cut to one bounce.

A mask starts as a blank, a polished plate with no pattern on it yet. For deep ultraviolet the blank is a window of quartz carrying a light-blocking film such as molybdenum

³ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipeexplorer.eto.tech

¹² Photronics Reports Full Year and Fourth Quarter Fiscal 2025 Results. GlobeNewswire (release by Photronics), 10 December 2025. globenewswire.com

¹⁴ Mask Service. SMIC, accessed 9 September 2026. smics.com

¹⁵ Reticle Qualification. KLA Corporation, accessed 20 October 2026. kla.com

silicide¹⁶. Japan's Shin-Etsu is one maker of those blanks¹⁶. For EUV the blank is a mirror of about 40 molybdenum and silicon layer pairs, 7 nm to a pair, laid on glass¹⁷. A dark tantalum film on top, called the absorber, will carry the pattern¹⁸.

The blank is coated with a sensitive film called resist. A mask writer then draws the design into the resist with electrons. A single-beam writer flashes one shape at a time, while NuFlare's multi-beam writer for the most advanced masks controls 260,000 beams at once¹⁹.

A wash removes the drawn resist. An etch then removes the blocking film or absorber wherever the resist is gone, and the rest of the resist is stripped. The plate now passes light, or reflects it, in the shape of one layer of the chip. On standard EUV scanners the pattern is drawn four times larger than it will print²⁰. An inspection tool compares the plate to the design, and a repair tool fixes the stray defects it finds.

EUV masks bring problems of their own:

- **Mask 3D effects.** Light strikes the mirror at a slant, and the absorber has height, so its edges cast small shadows that distort the printed shape. Software has to correct for the shadows in advance.
- **Write precision.** Every edge of the absorber has to sit within a few nanometers of where the design says.
- **Particles.** Anything on the mirror prints on every wafer until someone finds it.

High-NA scanners, the newest EUV machines, print finer lines with larger mirrors. To keep masks at their usual size, the scanners' mirrors shrink the pattern four times in one direction and eight times in the other²⁰. So each exposure covers half the area of a standard exposure, and a wafer takes twice as many exposures²⁰.

On 8 September 2026 ASML and TSMC announced a plan to move from the current 6-inch masks to 12-inch masks⁷. They expect the change to raise fab productivity, lower chipmaking costs and remove stitching constraints, the design limits that come from printing a large chip in two halves⁷. They aim to set up a 12-inch mask pilot line by 2031, so that High-NA scanners using 12-inch masks can enter advanced chip production by 2033⁷.

02

The tools and materials of mask making

Blanks

AGC says it spent more than a decade meeting the blank's requirements, which include near-zero thermal expansion, perfectly smooth and flat surfaces and no particle contamination⁸. It says it began mass production only in 2017⁸.

⁷ ASML and TSMC Announce Initiative to Pioneer Industry Transition to... TSMC, 8 September 2026. pr.tsmc.com

⁸ The Japanese glass behind next-generation chips. AGC, 13 December 2024. agc.com

¹⁶ Photomask blanks. Shin-Etsu Chemical, 3 April 2019. shinetsu.co.jp

¹⁷ The refined EUV mask model. ArXiv, 19 December 2019, p. 2. arxiv.org

¹⁸ The refined EUV mask model. ArXiv, 19 December 2019, p. 1. arxiv.org

¹⁹ EB Mask Writer. NuFlare Technology, accessed 9 September 2026. nuflare.co.jp

²⁰ 5 things you should know about High NA in EUV. ASML, 25 January 2024. asml.com

AGC publishes no market share figure for EUV blanks. In its data book, AGC ranks itself No.2 worldwide in EUV blanks, based on its own fiscal 2026 estimates¹⁰. Hoya says its share of the mask blank market is exceptionally high, and it calls itself the primary supplier for leading-edge EUV nodes⁴. It also says customers may gradually start buying EUV blanks from more than one supplier⁴.

AGC planned to add EUV blank capacity by 2025, and it says its sales reached their target a year early. In April 2023 AGC said its EUV blank capacity would grow by about 30 percent in 2025⁹. The growth would come from a line in Fukushima⁹. METI, Japan's industry ministry, chose the project for a program that supports new plants and equipment in Japan to strengthen supply chains⁹. AGC also said it was aiming for more than ¥40 billion of sales in the business by 2025⁹. Its EUV blank sales grew 50 percent in 2023, AGC said in December 2024⁸. In February 2025 AGC reported that the sales reached ¥40 billion in 2024, which it called a year ahead of its initial target²¹.

AGC plans to add capacity again after a dip in sales. Its EUV blank sales declined in 2025 and were recovering in 2026, AGC said in June 2026²². In August 2026 AGC set out capacity expansions of 20 to 50 percent across EUV blanks, polishing slurry and lens materials for lithography tools²³. It gave no separate figure for the blanks²³. Mass production on the added capacity is to begin in 2028²³.

Writers

An electron-beam writer draws the pattern into the resist on the blank. Multi-beam writers fire many beams at once, and Japan's NuFlare sells them for the 3 nm node¹⁹.

In September 2023 Intel, the majority owner of Austria's IMS Nanofabrication, called it the established industry leader in the multi-beam mask writing tools that advanced EUV requires²⁴. Counting all electron-beam mask writers, CSET, a research center at Georgetown University, put IMS's share of a \$994 million world market at 46.6 percent in 2025, using TechInsights data³. NuFlare had 39.2 percent and JEOL 14.2 percent, in the same CSET analysis of TechInsights data³.

Intel sold a combined 32 percent of IMS in 2023 and still held the other 68 percent on 27 December 2025²⁵. In June 2023 it agreed to sell about 20 percent of IMS to Bain Capital²⁴. Intel agreed in September 2023 to sell roughly 10 percent of IMS to TSMC at a valuation of about \$4.3 billion²⁴. TSMC's subsidiary TSMC Development held that 10 percent at the end of 2024, at a fair value of \$432.8 million in TSMC's accounts²⁶.

3 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

4 HOYA, Information Technology business, review of operations, Integrated Report... HOYA, accessed 9 September 2026. hoya.com

8 The Japanese glass behind next-generation chips. AGC, 13 December 2024. agc.com

9 AGC to Boost Production Capacity of EUVL Photomask Blanks. AGC, 27 April 2023. agc.com

10 AGC Data Book. AGC Inc., 29 May 2026, p. 8. agc.com

19 EB Mask Writer. NuFlare Technology, accessed 9 September 2026. nuflare.co.jp

21 Financial Results for FY2024. AGC Inc., 7 February 2025, p. 45. agc.com

22 Semiconductor-related Business Briefing: Event Summary. AGC Inc., 2 June 2026, p. 17. agc.com

23 AGC Company Overview. AGC Inc., August 2026, p. 52. agc.com

24 Intel to Sell Minority Stake in IMS Nanofabrication Business to TSMC. Intel, 12 September 2023. intc.com

25 Intel, annual report on Form 10-K for the fiscal year ended 27 December 2025. U.S. Securities and Exchange Commission, 23 January 2026. sec.gov

26 TSMC, report on Form 6-K dated 31 December 2024. U.S. Securities and Exchange Commission, 27 February 2025. sec.gov

Inspection and repair

A mask defect cuts the number of good chips on every wafer that mask prints, so masks are checked as blanks, after patterning and again at the fab. Actinic inspection uses 13.5 nm light, the wavelength of EUV lithography¹¹. In 2019 Lasertec launched the ACTIS A150, which it calls the world's first actinic inspection system for patterned EUV masks¹¹. In October 2025 it launched the ACTIS A200HiT series, which it says triples the A150's inspection speed¹¹. Lasertec reported net sales of ¥230,485 million in the year to June 2026²⁷.

As of 2026 KLA's Teron systems for mask shops detect pattern and particle defects on both EUV masks and optical masks, the quartz masks used with deep ultraviolet light¹⁵.

Zeiss makes AIMS EUV, which checks a mask in EUV light under the scanner's own imaging conditions to judge how a defect will affect printing¹³. Zeiss calls AIMS the only system that tests how a mask will print under conditions equivalent to the scanner's¹³. Zeiss says the tool can be extended to ASML's High-NA scanner, the EXE:5000¹³. Zeiss also sells electron-beam repair tools that work on EUV masks²⁸.

Pellicles

A pellicle is a thin membrane on a frame above the mask. Particles land on it, too far out of focus to print, and the pattern below stays clean.

Every photon a pellicle absorbs is light that never reaches the wafer²⁹. The light crosses the pellicle twice, on the way in and on the way back off the mirror, so absorption counts double. In 2022 ASML described its most advanced EUV pellicle as a membrane 13 nanometers thick that can withstand up to 500 degrees Celsius in a high vacuum²⁹. ASML released its first EUV pellicles in 2016 and calls the pellicle one of the breakthroughs that brought EUV lithography to high-volume manufacturing²⁹.

Carbon nanotube membranes are a newer kind of pellicle, aimed at next-generation High-NA, high-output EUV scanners³⁰. In 2020 imec, a Belgian chip research center, mounted them on masks and exposed them in an ASML NXE:3300 scanner³¹. The membranes passed up to 97 percent of the light in a single crossing, and imec found their effect on imaging low and correctable³¹.

Mitsui Chemicals began commercial production of silicon-based EUV pellicles under an ASML license in 2021³⁰. In 2024 it said it would build a carbon nanotube membrane plant at Iwakuni-Ohtake, tentatively due to finish in December 2025³⁰. In December 2025 Mitsui Chemicals said the plant was scheduled for completion in its fiscal 2025, in line with its initial plan³². The same presentation lists the plant under March 2026 in

11 Lasertec Releases ACTIS A200HiT Series Actinic EUV Patterned Mask Inspection... Lasertec, 31 October 2025. lasertec.co.jp

13 Mask Qualification Solutions by ZEISS SMT. Carl Zeiss, accessed 9 September 2026. zeiss.com

15 Reticle Qualification. KLA Corporation, accessed 20 October 2026. kla.com

27 Lasertec, business report. Lasertec, September 2026. lasertec.co.jp

28 Mask Repair Solutions by ZEISS SMT. Carl Zeiss, accessed 9 September 2026. zeiss.com

29 Indistinguishable from magic: the EUV pellicle. ASML, 14 September 2022. asml.com

30 Mitsui Chemicals Sets up Production Facilities for CNT Pellicles to Be Used in... Mitsui Chemicals, 28 May 2024. jp.mitsuichemicals.com

31 Imec demonstrates CNT pellicle utilization on EUV scanner. Imec, 6 October 2020. imec-int.com

32 Business Strategy Presentation (L&HC, Mobility, ICT) in December 2025. Mitsui Chemicals, 17 December 2025, p. 31. jp.mitsuichemicals.com

its table of key investments³³. The membranes are designed to pass 92 percent or more of the light and to withstand exposure power above 1 kW³⁰.

03

Why masks cost more for newer chips

A mask set costs more at each newer node, by SemiAnalysis's figures. In July 2022 SemiAnalysis put mask sets above \$1 million at 28 nm and above \$10 million at 7 nm⁶. It expected 3 nm mask sets to reach the \$40 million range⁶. Its May 2026 primer still puts a leading-edge mask set at \$40 million⁵. The same primer puts a single respin, remaking a chip after a design flaw, at \$50 million to \$100 million at leading-edge nodes⁵.

Mask costs restrict which firms can use a node. SemiAnalysis wrote that at 5 nm and 3 nm, only firms with large wafer volume see the cost per transistor fall⁶. It wrote that more companies will lack the volume to spread the fixed cost of mask sets⁶. It expected failed chip designs to show up first among AI chip startups, which work on much tighter budgets⁶.

Figure 05.2

In 2022 SemiAnalysis forecast a 3 nm mask set at \$40 million

What one photomask set costs, by node, 2022. The 28 nm and 7 nm figures are minimums, and 3 nm was a forecast



Source: SemiAnalysis, The Dark Side of the Semiconductor Design Renaissance, July 2022. SemiAnalysis's May 2026 EDA Market Primer puts a leading-edge mask set at \$40 million [6]

04

Who makes photomasks

Mask making splits between chipmakers that make masks for their own use and independent merchant firms that sell to them and others¹. Photronics says that chipmakers' own shops once supplied most of the market, and that production has more recently tended to move toward the independents¹. TSMC makes masks too, and lists mask making among the services it offers besides making wafers³⁴.

1 Photronics, annual report on Form 10-K for the fiscal year ended 31 October 2025. U.S. Securities and Exchange Commission, 17 December 2025. [sec.gov](#)

5 EDA Market Primer. SemiAnalysis, 21 May 2026. [newsletter.semianalysis.com](#)

6 The Dark Side Of The Semiconductor Design Renaissance – Fixed Costs Soaring Due... SemiAnalysis, 24 July 2022. [newsletter.semianalysis.com](#)

30 Mitsui Chemicals Sets up Production Facilities for CNT Pellicles to Be Used in... Mitsui Chemicals, 28 May 2024. [jp.mitsuichemicals.com](#)

33 Business Strategy Presentation (L&HC, Mobility, ICT) in December 2025. Mitsui Chemicals, 17 December 2025, p. 28. [jp.mitsuichemicals.com](#)

34 TSMC, annual report on Form 20-F for the fiscal year ended 31 December 2025. U.S. Securities and Exchange Commission, 16 April 2026. [sec.gov](#)

Photronics calls itself a leading worldwide maker of masks for chips and flat panel displays¹². It had \$849.3 million of revenue in fiscal 2025, \$615.1 million of it from chip masks¹². The competitors it names in chip and display masks include Dai Nippon Printing, Hoya, Tekscend Photomask and two Chinese firms, Shenzhen Newway Photomask and Shenzhen Qingyi Photomask¹. It also competes with chipmakers' own mask shops¹.

Chinese and foreign firms make masks in China, but no Chinese firm appears in CSET's 2025 market shares for electron-beam mask writers, the machines that draw the pattern onto a mask³. SMIC, a Chinese foundry, runs two in-house mask shops in Shanghai that make masks for deep ultraviolet and older lithography machines¹⁴. Photronics began operating two mask plants in China, in Hefei and Xiamen, in 2019¹. Its chip mask business in Xiamen is a joint venture in which Dai Nippon Printing holds 49.99 percent¹.

05

The few firms behind every EUV mask

Every EUV mask depends on a handful of firms at each step, from the blank plate to the tool that tests how it will print. Only three firms supply the blank plates for EUV masks⁸. IMS Nanofabrication held 46.6 percent of the 2025 market for electron-beam mask writers and NuFlare 39.2 percent, by CSET's count³. In 2019 Lasertec launched what it calls the first tool that inspects patterned EUV masks in EUV light¹¹. Zeiss calls its AIMS the only system that tests how a mask will print under conditions equivalent to the scanner's¹³.

Pellicles already work in high-volume EUV manufacturing²⁹. But ASML says no material is completely transparent to EUV light, so any pellicle in the light's path costs customers productivity²⁹. In 2024 Mitsui Chemicals said it would set up production of carbon nanotube membranes, designed to pass 92 percent or more of the light, for next-generation High-NA, high-output EUV scanners³⁰.

Four questions to answer from memory

1. What is a photomask? see [How it works](#)
2. Why is the mask for an EUV layer a mirror? see [How it works](#)
3. What does a pellicle do? see [How it works](#)
4. Who makes the blank plates for EUV masks? see [The chokepoint](#)

1 Photronics, annual report on Form 10-K for the fiscal year ended 31 October 2025. U.S. Securities and Exchange Commission, 17 December 2025. [sec.gov](#)

3 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. [chipexplorer.eto.tech](#)

8 The Japanese glass behind next-generation chips. AGC, 13 December 2024. [agc.com](#)

11 Lasertec Releases ACTIS A200HiT Series Actinic EUV Patterned Mask Inspection... Lasertec, 31 October 2025. [lasertec.co.jp](#)

12 Photronics Reports Full Year and Fourth Quarter Fiscal 2025 Results. GlobeNewswire (release by Photronics), 10 December 2025. [globenewswire.com](#)

13 Mask Qualification Solutions by ZEISS SMT. Carl Zeiss, accessed 9 September 2026. [zeiss.com](#)

14 Mask Service. SMIC, accessed 9 September 2026. [smics.com](#)

29 Indistinguishable from magic: the EUV pellicle. ASML, 14 September 2022. [asml.com](#)

30 Mitsui Chemicals Sets up Production Facilities for CNT Pellicles to Be Used in... Mitsui Chemicals, 28 May 2024. [jp.mitsuichemicals.com](#)

Four things to remember

- A photomask is the stencil for one layer of a chip, and any flaw on it repeats on every wafer.
 - Three firms make EUV mask blanks, and Lasertec launched the first tool that checks finished masks in EUV light.
 - AGC spent more than a decade learning to make EUV blanks before mass production began in 2017.
 - China makes masks for deep ultraviolet machines and older ones, in SMIC's own mask shops and at independent firms such as Shenzhen Qingyi and Shenzhen Newway.
-

Sources (34)

1. A Photronics, annual report on Form 10-K for the fiscal year ended 31 October 2025. U.S. Securities and Exchange Commission (filing by Photronics) · 17 December 2025
www.sec.gov/Archives/edgar/data/810136/000114036125045801/ef20057458_10k.htm
2. A See ASML's DUV lithography systems. ASML · Accessed 9 September 2026
www.asml.com/en/products/duv-lithography-systems
3. A Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipeexplorer.eto.tech/?parentNode=N25&selectedNode=N29
4. A HOYA, Information Technology business, review of operations, Integrated Report 2026. HOYA · Accessed 9 September 2026
www.hoya.com/ir/2026/en/review/it.html
5. B EDA Market Primer. SemiAnalysis · 21 May 2026
newsletter.semianalysis.com/p/eda-market-primer
6. B The Dark Side Of The Semiconductor Design Renaissance – Fixed Costs Soaring Due To Photomask Sets, Verification, and Validation. SemiAnalysis · 24 July 2022
newsletter.semianalysis.com/p/the-dark-side-of-the-semiconductor
7. A ASML and TSMC Announce Initiative to Pioneer Industry Transition to Large-Format Photomasks for High NA EUV. TSMC · 8 September 2026
pr.tsmc.com/english/news/3338
8. A The Japanese glass behind next-generation chips. AGC · 13 December 2024
www.agc.com/en/hub/pr/the-japanese-glass-behind-next-generation-chips.html
9. A AGC to Boost Production Capacity of EUVL Photomask Blanks. AGC · 27 April 2023
www.agc.com/en/news/detail/1203819_2814.html
10. A AGC Data Book. AGC Inc. · 29 May 2026 · p. 8
www.agc.com/en/ir/library/outline/pdf/reference.pdf#page=8
11. A Lasertec Releases ACTIS A200HiT Series Actinic EUV Patterned Mask Inspection System. Lasertec · 31 October 2025
www.lasertec.co.jp/en/news/2025/20251031_3912.html
12. A Photronics Reports Full Year and Fourth Quarter Fiscal 2025 Results. GlobeNewswire (release by Photronics) · 10 December 2025
www.globenewswire.com/news-release/2025/12/10/3203040/0/en/Photronics-Reports-Full-Year-and-Fourth-Quarter-Fiscal-2025-Results.html
13. A Mask Qualification Solutions by ZEISS SMT. Carl Zeiss · Accessed 9 September 2026
www.zeiss.com/semiconductor-manufacturing-technology/products/photomask-solutions/mask-qualification.html
14. A Mask Service. SMIC · Accessed 9 September 2026
www.smics.com/en/site/mask
15. A Reticle Qualification. KLA Corporation · Accessed 20 October 2026
www.kla.com/products/reticle-manufacturing
16. A Photomask blanks. Shin-Etsu Chemical · 3 April 2019
www.shinetsu.co.jp/en/products/electronics-materials/photomask-blanks/
17. A The refined EUV mask model. arXiv · 19 December 2019 · p. 2
arxiv.org/pdf/1912.09075#page=2
18. A The refined EUV mask model. arXiv · 19 December 2019 · p. 1
arxiv.org/pdf/1912.09075#page=1
19. A EB Mask Writer. NuFlare Technology · Accessed 9 September 2026
www.nuflare.co.jp/english/products/beam/
20. A 5 things you should know about High NA in EUV. ASML · 25 January 2024
www.asml.com/en/company/stories/2024/5-things-high-na-euv

21. A **Financial Results for FY2024.** AGC Inc. · 7 February 2025 · p. 45
www.agc.com/en/ir/library/briefing/pdf/2025_0207e_1.pdf#page=45
22. A **Semiconductor-related Business Briefing: Event Summary.** AGC Inc. · 2 June 2026 · p. 17
www.agc.com/en/ir/library/bizbriefing/pdf/2026_0602esemiconductor_transcript.pdf#page=17
23. A **AGC Company Overview.** AGC Inc. · August 2026 · p. 52
www.agc.com/en/ir/library/outline/pdf/c_overview.pdf#page=52
24. A **Intel to Sell Minority Stake in IMS Nanofabrication Business to TSMC.** Intel · 12 September 2023
www.intc.com/news-events/press-releases/detail/1645/intel-to-sell-minority-stake-in-ims-nanofabrication
25. A **Intel, annual report on Form 10-K for the fiscal year ended 27 December 2025.** U.S. Securities and Exchange Commission (filing by Intel) · 23 January 2026
www.sec.gov/Archives/edgar/data/50863/000005086326000011/intc-20251227.htm
26. A **TSMC, report on Form 6-K dated 31 December 2024.** U.S. Securities and Exchange Commission (filing by TSMC) · 27 February 2025
www.sec.gov/Archives/edgar/data/1046179/000104617925000019/tsmc2024q4consolidatedfina.htm
27. A **Lasertec, business report.** Lasertec · September 2026
www.lasertec.co.jp/en/ir/plan/message.html
28. A **Mask Repair Solutions by ZEISS SMT.** Carl Zeiss · Accessed 9 September 2026
www.zeiss.com/semiconductor-manufacturing-technology/products/photomask-solutions/mask-repair.html
29. A **Indistinguishable from magic: the EUV pellicle.** ASML · 14 September 2022
www.asml.com/en/news/stories/2022/the-euv-pellicle-indistinguishable-from-magic
30. A **Mitsui Chemicals Sets up Production Facilities for CNT Pellicles to Be Used in Next-Gen EUV Lithography.** Mitsui Chemicals · 28 May 2024
jp.mitsuichemicals.com/en/release/2024/2024_0528_1/index.htm
31. A **Imec demonstrates CNT pellicle utilization on EUV scanner.** imec · 6 October 2020
www.imec-int.com/en/press/imec-demonstrates-cnt-pellicle-utilization-euv-scanner
32. A **Business Strategy Presentation (L&HC, Mobility, ICT) in December 2025.** Mitsui Chemicals · 17 December 2025 · p. 31
jp.mitsuichemicals.com/content/dam/mitsuichemicals/sites/mci/documents/release/2025/event_251217e.pdf#page=31
33. A **Business Strategy Presentation (L&HC, Mobility, ICT) in December 2025.** Mitsui Chemicals · 17 December 2025 · p. 28
jp.mitsuichemicals.com/content/dam/mitsuichemicals/sites/mci/documents/release/2025/event_251217e.pdf#page=28
34. A **TSMC, annual report on Form 20-F for the fiscal year ended 31 December 2025.** U.S. Securities and Exchange Commission (filing by TSMC) · 16 April 2026
www.sec.gov/Archives/edgar/data/1046179/000162828026025362/tsm-20251231.htm



01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Deposition and Etch

Deposition and etch tools build a chip layer by layer.

China-based toolmakers' share of deposition tools rose from 2 to 7 percent between 2019 and 2024, by CSET's count.

Specimen 06 · Deposition and Etch

A plasma etch chamber cut in half. The vessel is 500 mm across inside and holds one 300 mm wafer clamped to a holder, called a chuck, at the bottom. The violet haze above the wafer is the plasma. The gap it fills is drawn about twice its real height of 30 to 40 mm. The rest is to scale.

In plain terms

Deposition and etch build the chip itself, one layer at a time. Deposition lays down a thin film, sometimes only a few atoms thick. Lithography prints a pattern on it. Etch then eats away everything the pattern does not protect, and the next film goes down on top. Making one chip takes 1,000 to 1,500 steps, the Semiconductor Industry Association estimated in 2025¹. Some of the holes the etch cuts in memory chips are more than 50 times deeper than they are wide, like a finger-wide shaft about a meter deep². The film has to coat them right to the bottom. The etch has to eat one material and leave the one beside it untouched. Applied Materials and Lam Research in the United States, Tokyo Electron in Japan and ASM International in the Netherlands make most of these machines. Chinese toolmakers have gained share in both kinds of tool since 2019.

In short

American companies held 60.3 percent of the world market for deposition tools in 2025, Japanese companies 14.0 percent and China-based companies 9.8 percent, by CSET's count from TechInsights data³. In etch and cleaning tools that year, American companies held 52.6 percent, Japanese companies 32.6 percent and China-based companies 10.1 percent⁴.

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- 1 Testimony of David Isaacs, Semiconductor Industry Association, hearing on... U.S. Senate Committee on Finance, 14 May 2025, p. 2. finance.senate.gov
 - 2 Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... U.S. Government Publishing Office, 5 December 2024, p. 17. govinfo.gov
 - 3 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech
 - 4 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

Atomic layer deposition tools coat a hole's walls and floor as evenly as its rim⁵. China-based companies held only 2.6 percent of the world market for them in 2025, by CSET's count from TechInsights data⁶. The December 2024 US export rule targets tools for atomic layer deposition of the metals molybdenum and ruthenium, and for coating holes more than 200 times deeper than they are wide⁷.

Applied Materials and Lam Research are the two largest deposition and etch suppliers. Applied Materials' revenue across all its businesses was \$28.368 billion in fiscal 2025⁸. Lam Research's was \$23.233 billion in fiscal 2026, the year to June 2026⁹.

Chokepoint card		Deposition and Etch	
Concentration		Substitutability	Price or market size
 High Four to six firms could supply this stage today, and the top two take most of the revenue.		Moderate In 2025 Lam Research held 41.1 percent of dry etch tools, Tokyo Electron 23.4 percent and Applied Materials 17.4 percent, by CSET's count from TechInsights data ¹⁰ .	\$26.2 billion deposition tool market in 2025, by CSET's count from TechInsights data ³ . Dry etch tools were a \$21.9 billion market in 2025 ¹⁰
Who leads	US	Applied Materials	82.4 percent of physical vapor deposition tools in 2025, by CSET's count from TechInsights data ¹¹
	US	Lam Research	51.2 percent of conductor etch tools in 2025 ¹²
	JP	Tokyo Electron	55.9 percent of dielectric etch tools in 2025 ¹³
	NL	ASM International	54.5 percent of atomic layer deposition tools in 2025 ⁶
	CN	Naura	14.7 percent of physical vapor deposition tools in 2025 ¹¹
Where it is made	US	United States	Applied Materials, Lam Research
	JP	Japan	Tokyo Electron, Kokusai Electric
	NL	Netherlands	ASM International, atomic layer deposition
	KR	South Korea	Large equipment buyer
	CN	China	Naura, AMEC and Piotech, in the largest equipment market (\$49.3 billion in 2025)
Why substitution is possible	Buyers have alternatives ⁵ . At least five firms sell atomic layer deposition tools, which lay down a film a fraction of a layer of atoms at a time ⁶ .		

3 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

5 Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office, 25 October 2023, p. 16. govinfo.gov

6 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

7 Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... U.S. Government Publishing Office, 5 December 2024, p. 33. govinfo.gov

8 Applied Materials, revenue reported to the SEC (XBRL company data). U.S. Securities and Exchange Commission, accessed 9 September 2026. data.sec.gov

9 Lam Research, current report on Form 8-K dated 29 July 2026. U.S. Securities and Exchange Commission, 29 July 2026. sec.gov

10 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

11 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

12 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

13 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

Where China stands

Chinese toolmakers held 12.4 percent of dry etch in 2025, according to CSET's analysis of TechInsights data¹⁰. They held 2.6 percent of atomic layer deposition that year, by the same count⁶.

Where the US stands

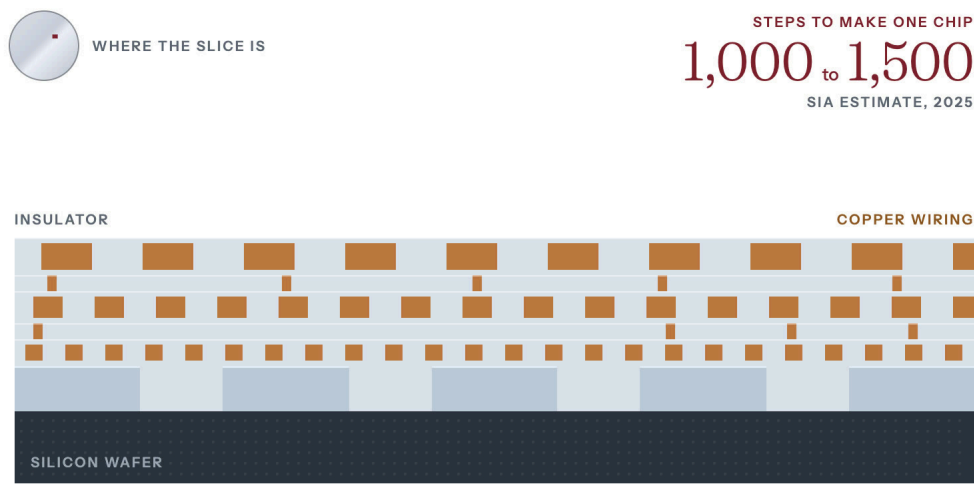
A December 2024 US rule lists some dry etch, atomic layer deposition and deep-hole deposition tools as controlled exports¹⁴. Its foreign direct product rule reaches some tools built outside the United States¹⁵.

01

How deposition and etching work

Figure 06.1 · Explainer, 24 seconds

One round of deposition and etch



1. **The wafer.** A slice through one spot on a wafer, magnified until its layers show.
2. **Deposit.** A thin film is laid over the whole wafer.
3. **Coat.** A light-sensitive coating, the resist, is spun on top.
4. **Expose.** Light shines through a stencil and changes the resist wherever it lands.
5. **Develop.** A wash removes the resist the light reached, leaving the stencil's pattern.
6. **Etch.** A plasma cuts straight down through the film wherever the resist is gone.
7. **Strip.** The leftover resist is removed. The pattern now sits in the film.
8. **Repeat.** Insulator fills the gaps and the next layer goes on. Making one chip takes 1,000 to 1,500 steps, the Semiconductor Industry Association estimated in 2025.

Note: Simplified cross-section. The layers are drawn much thicker than they are.

Most etch steps, and many deposition steps, happen in a vacuum chamber that holds one wafer at a time. A pump empties the chamber of air, and a measured flow of gas comes in. A radio-frequency field, an electric field that reverses millions of times a second, turns the gas into a plasma. The field splits the gas into charged ions and into neutral fragments called radicals, which are more reactive than whole molecules¹⁶.

6 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

10 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

14 Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... U.S. Government Publishing Office, 5 December 2024, p. 32. [govinfo.gov](https://www.govinfo.gov)

15 Commerce Strengthens Export Controls to Restrict China's Capability to Produce... U.S. Bureau of Industry and Security, 2 December 2024. [bis.gov](https://www.bis.gov)

16 Etch Essentials: The Building Blocks of AI Era Microchips (Semi 101). Lam Research, 12 June 2024. newsroom.lamresearch.com

In most deposition steps, the gas carries the material the film will be made of. The molecules, or the radicals a plasma splits from them, land on the wafer and stick. The film builds up a few atoms at a time.

To coat the floor of a deep hole as thickly as its rim, the machine can work in cycles, a method called atomic layer deposition. First one gas settles in a single layer on every surface, and the pump removes the rest. Then a second gas reacts with that layer and nothing else, and the pump empties the chamber again. Each cycle adds a fraction of a layer of atoms wherever the gas reached, so the film grows as evenly on a hole's walls and floor as on its rim⁵.

Not every step runs one wafer at a time. Batch furnaces such as Tokyo Electron's TELINDY PLUS heat as many as 125 wafers at once, usually without plasma¹⁷. They grow oxide films and run low-pressure chemical vapor deposition and some atomic layer deposition¹⁷.

For etch, the gas attacks one material and leaves the one beside it. Wherever the photoresist covers the wafer, it shields the film beneath. Wherever it does not, the radicals react with the surface and turn it into a gas, which the pump carries away. A second field pulls the ions straight down at the wafer, so the etch cuts vertically and a narrow hole keeps its width as it deepens¹⁶. When the etch reaches the material underneath, which the gas was chosen not to touch, it slows almost to a stop, and the tool ends the step.

02

Types of deposition and etching

Deposition families

The market sizes and leading shares below are 2025 figures from Georgetown University's Center for Security and Emerging Technology (CSET), based on data from the research firm TechInsights. CSET puts the deposition tool market at \$26.2 billion³. It puts the dry etch market at \$21.9 billion¹⁰.

- **Physical vapor deposition (PVD)**, which knocks atoms off a solid target and lands them on the wafer, was a \$4.9 billion market in 2025¹¹. Applied Materials held 82.4 percent of it and China's Naura 14.7 percent¹¹.
- **Chemical vapor deposition (CVD)**, which reacts gases at the wafer surface to grow a film, was an \$11.2 billion market in 2025, led by Applied Materials at 47 percent¹⁸.

³ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

⁵ Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office, 25 October 2023, p. 16. govinfo.gov

¹⁰ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

¹¹ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

¹⁶ Etch Essentials: The Building Blocks of AI Era Microchips (Semi 101). Lam Research, 12 June 2024. newsroom.lamresearch.com

¹⁷ TELINDY™ Series. Tokyo Electron, accessed 9 September 2026. tel.com

¹⁸ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

The plasma-enhanced version (PECVD) runs cooler and made up most of it, \$7.5 billion¹⁹.

- **Atomic layer deposition** (ALD) lays down less than one atomic layer at a time. Each step stops once every surface is covered, so it coats vertical walls as evenly as horizontal floors. The US Bureau of Industry and Security (BIS), which writes the export rules, says that even coating makes it important for building 3D structures, such as 3D DRAM, 3D NAND, and the FinFET and gate-all-around transistors in logic chips⁵. ASM International leads it with 54.5 percent of a \$4.1 billion market in 2025⁶.
- **Epitaxy** grows layers that line up with the crystal beneath them, using high-temperature CVD tools²⁰. **Electroplating** deposits the copper used for wiring across the wafer²¹.

Etch families

- **Conductor etch**, which cuts gates, metals and silicon, was a \$12.2 billion market in 2025, led by Lam at 51.2 percent, by CSET's count from TechInsights data¹².
- **Dielectric etch**, which cuts the insulating oxides and nitrides between the conductors, was an \$8.7 billion market in 2025, led by Tokyo Electron at 55.9 percent, by CSET's count from TechInsights data¹³.
- **High-aspect-ratio etch** cuts the deep, narrow channels that let 3D NAND stack layers of memory cells²². A channel's aspect ratio is its depth divided by its width. Lam says slight departures from a channel's intended shape can hurt yield²². Lam runs this etch well below 0 degrees Celsius²². It says its Cryo 3.0 technology can etch channels up to 10 microns deep whose width varies from top to bottom by less than 0.1 percent of their depth²².

AI hardware needs sideways cuts, deeper holes and a second stack of metal wiring on the back of the wafer.

- **Gate-all-around** transistors need highly selective isotropic etch, which cuts sideways²³. BIS controls isotropic dry etch tools that remove silicon-germanium at least 100 times faster than silicon, a selectivity of 100:1 or more²⁴.
- **HBM** (high-bandwidth memory) needs holes etched straight through the silicon, called through-silicon vias (TSVs), so chips can be stacked and wired²⁵. BIS controls the tools that etch these holes at aspect ratios (depth to width) of 10:1 or more and at

5 Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office, 25 October 2023, p. 16. govinfo.gov

6 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

12 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

13 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

19 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

20 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

21 The Semiconductor Supply Chain - Issue Brief. Center for Security and Emerging Technology, 21 January 2021, p. 39. cset.georgetown.edu

22 Lam Research Introduces Lam Cryo™ 3.0 Cryogenic Etch Technology to Accelerate... Lam Research, 31 July 2024. newsroom.lamresearch.com

23 Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office, 25 October 2023, p. 15. govinfo.gov

24 Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office, 25 October 2023, p. 28. govinfo.gov

25 Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... U.S. Government Publishing Office, 5 December 2024, p. 15. govinfo.gov

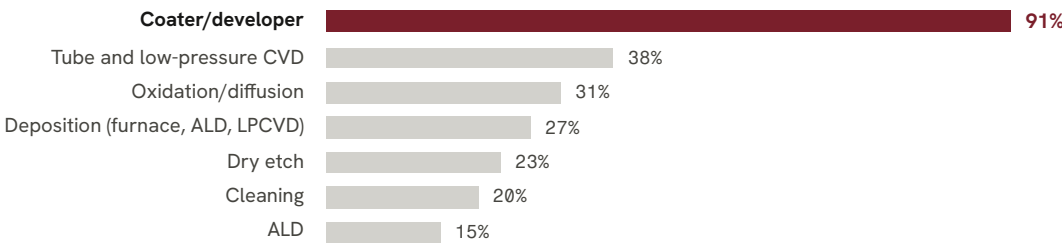
rates above 7 microns a minute¹⁴. The control covers only tools that also keep the holes' depth even to within 2 percent across the wafer¹⁴.

- **Backside power delivery** moves the wires that carry power to the back of the wafer²⁶. In July 2024 Applied Materials said it expected backside power to add \$1 billion to the market for its wiring tools, for every 100,000 wafers a month of new fab capacity²⁷.

Figure 06.2

Tokyo Electron held 91 percent of coater/developers in 2025, on Gartner's figures

Tokyo Electron world market share by tool type, 2025. Some types overlap, because deposition includes furnace, ALD and low-pressure CVD tools



Source: Gartner, as reported in Tokyo Electron's FY2026 Q4 results presentation [28]

03

Who makes deposition and etch tools

The industry association SEMI put world sales of chipmaking equipment at \$135.1 billion in 2025, up 15 percent from \$117.1 billion²⁹. Sales of wafer processing equipment, the category that includes deposition and etch tools, rose 12 percent²⁹.

No one firm dominates deposition and etch the way ASML dominates lithography. In dry etch, CSET's count for 2025 from TechInsights data puts Lam Research at 41.1 percent, Tokyo Electron at 23.4 percent and Applied Materials at 17.4 percent¹⁰. Tokyo Electron's own results presentation, citing Gartner, gives it 23 percent of dry etch and 27 percent of deposition systems in 2025, a category that includes furnace, ALD and low-pressure CVD tools²⁸. Within that category, Tokyo Electron's share of ALD was 15 percent²⁸. The same presentation, again citing Gartner, gives it 91 percent of coater/developers in 2025²⁸. These machines coat wafers with photoresist and develop the pattern after lithography.

ASM International, the atomic layer deposition specialist, reached a record EUR 3.2 billion of revenue in 2025 as customers built 2 nm gate-all-around capacity³⁰.

Molybdenum ALD, a new use of its tools that deposits the metal molybdenum, entered volume production that year³⁰.

10 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

14 Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... U.S. Government Publishing Office, 5 December 2024, p. 32. [govinfo.gov](https://www.govinfo.gov)

26 PowerVia Test Shows Industry-Leading Performance. Intel, 5 June 2023. download.intel.com

27 Applied Materials Unveils Chip Wiring Innovations for More Energy-Efficient... GlobeNewswire (release by Applied Materials), 8 July 2024. globenewswire.com

28 FY2026 (April 2025-March 2026) Financial Announcement, transcript. Tokyo Electron, 30 April 2026, p. 28. tel.com

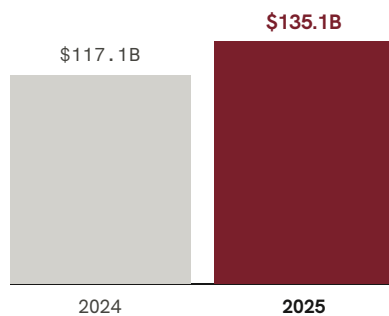
29 SEMI Reports Global Semiconductor Equipment Billings Reached \$135 Billion in... SEMI, 7 April 2026. semi.org

30 ASM reports Q4 and full-year 2025 results. ASM International, 3 March 2026, p. 2. asm.com

Figure 06.3

Chipmaking equipment sales rose to \$135.1 billion in 2025, from \$117.1 billion

What the world spent on chipmaking equipment



Source: SEMI, Worldwide Semiconductor Equipment Market Statistics [29]

04

China's toolmakers and export controls

China is the tool vendors' largest market, buying \$49.3 billion of equipment in 2025, half a percent less than in 2024²⁹. Taiwan's spending rose 90 percent to \$31.5 billion²⁹. South Korea's rose 26 percent to \$25.8 billion²⁹. China still takes a large share of every major vendor's sales.

- **Tokyo Electron:** 34.1 percent of sales in the year to March 2026, down from 41.7 percent³¹. It was 30.4 percent in the quarter to June 2026³².
- **Lam Research:** about 34 percent of revenue in the year to June 2026, the same as a year earlier³³.
- **Applied Materials:** 28 percent in the third fiscal quarter of 2026, down from 35 percent a year earlier³⁴.
- **ASM International:** more than 30 percent of 2025 revenue³⁰.

Between 2019 and 2024, by CSET's analysis of TechInsights data, China-based suppliers went from 2 to 7 percent of deposition and from under 3 to almost 9 percent of etch and clean³⁵. In ALD they gained no share and held less than 1 percent in 2024³⁵.

CSET's newer analysis, of data that TechInsights published in July 2026, puts China-based suppliers at 9.8 percent of deposition in 2025³. They held 10.1 percent of etch and

3 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

29 SEMI Reports Global Semiconductor Equipment Billings Reached \$135 Billion in... SEMI, 7 April 2026. semi.org

30 ASM reports Q4 and full-year 2025 results. ASM International, 3 March 2026, p. 2. asm.com

31 FY2026 (April 2025-March 2026) Financial Announcement, transcript. Tokyo Electron, 30 April 2026, p. 27. tel.com

32 Q1 FY2027 (April-June 2026) Financial Announcement, transcript. Tokyo Electron, 30 July 2026, p. 6. tel.com

33 Lam Research, annual report on Form 10-K for the fiscal year ended 28 June 2026. U.S. Securities and Exchange Commission, 7 August 2026. sec.gov

34 Applied Materials Announces Third Quarter 2026 Results. GlobeNewswire (release by Applied Materials), 13 August 2026. globenewswire.com

35 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology, 14 July 2025. cset.georgetown.edu

clean that year⁴. In dry etch alone their share was 12.4 percent¹⁰. In ALD they held 2.6 percent in 2025, most of it from Piotech⁶.

The Chinese toolmaker AMEC alone held 12.4 percent of dielectric etch in 2025, by CSET's count from TechInsights data¹³. Its revenue was RMB 12.385 billion that year, up about 36.62 percent³⁶. It spent RMB 3.744 billion on research and development, 30.2 percent of sales³⁶.

The United States tightened its export controls at least five times between 2022 and 2025. The rules describe each deposition or etch tool by the process it is designed to run²⁴.

- **October 2022.** BIS issued a rule on 7 October that required a license to export advanced chipmaking equipment to China³⁷. The rule listed that equipment under a new entry, ECCN 3B090³⁷. It also required US persons to get a license to ship, transfer or service items used at advanced fabs in China³⁸. It defined these as fabs that make logic chips with non-planar transistors or at 16/14 nm or below, NAND memory with 128 or more layers, or DRAM at 18 nm half-pitch or below³⁸. The rule extended US license rules to more foreign-made items bound for 28 Chinese entities on the Entity List³⁹. That list names the foreign firms that exporters need a license to supply.
- **October 2023.** A rule issued in October 2023 and effective 17 November rewrote the US control list's entries for chipmaking equipment⁴⁰. It added tools for four processes⁵. The first is dry etch, both sideways (isotropic) and vertical (anisotropic), under ECCN 3B001.c.1²³. The second is spatial ALD (3B001.d.9), whose design keeps stray particles down to the level advanced chips need⁵. The third is low-fluorine tungsten ALD and CVD (3B001.d.10), which fills deep, narrow gaps in advanced chips with tungsten while keeping resistance low⁵. The fourth is carbon hard mask PECVD (3B001.d.5), which lays down the etch-resistant carbon films that smaller features need⁵.
- **December 2024.** BIS controlled 24 more types of equipment and three types of software, and added 140 entities to the Entity List¹⁵. The new equipment entries

4 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

5 Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office, 25 October 2023, p. 16. govinfo.gov

6 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

10 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

13 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

15 Commerce Strengthens Export Controls to Restrict China's Capability to Produce... U.S. Bureau of Industry and Security, 2 December 2024. bis.gov

23 Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office, 25 October 2023, p. 15. govinfo.gov

24 Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office, 25 October 2023, p. 28. govinfo.gov

36 AMEC holds its 2025 annual results briefing (中微公司成功举办2025年度业绩说明会). Advanced Micro-Fabrication Equipment (AMEC), 1 April 2026. amec-inc.com

37 Implementation of Additional Export Controls: Certain Advanced Computing and... U.S. Government Publishing Office, 13 October 2022, p. 7. govinfo.gov

38 Implementation of Additional Export Controls: Certain Advanced Computing and... U.S. Government Publishing Office, 13 October 2022, p. 14. govinfo.gov

39 Implementation of Additional Export Controls: Certain Advanced Computing and... U.S. Government Publishing Office, 13 October 2022, p. 1. govinfo.gov

40 Export Controls on Semiconductor Manufacturing Items. U.S. Government Publishing Office, 25 October 2023, p. 1. govinfo.gov

include TSV etch, and deposition into features with aspect ratios above 200:1⁴¹. BIS also wrote a foreign direct product rule that reaches some tools built outside the United States¹⁵. The rule largely exempts foreign-made tools exported by firms located in Japan, the Netherlands and the 31 other countries it lists, whose governments can control these tools themselves⁴². Japan, one of those countries, had added advanced chipmaking equipment to its own control list on 23 July 2023⁴³.

- **September 2025.** BIS removed the Chinese units of Samsung and SK hynix, and Intel Semiconductor (Dalian), from the Validated End-User program, effective 31 December 2025⁴⁴. From that date, US tools bound for them need a license⁴⁴. BIS estimated that the change would add 1,000 license applications a year⁴⁴.
- **September 2025.** The Affiliates Rule extended Entity List restrictions to any company at least 50 percent owned by a listed entity⁴⁵. BIS then suspended it until 9 November 2026⁴⁶.

BIS enforces the rules on toolmakers too. In February 2026 BIS said Applied Materials had shipped ion implanters, tools that fire atoms into silicon, to a company in China on the Entity List in 2021 and 2022 without the license the Entity List requires⁴⁷. The tools, worth about \$126 million, went to China through Applied's Korean unit⁴⁷. BIS set the penalty at about \$252 million, twice their value and the most the law allows⁴⁷. In fiscal 2026 Applied Materials took a \$253 million charge to settle an export controls compliance matter with BIS³⁴.

Among deposition and etch tool segments, China-based suppliers have their largest share in dry stripping, which clears leftover photoresist off the wafer⁴⁸. Dry stripping was a \$314.6 million market in 2025, by CSET's count from TechInsights data⁴⁸. Japan's Kokusai held 35.7 percent of it, Mattson Technology 22.6 percent and Naura 8.3 percent⁴⁸. Mattson is based in the United States, but Beijing E-Town bought it in 2016³⁵. CSET counts Mattson's share as China's³⁵.

15 Commerce Strengthens Export Controls to Restrict China's Capability to Produce... U.S. Bureau of Industry and Security, 2 December 2024. bis.gov

34 Applied Materials Announces Third Quarter 2026 Results. GlobeNewswire (release by Applied Materials), 13 August 2026. globenewswire.com

35 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology, 14 July 2025. cset.georgetown.edu

41 Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... U.S. Government Publishing Office, 5 December 2024, p. 16. govinfo.gov

42 Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... U.S. Government Publishing Office, 5 December 2024, p. 28. govinfo.gov

43 Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... U.S. Government Publishing Office, 5 December 2024, p. 21. govinfo.gov

44 Revocation of Validated End-User Authorizations in the People's Republic of... U.S. Government Publishing Office, 2 September 2025. govinfo.gov

45 Expansion of End-User Controls To Cover Affiliates of Certain Listed Entities. U.S. Government Publishing Office, 30 September 2025, p. 1. govinfo.gov

46 One Year Suspension of Expansion of End-User Controls for Affiliates of Certain... U.S. Government Publishing Office, 12 November 2025. govinfo.gov

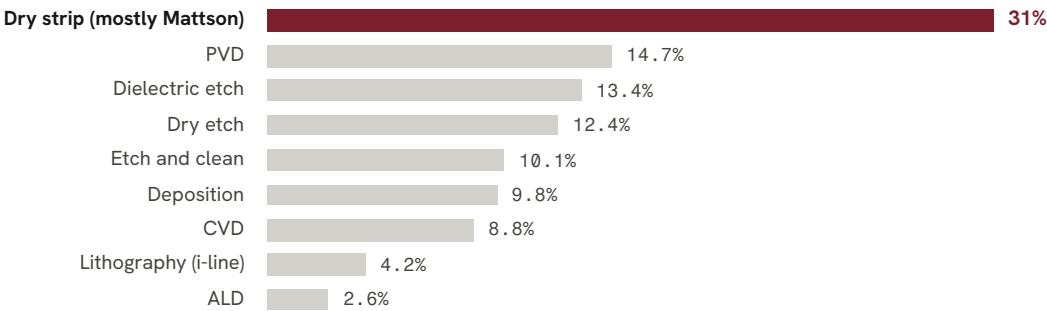
47 Applied Materials to Pay \$252 Million Penalty to BIS for Illegally Exporting... U.S. Bureau of Industry and Security, 11 February 2026. bis.gov

48 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

Figure 06.4

China-based suppliers held 31 percent of dry strip in 2025, mostly Mattson's

China-based suppliers' share of global tool segments, 2025



Source: CSET analysis of TechInsights data (published July 2026), ETO Chip Explorer [3]

05

Why deposition and etch are a weaker chokepoint

Deposition and etch tools are a chokepoint, but a weaker one than lithography, because chipmakers can buy each main tool from more than one maker. In dry etch, Lam Research held 41.1 percent in 2025, Tokyo Electron 23.4 percent and Applied Materials 17.4 percent, by CSET's count¹⁰. Atomic layer deposition has at least five makers⁶.

Four questions to answer from memory

- 1. What do deposition and etch do? see How it works
- 2. What makes deposition and etch hard? see How it works
- 3. Who makes most of these tools? see How it works
- 4. Can a chipmaker switch to another toolmaker here? see Who makes it

Four things to remember

- Deposition lays down thin films and etch cuts them into patterns. Making one chip takes 1,000 to 1,500 steps, by a 2025 industry estimate.
- Four American, Japanese and Dutch firms make most of these tools, and none dominates.
- Chinese makers held 12.4 percent of dry etch and 9.8 percent of deposition in 2025, on CSET's count.
- Chinese makers held 2.6 percent of atomic layer deposition in 2025, most of it from Piotech.

3 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

6 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

10 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

Sources (48)

1. A **Testimony of David Isaacs, Semiconductor Industry Association, hearing on “Trade in Critical Supply Chains”**. U.S. Senate Committee on Finance · 14 May 2025 · p. 2
www.finance.senate.gov/download/051425-isaacs-testimony&download=1#page=2
2. A **Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items**. U.S. Government Publishing Office (Federal Register) · 5 December 2024 · p. 17
www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf#page=17
3. A **Supply Chain Explorer: Advanced Chips**. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N35&selectedNode=N36
4. A **Supply Chain Explorer: Advanced Chips**. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N46&selectedNode=N55
5. A **Export Controls on Semiconductor Manufacturing Items**. U.S. Government Publishing Office (Federal Register) · 25 October 2023 · p. 16
www.govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf#page=16
6. A **Supply Chain Explorer: Advanced Chips**. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N35&selectedNode=N41
7. A **Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items**. U.S. Government Publishing Office (Federal Register) · 5 December 2024 · p. 33
www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf#page=33
8. A **Applied Materials, revenue reported to the SEC (XBRL company data)**. U.S. Securities and Exchange Commission (XBRL data for Applied Materials) · Accessed 9 September 2026
data.sec.gov/api/xbrl/companyconcept/CIK0000006951/us-gaap/RevenueFromContractWithCustomerExcludingAssessedTax.json
9. A **Lam Research, current report on Form 8-K dated 29 July 2026**. U.S. Securities and Exchange Commission (filing by Lam Research) · 29 July 2026
www.sec.gov/Archives/edgar/data/707549/000070754926000033/lrcx_exhibitx991xq4x2026.htm
10. A **Supply Chain Explorer: Advanced Chips**. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N46&selectedNode=N103
11. A **Supply Chain Explorer: Advanced Chips**. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N35&selectedNode=N42
12. A **Supply Chain Explorer: Advanced Chips**. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N46&selectedNode=N50
13. A **Supply Chain Explorer: Advanced Chips**. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N46&selectedNode=N51
14. A **Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items**. U.S. Government Publishing Office (Federal Register) · 5 December 2024 · p. 32
www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf#page=32
15. A **Commerce Strengthens Export Controls to Restrict China's Capability to Produce Advanced Semiconductors for Military Applications**. U.S. Bureau of Industry and Security · 2 December 2024
www.bis.gov/press-release/commerce-strengthens-export-controls-restrict-chinas-capability-produce-advanced-semiconductors-military
16. A **Etch Essentials: The Building Blocks of AI Era Microchips (Semi 101)**. Lam Research · 12 June 2024
newsroom.lamresearch.com/etch-essentials-semiconductor-manufacturing
17. A **TELINDY™ Series**. Tokyo Electron · Accessed 9 September 2026
www.tel.com/product/telindy.html
18. A **Supply Chain Explorer: Advanced Chips**. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N35&selectedNode=N47
19. A **Supply Chain Explorer: Advanced Chips**. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N35&selectedNode=N38
20. A **Supply Chain Explorer: Advanced Chips**. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N35&selectedNode=N40
21. A **The Semiconductor Supply Chain - Issue Brief**. Center for Security and Emerging Technology (CSET) · 21 January 2021 · p. 39
cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief-1.pdf#page=39

22. A **Lam Research Introduces Lam Cryo™ 3.0 Cryogenic Etch Technology to Accelerate Scaling of 3D NAND for the AI Era.** Lam Research · 31 July 2024
newsroom.lamresearch.com/2024-07-31-Lam-Research-Introduces-Lam-Cryo-TM-3-0-Cryogenic-Etch-Technology-to-Accelerate-Scaling-of-3D-NAND-for-the-AI-Era
23. A **Export Controls on Semiconductor Manufacturing Items.** U.S. Government Publishing Office (Federal Register) · 25 October 2023 · p. 15
www.govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf#page=15
24. A **Export Controls on Semiconductor Manufacturing Items.** U.S. Government Publishing Office (Federal Register) · 25 October 2023 · p. 28
www.govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf#page=28
25. A **Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items.** U.S. Government Publishing Office (Federal Register) · 5 December 2024 · p. 15
www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf#page=15
26. A **PowerVia Test Shows Industry-Leading Performance.** Intel · 5 June 2023
download.intel.com/newsroom/archive/2025/en-us-2023-06-05-powervia-test-shows-industry-leading-performance.pdf
27. A **Applied Materials Unveils Chip Wiring Innovations for More Energy-Efficient Computing.** GlobeNewswire (release by Applied Materials) · 8 July 2024
www.globenewswire.com/news-release/2024/07/08/2909540/0/en/applied-materials-unveils-chip-wiring-innovations-for-more-energy-efficient-computing.html
28. A **FY2026 (April 2025-March 2026) Financial Announcement, transcript.** Tokyo Electron · 30 April 2026 · p. 28
www.tel.com/ir/library/report/pjuomj00000000tf-att/fy26q4transcript-e.pdf#page=28
29. A **SEMI Reports Global Semiconductor Equipment Billings Reached \$135 Billion in 2025, Up 15% Year-on-Year.** SEMI · 7 April 2026
www.semi.org/en/SEMI-Reports-Global-Semiconductor-Equipment-Billings-Reached-135-Billion-in-2025
30. A **ASM reports Q4 and full-year 2025 results.** ASM International · 3 March 2026 · p. 2
www.asm.com/media/yvxbavwe/20260303-asm-reports-q4-and-full-year-2025-results.pdf#page=2
31. A **FY2026 (April 2025-March 2026) Financial Announcement, transcript.** Tokyo Electron · 30 April 2026 · p. 27
www.tel.com/ir/library/report/pjuomj00000000tf-att/fy26q4transcript-e.pdf#page=27
32. A **Q1 FY2027 (April-June 2026) Financial Announcement, transcript.** Tokyo Electron · 30 July 2026 · p. 6
www.tel.com/ir/library/report/i242su0000000goz-att/fy27q1transcript-e.pdf#page=6
33. A **Lam Research, annual report on Form 10-K for the fiscal year ended 28 June 2026.** U.S. Securities and Exchange Commission (filing by Lam Research) · 7 August 2026
www.sec.gov/Archives/edgar/data/707549/000070754926000037/lrcx-20260628.htm
34. A **Applied Materials Announces Third Quarter 2026 Results.** GlobeNewswire (release by Applied Materials) · 13 August 2026
www.globenewswire.com/news-release/2026/08/13/3344890/0/en/applied-materials-announces-third-quarter-2026-results.html
35. A **Inside Beijing's Chipmaking Offensive.** Center for Security and Emerging Technology (CSET) · 14 July 2025
cset.georgetown.edu/article/inside-beijings-chipmaking-offensive/
36. A **AMEC holds its 2025 annual results briefing (中微公司成功举办2025年度业绩说明会).** Advanced Micro-Fabrication Equipment (AMEC) · 1 April 2026
www.amec-inc.com/news/708.html
37. A **Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification.** U.S. Government Publishing Office (Federal Register) · 13 October 2022 · p. 7
www.govinfo.gov/content/pkg/FR-2022-10-13/pdf/2022-21658.pdf#page=7
38. A **Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification.** U.S. Government Publishing Office (Federal Register) · 13 October 2022 · p. 14
www.govinfo.gov/content/pkg/FR-2022-10-13/pdf/2022-21658.pdf#page=14
39. A **Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification.** U.S. Government Publishing Office (Federal Register) · 13 October 2022 · p. 1
www.govinfo.gov/content/pkg/FR-2022-10-13/pdf/2022-21658.pdf#page=1
40. A **Export Controls on Semiconductor Manufacturing Items.** U.S. Government Publishing Office (Federal Register) · 25 October 2023 · p. 1
www.govinfo.gov/content/pkg/FR-2023-10-25/pdf/2023-23049.pdf#page=1
41. A **Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items.** U.S. Government Publishing Office (Federal Register) · 5 December 2024 · p. 16
www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf#page=16
42. A **Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items.** U.S. Government Publishing Office (Federal Register) · 5 December 2024 · p. 28
www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf#page=28
43. A **Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items.** U.S. Government Publishing Office (Federal Register) · 5 December 2024 · p. 21
www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf#page=21

44. A **Revocation of Validated End-User Authorizations in the People's Republic of China.** U.S. Government Publishing Office (Federal Register) · 2 September 2025
www.govinfo.gov/content/pkg/FR-2025-09-02/html/2025-16735.htm
45. A **Expansion of End-User Controls To Cover Affiliates of Certain Listed Entities.** U.S. Government Publishing Office (Federal Register) · 30 September 2025 · p. 1
www.govinfo.gov/content/pkg/FR-2025-09-30/pdf/2025-19001.pdf#page=1
46. A **One Year Suspension of Expansion of End-User Controls for Affiliates of Certain Listed Entities.** U.S. Government Publishing Office (Federal Register) · 12 November 2025
www.govinfo.gov/content/pkg/FR-2025-11-12/pdf/2025-19846.pdf
47. A **Applied Materials to Pay \$252 Million Penalty to BIS for Illegally Exporting Semiconductor Manufacturing Equipment.** U.S. Bureau of Industry and Security · 11 February 2026
www.bis.gov/press-release/applied-materials-pay-252-million-penalty-bis-illegally-exporting-semiconductor-manufacturing-equipment
48. A **Supply Chain Explorer: Advanced Chips.** Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N46&selectedNode=N53



01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Metrology and Inspection

KLA, an American firm, held 56.8 percent of the market for tools that measure and inspect wafers in 2025, by CSET's count.

Specimen 07 · Metrology and Inspection

An electron-beam inspection column, cut in half down its axis, standing over a 300 mm wafer. The column is about a meter tall, drawn to scale. The green line is the electron beam, running from the emitter at the top through the lenses to the spot where it lands on the wafer.

In plain terms

Metrology (measurement) and inspection are a chip factory's quality control. Between the steps that build a chip, another machine looks the wafer over. It checks whether the lines are the right width, whether this layer landed squarely on the last one, and whether a speck of dirt has killed a circuit. The main chip in an AI accelerator, the one that does the calculating, is one of the largest cut from a wafer. A bigger chip is a bigger target for a speck. In a textbook example with the same density of specks, 49.2 percent of chips 1 centimeter on a side come out flawless, but only 11.3 percent of chips 2 centimeters on a side¹. In 2025 one American firm, KLA, held 56.8 percent of the market for these tools, by CSET's count from TechInsights data². So most of the tools that a chip factory, or fab, uses to find faults come from KLA.

In short

By CSET's count from TechInsights data, defect inspection was the largest kind of measuring and inspection tool in 2025, a \$6.7 billion market². KLA held 85.9 percent of it². Chinese makers held 0.7 percent of the whole market that year by the same count². Yet China took 26 percent of KLA's revenue in the June 2026 quarter³.

Since October 2022 the US has required a license for any tool subject to US export rules bound for Chinese fabs that make advanced logic or memory chips⁴. A December 2024 rule added specific tools to the export control list, among them inspection tools that can find defects of 21 nm or smaller⁵.

¹ Behrooz Parhami, Dependable Computing: A Multilevel Approach, part 2. University of California, Santa Barbara, 11 October 2020, p. 8. web.ece.ucsb.edu

² Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

³ Letter to Shareholders Q4 Fiscal 2026. KLA Corporation, 28 July 2026, p. 5. d1io3yog@oux5.cloudfront.net

⁴ Implementation of Additional Export Controls: Certain Advanced Computing and... U.S. Government Publishing Office, 13 October 2022, p. 5. govinfo.gov

⁵ Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... U.S. Government Publishing Office, 5 December 2024, p. 18. govinfo.gov

Process control tools, the machines that measure and inspect wafers and masks, were a \$15.7 billion market in 2025, by CSET's count from TechInsights data². CSET is a research center at Georgetown University. KLA puts the whole wafer equipment market, including advanced packaging, at about \$120 billion that year⁶.

KLA held more than half of this market in 2025, several times the share of any rival. CSET's count puts KLA at 56.8 percent and Applied Materials, the next largest, at 11.2 percent². At its March 2026 investor day KLA cited Gartner's figures for 2024, which put its share at 56.5 percent, 6.5 times its nearest competitor's⁷. In April 2026 KLA said its 2025 share was about 7 times the nearest competitor's⁸.

Chokepoint card		Metrology and Inspection	
<div>Concentration</div> <div> High</div> <div>Four to six firms could supply this stage today, and the top two take most of the revenue.</div>		<div>Substitutability</div> <div>Moderate</div> <div>Every kind of measuring and inspecting tool had a second maker in 2025².</div>	
		<div>Price or market size</div> <div>\$15.7 billion</div> <div>process control tool market in 2025². KLA puts the 2025 wafer equipment market at about \$120 billion⁶</div>	
Who leads	US	KLA	56.8 percent of process control tools in 2025 by CSET's count ²
	US	Applied Materials	11.2 percent of process control tools in 2025 ²
	JP	Lasertec	6.4 percent of process control tools in 2025 ²
	JP	Hitachi High-Tech	6.2 percent of process control tools in 2025 ²
	NL	ASML	5.9 percent of process control tools in 2025 ²
	IL	Nova	4.3 percent of process control tools in 2025 ²
	US	Onto Innovation	2.6 percent of process control tools in 2025 ²
Where it is made	US	United States	KLA (Milpitas), Onto Innovation (Wilmington, MA), Applied Materials
	NL	Netherlands	ASML YieldStar and HMI e-beam, Veldhoven and San Jose
	JP	Japan	Hitachi High-Tech (CD-SEM), Lasertec (mask inspection), Rigaku (X-ray)
	IL	Israel	Nova (Rehovot) and Camtek (Migdal Haemek)
	CN	China	Skyverse (Shenzhen), RSIC and other domestic makers, with 0.7 percent of the market in 2025 by CSET's count
Why substitution is possible	Eight firms besides KLA each held more than 1 percent of the market in 2025 ² . But KLA alone held 85.9 percent of defect inspection, the largest kind, that year ² .		
Where China stands		Where the US stands	
Chinese firms held 0.7 percent of the world market for tools that measure and inspect wafers in 2025, by CSET's count ² . Skyverse, a Shenzhen maker of inspection and metrology tools, reported 2,053,298,171.74 yuan of revenue in 2025, up 48.75 percent on 2024 ⁹ .		In 2025 the American firm KLA was the world's largest maker of metrology and inspection tools ² . Citing Gartner, KLA puts its 2024 share at 56.5 percent, 6.5 times its nearest rival's share ⁷ .	

2 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

6 Letter to Shareholders Q4 Fiscal 2026. KLA Corporation, 28 July 2026, p. 7. d1io3yog0oux5.cloudfront.net

7 Compounding Sustainable Outperformance. KLA Corporation, 12 March 2026, p. 35. d1io3yog0oux5.cloudfront.net

8 Letter to Shareholders Q3 Fiscal 2026. KLA Corporation, 29 April 2026, p. 3. d1io3yog0oux5.cloudfront.net

9 深圳中科飞测科技股份有限公司2025年年度报告摘要. CNINFO, 24 April 2026, p. 12. static.cninfo.com.cn

01

How chipmakers measure and inspect wafers

An inspection tool sweeps a beam of light across the wafer, photographs it, and compares the image of each chip with the image of its neighbors. The chips on a wafer are meant to be identical, so the tool flags anything that shows in one and not the others as a possible defect. It records where each one is. For faults too small for light to show, a second tool scans a beam of electrons across a small patch and builds a picture from the electrons the beam knocks loose from the surface.

A metrology tool measures known shapes. It shines light on a test pattern printed beside the circuits and works out from the reflected light how wide the lines are and how thick the film is. It also reads marks printed in this layer and the last to measure how far the two are out of line, which chipmakers call overlay.

The fab pays for all this to protect yield, the share of chips on a wafer that work. A wafer loses value two ways: whole regions ruined by mishandling, misalignment or over-etching, and single circuits killed by stray material or an airborne particle¹⁰.

A bigger chip is a bigger target for the second kind, so the cost of each good chip grows faster than its area¹. Chipmakers call each chip on a wafer a die. In the standard formula, die yield is $(1 + D0A/a)^{-a}$ to the power minus a. Here D0 is defects per square centimeter, A is die area, and a is a clustering constant of 3 to 4 that says how much defects bunch together. At a defect density of 0.8 per square centimeter, with a set to 3, a 1 square centimeter die yields 49.2 percent and a 2 by 2 centimeter die 11.3 percent¹. Because the bigger die yields less and fits fewer times on a wafer, it costs 20.1 times as much as the small one¹.

One percentage point of yield can be worth millions of dollars a year. In another textbook example, a fab makes 5,000 wafers a week, each holding 200 dies, and earns \$15 from each good die¹¹. Each percentage point of yield is then worth \$7.8 million a year¹¹. Engineers raise yield by finding the process step that is losing dies and fixing it, work called yield learning.

Chipmakers can sell more dies than the formula suggests, because its percentages count only dies with no killer defect. A chip built from many identical blocks can carry spares and switch off a faulty block¹². Nvidia's full H100 design has 144 of its main computing blocks, called streaming multiprocessors, and the SXM5 version it ships has 132 turned on¹³. But the formula shows how fast flawless dies get scarce as chips grow.

¹ Behrooz Parhami, Dependable Computing: A Multilevel Approach, part 2. University of California, Santa Barbara, 11 October 2020, p. 8. web.ece.ucsb.edu

¹⁰ Behrooz Parhami, Dependable Computing: A Multilevel Approach, part 2. University of California, Santa Barbara, 11 October 2020, p. 10. web.ece.ucsb.edu

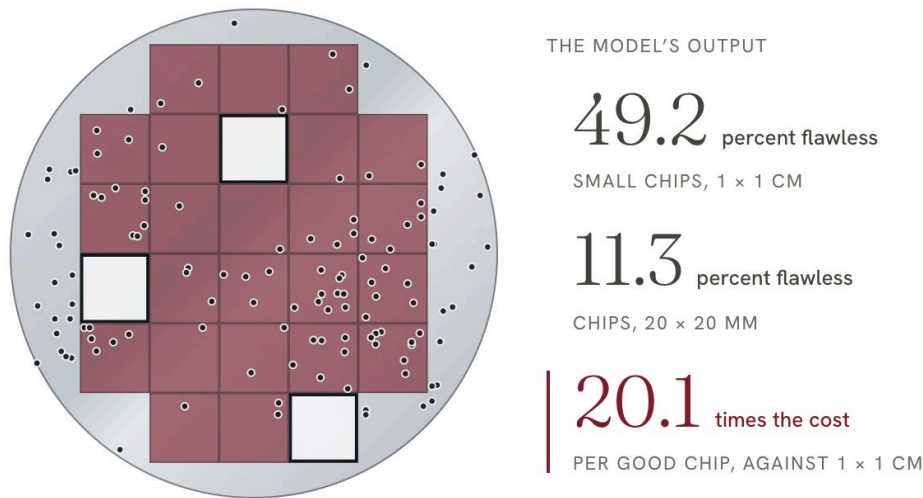
¹¹ Behrooz Parhami, Dependable Computing: A Multilevel Approach, part 2. University of California, Santa Barbara, 11 October 2020, p. 7. web.ece.ucsb.edu

¹² Behrooz Parhami, Dependable Computing: A Multilevel Approach, part 2. University of California, Santa Barbara, 11 October 2020, p. 23. web.ece.ucsb.edu

¹³ NVIDIA Hopper Architecture In-Depth. Nvidia, 22 March 2022. developer.nvidia.com

Figure 07.1 · Interactive explainer

Why big chips lose more to defects



1. **Specks land.** Specks of dust and tiny flaws land at random on every wafer. A textbook example assumes 0.8 per square centimeter.
2. **Small chips.** Of chips 1 centimeter on a side, 49.2 percent miss every speck and come out flawless.
3. **Big chips.** Chips 2 centimeters on a side are bigger targets for the same specks. Only 11.3 percent come out flawless.
4. **The cost.** The big chip yields less and fits fewer times on a wafer, so it costs 20.1 times as much as the small one.

Note: Simulated wafer laid out like the textbook example: 120 chips 1 centimeter on a side, or 26 chips 2 centimeters on a side. Other sizes fill the same wafer with whole chips only. Specks land at random in loose clusters, at the density set. The share of flawless chips follows the formula above, with a clustering constant of 3, as closely as whole chips allow. The cost compares good chips per wafer, from the shares as shown.

02

Types of inspection and measuring tools

All the market sizes and shares below are CSET's, for 2025, from TechInsights data².

- **Defect inspection** scans a whole wafer with light, or small areas of it with electrons, and compares each die against its neighbors. It is by far the largest family, at \$6.7 billion, and KLA held 85.9 percent of it. ASML's HMI eScan 1100 runs 25 electron beams at once, up to 15 times the throughput of single-beam inspection tools, and finds patterning defects down to 7 nm¹⁴.
- **Film and shape metrology** measures how thick each film is and how flat the wafer is, without cutting it open. In this \$2.6 billion family KLA held 45.6 percent, Nova 24.6 and Onto Innovation 10.9. Onto paid about \$720 million in August 2026 for 27 percent of the Japanese X-ray tool maker Rigaku¹⁵.

² Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

¹⁴ The HMI eScan 1100. ASML, accessed 9 September 2026. asml.com

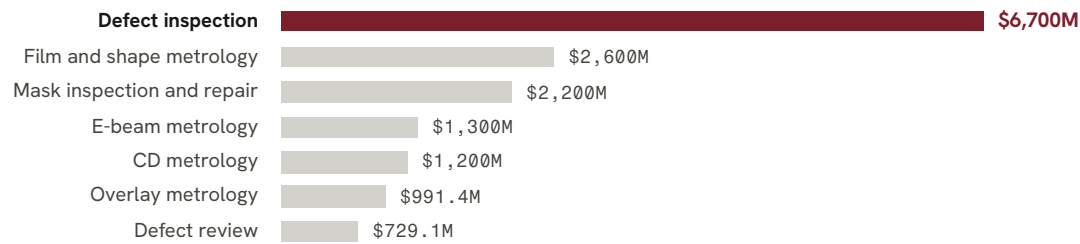
¹⁵ Onto Innovation Completes Strategic Investment in Rigaku Holdings Corporation. Onto Innovation, 10 August 2026. investors.ontoinnovation.com

- **Mask inspection and repair** has its own tools, because a defect on a mask, the stencil the circuit pattern is printed from, repeats on every die. This \$2.2 billion family and overlay metrology are the two where KLA has a close rival. KLA held 45.9 percent, Lasertec 42 and Zeiss 10.1. Lasertec also makes actinic inspection tools, which check EUV masks with the same 13.5 nm light that prints them¹⁶. Lasertec calls its ACTIS A150 the world's first EUV patterned mask inspection system¹⁶. KLA's own actinic mask inspection tool was still at an early demo stage at its March 2026 investor day¹⁷.
- **Overlay metrology** measures how well this layer lines up with the one below. Its \$991.4 million market was split almost evenly between KLA at 51.5 percent and ASML at 47.9.
- **Critical dimension metrology**, also called line-width measurement, measures how wide a printed feature came out. It is the one family Japan leads. Hitachi held 71.9 percent of this \$1.2 billion market and Applied Materials 27.5.
- **Electron-beam metrology** resolves detail too fine for light. Applied Materials led this \$1.3 billion family at 45.1 percent, with ASML at 35.6 and KLA at 18.8.

Figure 07.2

Defect inspection was the largest tool family in 2025, at \$6,700 million

Process control market by tool family, 2025



Source: ETO Supply Chain Explorer, CSET [2]

03

KLA and its smaller rivals

KLA says its share grew 3.6 percentage points from 2021 to 2025⁸. It says it gained share again in 2025 across mask, optical wafer and e-beam inspection⁸. Its revenue for fiscal 2026, the year to June 2026, was \$13.579 billion, up from \$12.156 billion in fiscal 2025¹⁸.

2 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

8 Letter to Shareholders Q3 Fiscal 2026. KLA Corporation, 29 April 2026, p. 3. d1io3yog@oux5.cloudfront.net

16 ACTIS A150. Lasertec, 12 September 2019. lasertec.co.jp

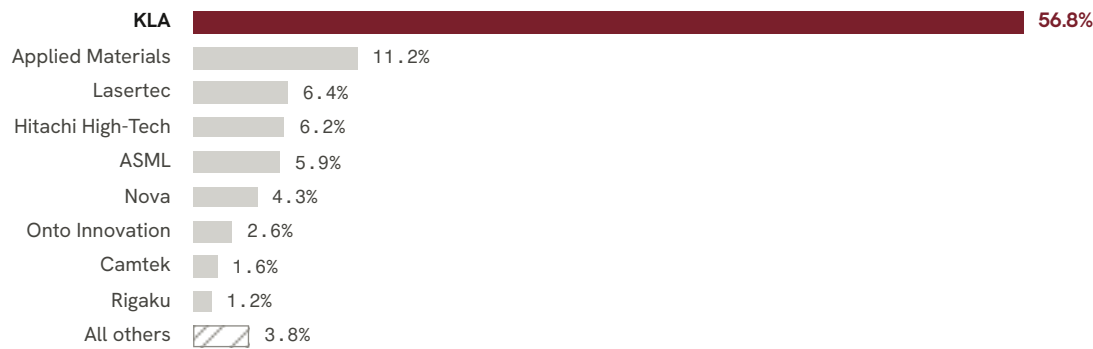
17 Compounding Sustainable Outperformance. KLA Corporation, 12 March 2026, p. 91. d1io3yog@oux5.cloudfront.net

18 KLA, revenue reported to the SEC (XBRL company data). U.S. Securities and Exchange Commission, accessed 9 September 2026. data.sec.gov

Figure 07.3

KLA held 56.8 percent of process control tool revenue in 2025

Process control tool revenue share, 2025



Source: ETO Supply Chain Explorer, CSET [2]

KLA's rivals are far smaller, and none holds more than 11.2 percent, by CSET's count from TechInsights data for 2025². Eight of them each held more than 1 percent of the market that year².

- **Applied Materials** is the largest of them. It sells e-beam defect review tools, CD-SEMs (electron microscopes that measure line width) and e-beam metrology tools next to the deposition and etch tools whose work they check.
- **Lasertec** holds 6.4 percent, almost all of it mask inspection². **Hitachi High-Tech** holds 6.2 percent, most of it from CD-SEMs². **ASML** holds 5.9 percent through YieldStar overlay and HMI e-beam metrology².
- **Nova** holds 4.3 percent, through film metrology². It took \$880.6 million of revenue in 2025¹⁹.
- **Onto Innovation** holds 2.6 percent². It took \$1,005.3 million of revenue in 2025²⁰.
- **Camtek** holds 1.6 percent². It took \$496.1 million of revenue in 2025²¹.

KLA's patterning line, which includes several metrology products and mask inspection, grew 61 percent year on year in the June 2026 quarter³.

KLA says process control's share of spending on chipmaking equipment is still rising²². For memory chips, KLA credits the rise to higher performance specifications, fewer spare circuits and more logic circuitry in devices built for high-performance computing²³.

KLA says its systems use AI to analyze data and suppress noise, and that this helps chipmakers reach high yield sooner²³. In April 2026 KLA said it had added AI to every product line over the previous five years²³.

2 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

3 Letter to Shareholders Q4 Fiscal 2026. KLA Corporation, 28 July 2026, p. 5. d1io3yog@oux5.cloudfront.net

19 Nova, revenue reported to the SEC (XBRL company data). U.S. Securities and Exchange Commission, accessed 9 September 2026. data.sec.gov

20 Onto Innovation Reports 2025 Fourth Quarter and Full Year Results. Onto Innovation, 19 February 2026. investors.ontoinnovation.com

21 Camtek, report on Form 6-K dated 18 February 2026. U.S. Securities and Exchange Commission, 18 February 2026. sec.gov

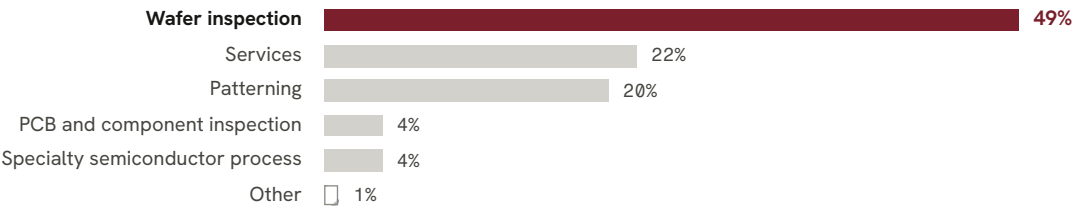
22 Letter to Shareholders Q3 Fiscal 2026. KLA Corporation, 29 April 2026, p. 12. d1io3yog@oux5.cloudfront.net

23 Letter to Shareholders Q3 Fiscal 2026. KLA Corporation, 29 April 2026, p. 4. d1io3yog@oux5.cloudfront.net

Figure 07.4

Wafer inspection was 49 percent of KLA's June 2026 quarter revenue

KLA revenue by product line, June 2026 quarter



Source: KLA letter to shareholders, Q4 FY2026 [3]

04

Packaging inspection, China's toolmakers and export controls

KLA says the AI build-out is making advanced packaging, and the process control it needs, more important²⁴. KLA says it became the largest supplier of process control tools for advanced wafer-level packaging in 2025, adding 14 percentage points of share⁸. It expects about \$1.1 billion of packaging process control revenue in 2026, up more than 70 percent²⁴. In February 2026 Onto said it had signed a volume purchase agreement estimated at over \$240 million with a high-bandwidth memory (HBM) maker²⁰. The deal covers 2D inspection and 3D bump metrology, which measures the tiny metal bumps that join stacked chips, through 2027²⁰.

Chinese makers are still small in process control, but one of them is growing fast. CSET's count, built on TechInsights data, puts all Chinese firms at 0.7 percent of the market in 2025². Skyverse (Shenzhen Zhongke Feice), a maker of wafer inspection and metrology tools, reported 2,053,298,171.74 yuan of revenue in 2025⁹. That was up 48.75 percent on 2024⁹. In its 2025 annual report Skyverse says Chinese makers still hold a low share of China's market for these tools and that KLA holds the largest share of it²⁵. In the June 2026 quarter China took 26 percent of KLA's revenue and Taiwan 31 percent³.

Chinese firms held 2 percent or less of each of five kinds of tool in 2025. By CSET's 2025 count from TechInsights data, they held 0.6 percent of defect inspection tools²⁶. They held 0.4 percent of line-width measurement tools in 2025²⁷. In film and shape metrology they held 2 percent in 2025, all of it from Raintree Scientific Instruments, or

2 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

3 Letter to Shareholders Q4 Fiscal 2026. KLA Corporation, 28 July 2026, p. 5. d1io3yog@oux5.cloudfront.net

8 Letter to Shareholders Q3 Fiscal 2026. KLA Corporation, 29 April 2026, p. 3. d1io3yog@oux5.cloudfront.net

9 深圳中科飞测科技股份有限公司2025年年度报告摘要. CNINFO, 24 April 2026, p. 12. static.cninfo.com.cn

20 Onto Innovation Reports 2025 Fourth Quarter and Full Year Results. Onto Innovation, 19 February 2026. investors.ontoinnovation.com

24 Letter to Shareholders Q4 Fiscal 2026. KLA Corporation, 28 July 2026, p. 2. d1io3yog@oux5.cloudfront.net

25 深圳中科飞测科技股份有限公司2025年年度报告摘要. CNINFO, 24 April 2026, p. 11. static.cninfo.com.cn

26 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

27 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

RSIC²⁸. They held no share of mask inspection and repair tools in 2025²⁹. Nor did they hold any share that year of the tools that inspect wafers during advanced packaging³⁰.

In October 2022 the US began requiring a license for any item subject to US export rules, process control tools included, bound for certain Chinese fabs⁴. The rule covered fabs that made logic chips at 16/14 nm or below, NAND memory with 128 or more layers, or DRAM at 18 nm half-pitch or below³¹.

A December 2024 rule added specific process control tools to the export control list. It controls tools for defect inspection and measurement of patterned 300 mm wafers if they can find defects of 21 nm or smaller³². The control covers only tools that do this using light with a wavelength below 400 nm, an electron beam with a resolution of 1.65 nm or better, a cold field emission source, or two or more electron-beam sources³². The same rule controls overlay metrology accurate to 0.5 nm or better in two cases³². One is a tool built into the track, the machine that coats and develops the light-sensitive resist³³. The other is a tool that can change its measurement wavelength and take a measurement in less than 25 ms³³. It also controls stand-alone wafer shape metrology that feeds corrections to immersion or EUV scanners³². A separate new entry, 3B994, covers optical film and line-width metrology for 300 mm wafers with software for measuring non-planar transistors³³.

BIS, the US Commerce Department bureau that wrote the rule, placed all of these tools in two new entries, 3B993 and 3B994, for items it says also have legitimate uses in older chipmaking³⁴. For that reason BIS decided that, unlike tools built only for advanced chips, they do not warrant a license requirement covering a whole country or a presumption that BIS will refuse a license³⁴. A new foreign direct product rule extends US jurisdiction to specified foreign-made chipmaking tools bound for Macau or for a Country Group D:5 destination such as China³⁵.

05

Why KLA's inspection tools are a chokepoint

A fab that can buy scanners and etchers but not sensitive inspection tools finds fewer of the defects that lower its yield, so its yield rises more slowly. Most of those tools come from one firm, KLA, which held more than half the process control market in 2025². KLA led four kinds of process control tool that year, by CSET's count². It held

² Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

⁴ Implementation of Additional Export Controls: Certain Advanced Computing and... U.S. Government Publishing Office, 13 October 2022, p. 5. [govinfo.gov](https://www.govinfo.gov)

²⁸ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

²⁹ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

³⁰ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

³¹ Implementation of Additional Export Controls: Certain Advanced Computing and... U.S. Government Publishing Office, 13 October 2022, p. 16. [govinfo.gov](https://www.govinfo.gov)

³² Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... U.S. Government Publishing Office, 5 December 2024, p. 37. [govinfo.gov](https://www.govinfo.gov)

³³ Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... U.S. Government Publishing Office, 5 December 2024, p. 38. [govinfo.gov](https://www.govinfo.gov)

³⁴ Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... U.S. Government Publishing Office, 5 December 2024, p. 17. [govinfo.gov](https://www.govinfo.gov)

³⁵ Commerce Strengthens Export Controls to Restrict China's Capability to Produce... U.S. Bureau of Industry and Security, 2 December 2024. [bis.gov](https://www.bis.gov)

85.9 percent of defect inspection, the largest kind². Still, every kind of process control tool had a second maker that year, by CSET's count from TechInsights data². KLA says its share of the whole market grew from 2021 to 2025⁸.

Four questions to answer from memory

1. What do metrology and inspection tools do? see How it works
 2. Why do large AI chips depend so much on finding defects? see How it works
 3. Which company leads in these tools?
 4. Can a chip factory buy these tools from a firm other than KLA?
see Variants and trade-offs
-

Four things to remember

- Metrology and inspection tools check each wafer between steps and help a fab find out why its chips fail.
 - AI chips are among the largest made, so finding defects matters most for them.
 - CSET's count puts KLA of the United States at 56.8 percent of this tool market in 2025, and Applied Materials, the next largest, at 11.2 percent.
 - Chinese makers held 0.7 percent of this tool market in 2025 on CSET's count, though one Chinese maker, Skyverse, grew its revenue 48.75 percent that year.
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Sources (35)

1. A Behrooz Parhami, Dependable Computing: A Multilevel Approach, part 2. University of California, Santa Barbara · 11 October 2020 · p. 8
web.ece.ucsb.edu/~parhami/docs_folder/f33-book-dep-comp-pt2.pdf#page=8
2. A Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N118&selectedNode=N60
3. A Letter to Shareholders Q4 Fiscal 2026. KLA Corporation · 28 July 2026 · p. 5
d11o3yog0oux5.cloudfront.net/_b9ee755a5f60dd0fb3f9e27967aed6af/klatencor/db/1117/10668/letter_to_shareholders/KLA+Earnings+Shareholder+Letter+--+Q4+FY26.pdf#page=5
4. A Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification. U.S. Government Publishing Office (Federal Register) · 13 October 2022 · p. 5
www.govinfo.gov/content/pkg/FR-2022-10-13/pdf/2022-21658.pdf#page=5
5. A Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 5 December 2024 · p. 18
www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf#page=18
6. A Letter to Shareholders Q4 Fiscal 2026. KLA Corporation · 28 July 2026 · p. 7
d11o3yog0oux5.cloudfront.net/_b9ee755a5f60dd0fb3f9e27967aed6af/klatencor/db/1117/10668/letter_to_shareholders/KLA+Earnings+Shareholder+Letter+--+Q4+FY26.pdf#page=7
7. A Compounding Sustainable Outperformance. KLA Corporation · 12 March 2026 · p. 35
d11o3yog0oux5.cloudfront.net/_7791115a123b86b3f10b1a5eb5210224/klatencor/db/1166/10653/file/2026+Investor+Day+Master+Final_IR+copy.pdf#page=35
8. A Letter to Shareholders Q3 Fiscal 2026. KLA Corporation · 29 April 2026 · p. 3
d11o3yog0oux5.cloudfront.net/_a357bfc9113388e37f3bfc2ea2f0b64/klatencor/db/1117/10655/letter_to_shareholders/KLA+Shareholder+Letter+--+Q3+FY26.pdf#page=3
9. A 深圳中科飞测科技股份有限公司2025年年度报告摘要. CNINFO · 24 April 2026 · p. 12
static.cninfo.com.cn/finalpage/2026-04-25/1225182755.PDF#page=12
10. A Behrooz Parhami, Dependable Computing: A Multilevel Approach, part 2. University of California, Santa Barbara · 11 October 2020 · p. 10
web.ece.ucsb.edu/~parhami/docs_folder/f33-book-dep-comp-pt2.pdf#page=10

² Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026.
chipexplorer.eto.tech

⁸ Letter to Shareholders Q3 Fiscal 2026. KLA Corporation, 29 April 2026, p. 3. d11o3yog0oux5.cloudfront.net

11. A Behrooz Parhami, Dependable Computing: A Multilevel Approach, part 2. University of California, Santa Barbara · 11 October 2020 · p. 7
web.ece.ucsb.edu/~parhami/docs_folder/f33-book-dep-comp-pt2.pdf#page=7
12. A Behrooz Parhami, Dependable Computing: A Multilevel Approach, part 2. University of California, Santa Barbara · 11 October 2020 · p. 23
web.ece.ucsb.edu/~parhami/docs_folder/f33-book-dep-comp-pt2.pdf#page=23
13. A NVIDIA Hopper Architecture In-Depth. Nvidia · 22 March 2022
developer.nvidia.com/blog/nvidia-hopper-architecture-in-depth/
14. A The HMI eScan 1100. ASML · Accessed 9 September 2026
www.asml.com/en/products/metrology-and-inspection-systems/hmi-escan-1100
15. A Onto Innovation Completes Strategic Investment in Rigaku Holdings Corporation. Onto Innovation · 10 August 2026
investors.ontoinnovation.com/news/news-details/2026/Onto-Innovation-Completes-Strategic-Investment-in-Rigaku-Holdings-Corporation/default.aspx
16. A ACTIS A150. Lasertec · 12 September 2019
www.lasertec.co.jp/en/products/semiconductor/actis_a150.html
17. A Compounding Sustainable Outperformance. KLA Corporation · 12 March 2026 · p. 91
d1io3yog0oux5.cloudfront.net/_7791115a123b86b3f10b1a5eb5210224/klatencor/db/1166/10653/file/2026+Investor+Day+Master+Final_IR+copy.pdf#page=91
18. A KLA, revenue reported to the SEC (XBRL company data). U.S. Securities and Exchange Commission (XBRL data for KLA) · Accessed 9 September 2026
data.sec.gov/api/xbrl/companyconcept/CIK0000319201/us-gaap/RevenueFromContractWithCustomerExcludingAssessedTax.json
19. A Nova, revenue reported to the SEC (XBRL company data). U.S. Securities and Exchange Commission (XBRL data for Nova) · Accessed 9 September 2026
data.sec.gov/api/xbrl/companyconcept/CIK0001109345/us-gaap/Revenues.json
20. A Onto Innovation Reports 2025 Fourth Quarter and Full Year Results. Onto Innovation · 19 February 2026
investors.ontoinnovation.com/news/news-details/2026/Onto-Innovation-Reports-2025-Fourth-Quarter-and-Full-Year-Results/default.aspx
21. A Camtek, report on Form 6-K dated 18 February 2026. U.S. Securities and Exchange Commission (filing by Camtek) · 18 February 2026
www.sec.gov/Archives/edgar/data/1109138/000117891326000549/zk2634405.htm
22. A Letter to Shareholders Q3 Fiscal 2026. KLA Corporation · 29 April 2026 · p. 12
d1io3yog0oux5.cloudfront.net/_a357bfc9113388e37f3bfc2ea2f0b64/klatencor/db/1117/10655/letter_to_shareholders/KLA+Shareholder+Letter--+Q3+FY26.pdf#page=12
23. A Letter to Shareholders Q3 Fiscal 2026. KLA Corporation · 29 April 2026 · p. 4
d1io3yog0oux5.cloudfront.net/_a357bfc9113388e37f3bfc2ea2f0b64/klatencor/db/1117/10655/letter_to_shareholders/KLA+Shareholder+Letter--+Q3+FY26.pdf#page=4
24. A Letter to Shareholders Q4 Fiscal 2026. KLA Corporation · 28 July 2026 · p. 2
d1io3yog0oux5.cloudfront.net/_b9ee755a5f60dd0fb3f9e27967aed6af/klatencor/db/1117/10668/letter_to_shareholders/KLA+Earnings+Shareholder+Letter--+Q4+FY26.pdf#page=2
25. A 深圳中科飞测科技股份有限公司2025年年度报告摘要. CNINFO · 24 April 2026 · p. 11
static.cninfo.com.cn/finalpage/2026-04-25/1225182755.PDF#page=11
26. A Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N118&selectedNode=N67
27. A Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N118&selectedNode=N66
28. A Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N118&selectedNode=N65
29. A Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N118&selectedNode=N62
30. A Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N69&selectedNode=N63
31. A Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification. U.S. Government Publishing Office (Federal Register) · 13 October 2022 · p. 16
www.govinfo.gov/content/pkg/FR-2022-10-13/pdf/2022-21658.pdf#page=16
32. A Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 5 December 2024 · p. 37
www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf#page=37
33. A Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 5 December 2024 · p. 38
www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf#page=38
34. A Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items. U.S. Government Publishing Office (Federal Register) · 5 December 2024 · p. 17
www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf#page=17

35. A **Commerce Strengthens Export Controls to Restrict China's Capability to Produce Advanced Semiconductors for Military Applications.** U.S. Bureau of Industry and Security · 2 December 2024
www.bis.gov/press-release/commerce-strengthens-export-controls-restrict-chinas-capability-produce-advanced-semiconductors-military



01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Foundries and Fabs

The newest chips need the know-how to build the newest transistors and a fab that costs tens of billions of dollars. Only TSMC, Intel and Samsung have both.

Specimen 08 · Foundries and Fabs

A gate-all-around transistor, the switch in a 2 nm-class chip, drawn at true proportions. The three silicon sheets are each 6 nm thick and 30 nm wide. Each sheet is a few dozen atoms from top to bottom, roughly ten thousand times thinner than a human hair. The gold cage is the gate metal wrapping all four sides of each sheet.

In plain terms

A chip factory, or fab, builds the transistors, the billions of tiny switches in every chip, and then wires them together. Each switch works like a valve. Current runs along a narrow strip of silicon called the channel, and a small voltage on a gate above the strip opens or shuts the flow. For decades chipmakers made the strips shorter, so the transistors switched faster and more of them fit on a chip. But once the strip gets short enough, current leaks through even when the gate is off, and the chip burns power doing nothing. The newest kind of transistor, called gate-all-around, cuts this leak by wrapping the gate around all four sides of the strip. A chipmaker needs two things to make the newest chips, and having one does not bring the other. The first is the know-how to build the newest switches, a long sequence of steps that have to run in exact order. In 2026 only TSMC, Intel and Samsung had it. The second is factories that cost tens of billions of dollars each, and in 2022 most of the world's capacity for the most advanced logic chips was in Taiwan. China's SMIC runs factories, but without EUV machines or the know-how for the newest switches, its most advanced chips are 7 nm-class. IBM developed 2 nm technology, but it yields no chips until Rapidus finishes a factory to run it, with mass production planned for 2027. No chip company sells enough of one product to fill such a factory on its own, so chip companies share a handful of them, run by foundries that make chips for other companies. TSMC runs the biggest, and all six of its largest plants are in Taiwan.

In short

Since September 2024 the United States has required a license to share the know-how for building gate-all-around transistors, except with countries

that impose matching controls¹. China has announced \$43 billion to develop its own extreme ultraviolet (EUV) scanners, but in September 2025 the Center for Strategic and International Studies judged that EUV remains firmly out of reach².

SEMI projected in 2026 that China would keep the world's largest installed fab capacity in 2026 and 2027³. In July 2026 TSMC raised its planned investment in Arizona to \$265 billion across 12 facilities⁴. SIA and BCG projected in May 2024 that the US share of the world's logic capacity below 10 nm would rise from almost none in 2022 to 28 percent by 2032⁵.

Nvidia's Blackwell GPU holds 208 billion switches on two dies, each die the largest a lithography machine can print in one shot⁶. Every switch has to turn on fully, let almost no current through when off, and keep doing it for years. Blackwell is made by TSMC, on a custom process called 4NP⁶. TSMC calls a plant a GIGAFAB once it can run more than 100,000 wafers a month, each a 300 mm disc, twelve inches across⁷. It operates six of them, and every one is in Taiwan⁸.

Chokepoint card		Foundries and Fabs	
Concentration		Substitutability	Price or market size
 Extreme Three or fewer firms could supply this stage today, or one firm holds more than half of it.		Very hard Intel Foundry earned only \$293 million of its \$5.765 billion revenue in the second quarter of 2026 from outside customers ⁹ .	\$35 billion to \$43 billion over ten years to own a new 2 nm-class fab completed in 2026, BCG's 2023 estimate ¹⁰ . A 300 mm wafer on TSMC's 4NP process cost \$17,000, Epoch AI estimated in December 2025 ¹¹ .
Who leads	TW TSMC US Intel KR Samsung Foundry CN SMIC JP Rapidus	N2, its first nanosheet node, in volume production since 4Q25 ¹² 18A in high-volume production in the United States, as of 2026 ¹³ 3 nm gate-all-around process in initial production since June 2022 ¹⁴ \$9.327 billion revenue in 2025, with its lines 93.5 percent full ¹⁵ 267.6 billion yen raised in February 2026 to reach 2 nm mass production by 2027 ¹⁶	

1 Commerce Control List Additions and Revisions; Implementation of Controls on... Federal Register, 6 September 2024. federalregister.gov

2 Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements. Center for Strategic and International Studies, 24 September 2025. csis.org

3 World Fab Forecast. SEMI, accessed 9 September 2026. semi.org

4 TSMC Announces Additional \$100 Billion Investment In Arizona. City of Phoenix, 16 July 2026. phoenix.gov

5 Emerging Resilience in the Semiconductor Supply Chain. Boston Consulting Group and Semiconductor Industry..., May 2024, p. 14. semiconductors.org

6 NVIDIA Blackwell Architecture. Nvidia, 18 December 2025. nvidia.com

7 GIGAFAB® Facilities. TSMC, accessed 9 September 2026. tsmc.com

8 Fab Capacity. TSMC, accessed 9 September 2026. tsmc.com

9 Intel, quarterly report on Form 10-Q for the quarter ended 27 June 2026. U.S. Securities and Exchange Commission, 24 July 2026. sec.gov

10 Navigating the Costly Economics of Chip Making. Boston Consulting Group, 28 September 2023. bcg.com

11 NVIDIA's B200 costs around \$6,400 to produce. Epoch AI, 10 December 2025. epoch.ai

12 2nm Technology. TSMC, accessed 9 September 2026. tsmc.com

13 Intel 18A: See Our Biggest Process Innovation. Intel, accessed 18 October 2026. intel.com

14 Samsung Begins Chip Production Using 3nm Process Technology With GAA... Samsung Global Newsroom, 30 June 2022. news.samsung.com

15 SMIC Announces 2025 Annual Results. SMIC, 26 March 2026. smics.com

16 Rapidus Secures 267.6 Billion Yen in Funding from Japan Government and Private... Rapidus, 27 February 2026. rapidus.inc

chipsupplychain.org · Edition of 29 October 2026

86 / 190

Where it is made	TW	Taiwan	TSMC's six gigafabs, with N2 at Fab 20 Hsinchu and Fab 22 Kaohsiung, and UMC
	KR	South Korea	Samsung Foundry, Hwaseong and Pyeongtaek
	US	United States	Intel 18A at Fab 52 in Arizona, TSMC Arizona, Samsung Taylor and GlobalFoundries
	JP	Japan	Rapidus Chitose, Hokkaido, and TSMC Kumamoto
	CN	China	SMIC Shanghai and Beijing 300 mm lines, and Hua Hong
Why substitution is slow	Since September 2024 the United States has required a license to share the know-how for building gate-all-around transistors, except with countries that impose matching controls ¹ . In March 2026 the Semiconductor Industry Association (SIA) put the cost to build and equip a leading-edge fab at as much as \$20 to \$25 billion ¹⁷ . SemiAnalysis judged in December 2025 that finding the highly skilled engineers a foundry needs remained a major challenge for TSMC in Arizona ¹⁸ .		
Where China stands		Where the US stands	
China's SMIC made its most advanced chips on N+3, a 7 nm-class process built without extreme ultraviolet scanners, SemiAnalysis found in June 2026 ¹⁹ . SMIC cannot buy those scanners, so it prints its tightest layers in several passes on older deep-ultraviolet machines ¹⁹ . China will keep the world's largest installed fab capacity in 2026 and 2027, SEMI projected in its third-quarter 2026 forecast ³ .		Intel is the only chipmaker that both develops and manufactures leading-edge logic chips in the United States, by its own account in August 2025 ²⁰ . The United States had almost no logic capacity below 10 nm in 2022, and SIA and BCG projected in May 2024 that its share would reach 28 percent by 2032 ⁵ . In July 2026 TSMC raised its planned investment in Arizona to \$265 billion across 12 facilities ⁴ . The US government agreed in August 2025 to buy a passive 9.9 percent stake in Intel, with no board seat ²⁰ .	

1 Commerce Control List Additions and Revisions; Implementation of Controls on... Federal Register, 6 September 2024. federalregister.gov

3 World Fab Forecast. SEMI, accessed 9 September 2026. semi.org

4 TSMC Announces Additional \$100 Billion Investment In Arizona. City of Phoenix, 16 July 2026. phoenix.gov

5 Emerging Resilience in the Semiconductor Supply Chain. Boston Consulting Group and Semiconductor Industry..., May 2024, p. 14. semiconductors.org

17 Testimony of the Semiconductor Industry Association (SIA) before the Senate... U.S. Senate Committee on Environment and Public Works, 4 March 2026, p. 3. epw.senate.gov

18 TSMC Overseas Fabs – A Success? SemiAnalysis, 1 December 2025. newsletter.semianalysis.com

19 Is SMIC N+3's Metal Pitch Smaller than Intel 18A's? SemiAnalysis, 14 June 2026. newsletter.semianalysis.com

20 Intel and Trump Administration Reach Historic Agreement to Accelerate American... Intel, 22 August 2025. intc.com

01

How a transistor works and why it leaks

Current leaks in two main ways, straight through the gate insulator and along the channel from end to end while the gate is off. The second leak grows as the channel gets shorter. Three fixes deal with the two leaks:

- **Better insulator.** A thicker hafnium-based film, paired with a metal gate, lets fewer electrons slip straight through yet controls the channel as tightly as before. Intel replaced the silicon dioxide insulator with it at 45 nm in 2007²¹. It said the new film cut leakage through the insulator more than tenfold²¹.
- **More gate.** A planar transistor lays the gate on one side of a flat channel, and as the channel shortens the gate loses control of it. A FinFET stands the channel on edge as a fin, so the gate covers three sides, and gate-all-around wraps it around all four.
- **Thinner channel.** The fab thins the silicon until no current can flow where the gate cannot reach it.

Figure 08.1 · Explainer, 23 seconds

Why the gate wraps around the channel

Wrap the gate all around

Shut far tighter, so switches can keep shrinking



1. **Inside a chip.** An AI chip does all its work with transistors, tiny switches built into the silicon. One Nvidia Blackwell GPU holds 208 billion of them. Making the switches is the front end of the factory, and wiring them together comes after.
2. **On.** Each one is a switch. Seen end on, current flows through a strip of silicon, the channel, and the gate sits on top.
3. **Off, leaking.** Switching off, the gate squeezes the flow shut, but only near itself. In a tiny transistor, current still leaks through the part it cannot reach.
4. **Fin.** Stand the channel on edge as a fin, and the gate covers three sides. Much less gets through.
5. **All around.** Split it into thin sheets and wrap the gate around every side, and it shuts far tighter. That lets the switches keep shrinking, so each new chip can pack in more of them.

Note: Simplified. The channel is seen end on, cut across the gate, with current drawn as points of light. Not to scale.

²¹ Intel's Transistor Technology Breakthrough Represents Biggest Change to... Intel, 27 January 2007. [intel.com](https://www.intel.com)

02

How transistors are built

Making the switches is called the front end of line. It builds them in a fixed order, starting with the channel. In a FinFET, the older design, the fab etches the silicon into thin fins that stand up from the wafer, and the gate goes over each one.

In a gate-all-around transistor, the fab instead grows alternating layers of silicon and silicon-germanium and cuts the stack into narrow bars²². It lays a placeholder, called a dummy gate, across each bar where the real gate will go²³. On either side of the placeholder it cuts deep trenches where the source and drain, the two ends of the channel, will go²⁴. Through those trenches it etches the silicon-germanium layers back a little and fills the gaps with an insulator, the inner spacer, which keeps the gate apart from the source and drain²². Then it grows the source and drain as crystal inside the trenches, a step called epitaxy²⁴.

Only then does the fab remove the placeholder and etch away the silicon-germanium, leaving thin silicon sheets that hang between the source and drain like shelves²². The inner spacer shields the source and drain from that etch²³. The fab coats every sheet with an insulating film a few atoms thick, so the gate can control the channel without touching it. Gate metal then fills the gaps above, below and beside each sheet, covering all four sides²⁵. Last come the contacts, small metal plugs down to the source, the drain and the gate, ready for the wiring layers above.

The steps have to run in exact order, because later layers cover earlier ones. Once gate metal surrounds a sheet, the insulating film can no longer go between the sheet and the metal. Each step is a separate deposition, etch or implant. An implant step, called ion implantation, fires atoms of boron or phosphorus into chosen patches of silicon so they conduct the way the design needs.

03

The newest transistor designs

Gate-all-around nanosheets

A nanosheet transistor lays the channel flat again, stacks two to four thin sheets and wraps gate metal around each one. Each fin in a FinFET adds a fixed amount of current, so a designer who needs more current has to add a whole fin. Nanosheets can be drawn at different widths, so current can be set in finer steps.

TSMC's N2, its first nanosheet node, entered volume production in the fourth quarter of 2025¹². TSMC rates the follow-on N2P at 18 percent more speed at the same power and 36 percent less power at the same speed than its earlier N3E²⁶. It gives N2P 1.2 times the logic density of N3E and 1.15 times its chip density, but its technology page

¹² 2nm Technology. TSMC, accessed 9 September 2026. [tsmc.com](https://www.tsmc.com)

²² Entering the nanosheet transistor era. Imec, 11 February 2022. [imec-int.com](https://www.imec-int.com)

²³ Development of SiGe Indentation Process Control for Gate-All-Around FET... ArXiv, 12 January 2022. arxiv.org

²⁴ Applied Materials Unveils Next-Gen Chipmaking Products to Supercharge AI... Applied Materials, 7 October 2025. [ir.appliedmaterials.com](https://www.appliedmaterials.com)

²⁵ Applied Materials Technologies Enable 2D Scaling with EUV and 3D... Applied Materials, 21 April 2022. [ir.appliedmaterials.com](https://www.appliedmaterials.com)

²⁶ HPC Platform – Advanced Technologies. TSMC, accessed 9 September 2026. [tsmc.com](https://www.tsmc.com)

does not define either measure²⁶. These numbers are TSMC's own claims until someone measures the silicon. Each foundry picks its own baseline, and none publishes a density figure that can be compared with a rival's.

Intel and Samsung also make gate-all-around transistors. Intel's version, called RibbonFET, is built into its 18A process, which Intel says is in high-volume production in the United States¹³. Samsung got there first, starting initial production of its 3 nm gate-all-around process in June 2022¹⁴. But SemiAnalysis reported in February 2023 that, because of yield problems, high-volume chips on Samsung's 3 nm gate-all-around technology were expected only in 2024²⁷.

SemiAnalysis reported in 2024 that the SRAM cell, which holds one bit in the fast memory on a logic die, had barely shrunk since the 5 nm node²⁸. TSMC said in 2025 that its 2 nm SRAM uses a 0.021 square-micrometer cell and gets 1.1 times the density of its previous node by tuning design and process together²⁹. See Memory and HBM.

Backside power delivery

In a conventional chip, power and signal share one stack of copper wiring above the transistors, where wide power rails crowd out the signal wires. With backside power, the fab grinds the wafer thin and builds a second network for power underneath it.

Intel's version, PowerVia, is part of 18A, and Intel calls it an industry first¹³. It cut routed area, the space a block of circuits takes once its wiring is laid out, by 11 percent and dynamic voltage droop tenfold³⁰. Droop is the sag in supply voltage when a block of logic switches on at once. TSMC's Super Power Rail connects the backside network directly to each transistor's source and drain²⁸. Against N2P, TSMC rates A16, which uses Super Power Rail, at 8 to 10 percent more speed, 15 to 20 percent less power and up to 1.10 times the chip density²⁶.

TSMC plans to start A14 production in 2028, with more than 20 percent higher logic density than N2³¹. It said in April 2026 that two more processes, A13 and A12, are scheduled to enter production in 2029³².

13 Intel 18A: See Our Biggest Process Innovation. Intel, accessed 18 October 2026. [intel.com](https://www.intel.com)

14 Samsung Begins Chip Production Using 3nm Process Technology With GAA... Samsung Global Newsroom, 30 June 2022. news.samsung.com

26 HPC Platform – Advanced Technologies. TSMC, accessed 9 September 2026. [tsmc.com](https://www.tsmc.com)

27 The Future of the Transistor. SemiAnalysis, 21 February 2023. newsletter.semianalysis.com

28 Clash of the Foundries: Gate All Around + Backside Power at 2nm. SemiAnalysis, 1 October 2024. newsletter.semianalysis.com

29 A 38.1Mb/mm² SRAM in a 2nm-CMOS-Nanosheet Technology for High-Density and... TSMC, 2025. research.tsmc.com

30 Intel Foundry Details Process Milestones and Future Innovation at VLSI Symposium. Intel, 16 June 2026. [intc.com](https://www.intel.com)

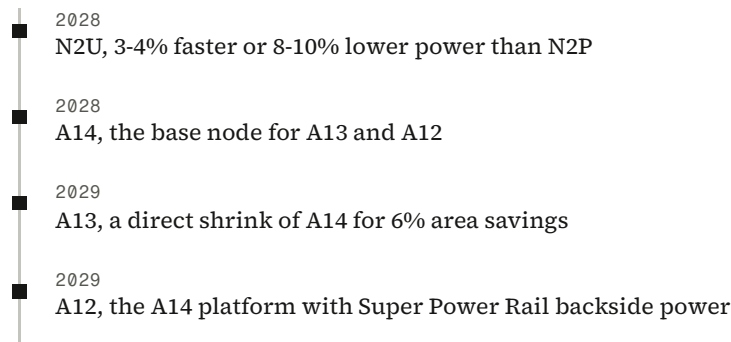
31 TSMC Unveils Next-Generation A14 Process at North America Technology Symposium. TSMC, 24 April 2025. pr.tsmc.com

32 TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC, 23 April 2026. pr.tsmc.com

Figure 08.2

TSMC plans four logic nodes beyond N2 for 2028 and 2029

TSMC's logic roadmap beyond N2, from its own announcements



Source: TSMC, 2026 North America Technology Symposium [32]

CFET and what comes after

A basic logic circuit needs two transistors that switch on opposite signals, and in production chips the two sit side by side. Complementary field-effect transistors, or CFETs, stack the two on top of each other³³. The research institute imec sees them as an attractive design for logic nodes beyond 1 nm³³.

04

The wiring above the transistors

Wiring the transistors together is called the back end of line, and it has become as hard to make as the transistor. Copper, the usual wiring metal, seeps into the insulator around it, so every wire needs a barrier, a liner and a cap³⁴. As the most critical wiring levels drop below a 20 nm pitch, those extra layers take a large share of the wire's width³⁴. Pitch is the distance from the center of one wire to the center of the next. Two metals are moving into those narrow levels.

- **Ruthenium** shows promise for use without a barrier, which would keep the wire's resistance low³⁴. imec has demonstrated ruthenium lines at a 16 nm pitch³⁵.
- **Molybdenum** in a thin film has up to 30 percent lower resistivity than tungsten, the metal it is replacing in contacts³⁶. It needs no barrier either, so chipmakers are putting it into some contacts and local wiring layers³⁶.

32 TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC, 23 April 2026. pr.tsmc.com

33 CFET (complementary FET). Imec, 16 June 2022. imec-int.com

34 Semi-damascene metallization. Imec, 31 October 2024. imec-int.com

35 16nm Ru lines using semi-damascene integration approach. Imec, 3 June 2025. imec-int.com

36 Molybdenum's Role in Ultra-Fast Computing: The Metal Behind the Speed. Entegris, 18 May 2026. blog.entegris.com

05

What foundries do and how a fab runs

A foundry makes chips designed by other companies, running all their designs on the same tools. TSMC and UMC, both based in Taiwan, make chips only for other companies. TSMC, founded in 1987, pioneered this pure-play model³⁷.

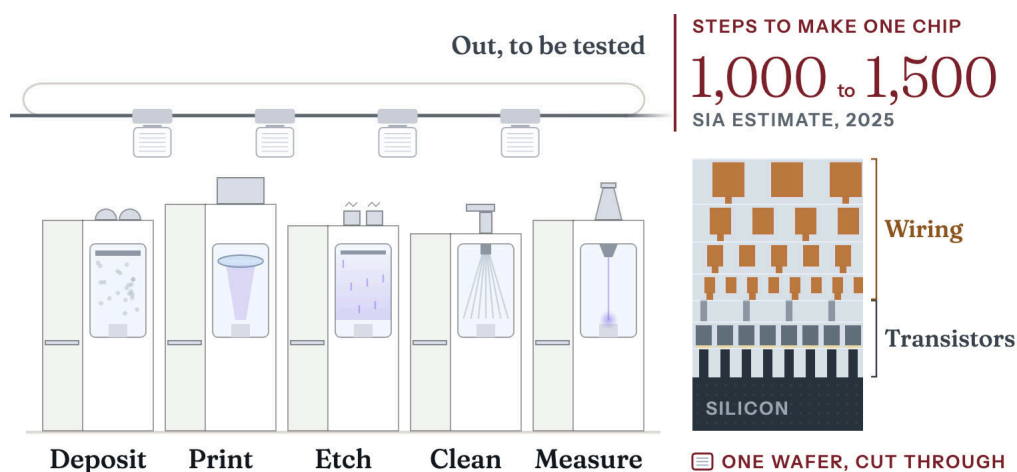
Inside a fab, a chip is built up in layers, and a similar loop of steps repeats for each one. Wafers travel in batches, called lots, inside a sealed pod called a FOUP, short for front-opening unified pod. Entegris, a US maker of these pods, offers a standard version that holds 25 wafers³⁸. An overhead track carries the pod from tool to tool.

At each tool a robot lifts one wafer out and the tool does its one job, such as depositing a film, printing a pattern, etching it, cleaning it or measuring it. Then the robot puts the wafer back, and the pod moves on to the next tool, often across the building. When a layer is finished, the loop starts again with the next one.

Turning silicon into a finished, packaged chip takes 1,000 to 1,500 steps, depending on how complex the chip is, the Semiconductor Industry Association said in 2025³⁹. In 2021 the association put the time to make a finished wafer at about 12 weeks on average, and up to 14 to 20 weeks for advanced processes⁴⁰. The pod keeps the wafer clean for all of that time, because the wafer never meets the room's air.

Figure 08.3 · Explainer, 20 seconds

How a fab builds a chip, layer by layer



1. **The fab.** Sealed pods carry wafers from tool to tool on a track near the ceiling.
2. **Deposit.** The first tool lays a thin film on the wafer.
3. **Print.** The next prints a pattern on it with light.

³⁷ TSMC, company profile page. TSMC, accessed 9 September 2026. [tsmc.com](https://www.tsmc.com)

³⁸ A300 FOUPs: Front opening unified pod platform with super microenvironment... Entegris, 2021. [entegris.com](https://www.entegris.com)

³⁹ Testimony of David Isaacs, Semiconductor Industry Association, hearing on... U.S. Senate Committee on Finance, 14 May 2025, p. 2. [finance.senate.gov](https://www.finance.senate.gov)

⁴⁰ Chipmakers Are Ramping Up Production to Address Semiconductor Shortage. Here's... Semiconductor Industry Association, 26 February 2021. [semiconductors.org](https://www.semiconductors.org)

4. **Etch.** An etch tool cuts the pattern into the film.
5. **Clean, measure.** The wafer is cleaned, then measured to check the layer came out right.
6. **Next layer.** Then the loop starts again for the next layer. The transistors come first, then the wiring above them.
7. **Finished.** Making one chip takes 1,000 to 1,500 steps, the Semiconductor Industry Association estimated in 2025.

Note: Simplified. A real fab has many tools of each kind, spread across the building, and a chip has far more layers than the seven shown. The layers are drawn far thicker than they are.

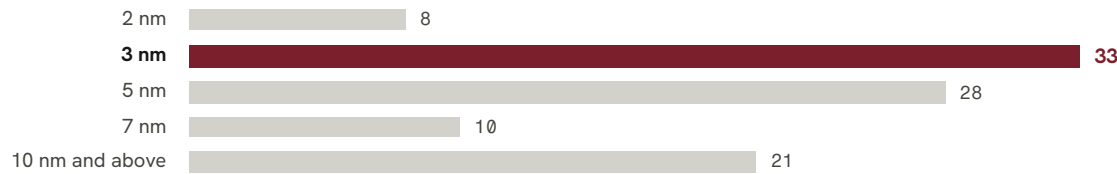
Each tool is set by a recipe, the list of gases, temperatures and times for one step. A foundry offers every customer the same list of recipes, so every design in the building can run on the same shared tools. The tools run day and night, because an idle tool earns nothing. The finished wafer is tested (see Test and assembly), then cut and packaged.

Chips at 7 nm and below, meaning the newest processes, were 79 percent of TSMC's wafer revenue in the third quarter of 2026⁴¹. That share split into 33 percent at 3 nm, 28 at 5 nm, 10 at 7 nm and 8 at 2 nm⁴¹. TSMC's revenue for the quarter was \$46.72 billion, at a 66.4 percent gross margin⁴¹.

Figure 08.4

3 nm led TSMC's wafer revenue in third-quarter 2026, at 33 percent

TSMC wafer revenue by node, 3Q26 % of wafer revenue



Source: TSMC 3Q26 results, filed with the SEC [41]

Intel and Samsung design and sell their own chips and rent out capacity too. Renting out capacity is harder for them, because customers dislike handing their designs to a competitor and each company's own products take its best capacity. Intel Foundry reported \$5.8 billion of segment revenue in the second quarter of 2026 and an operating loss of \$2.089 billion⁴². Only \$293 million of that revenue came from outside customers⁹.

06

The cost and capacity of the newest fabs

A new leading-edge fab costs tens of billions of dollars. In 2023 the Boston Consulting Group (BCG) estimated that a new fab for chips at 2 nm and below, completed in 2026, would cost \$35 to \$43 billion to build, equip and run over ten years¹⁰. Building and

⁹ Intel, quarterly report on Form 10-Q for the quarter ended 27 June 2026. U.S. Securities and Exchange Commission, 24 July 2026. sec.gov

¹⁰ Navigating the Costly Economics of Chip Making. Boston Consulting Group, 28 September 2023. bcg.com

⁴¹ TSMC Reports Third-Quarter EPS of NT\$29.43. U.S. Securities and Exchange Commission, 15 October 2026. sec.gov

⁴² Intel Reports Second-Quarter 2026 Financial Results. Intel, 23 July 2026. intel.com

equipping alone takes as much as \$20 to \$25 billion of capital for a leading-edge fab, the Semiconductor Industry Association (SIA) told the US Senate in March 2026¹⁷.

Most of TSMC's capacity is in its six GIGAFABs. Together, the plants TSMC and its subsidiaries run had capacity for more than 17 million wafers a year in 2025, counted as if each were the standard 12-inch size⁸. The six largest plants had a combined capacity of more than 13 million⁷. The other plants are five smaller fabs in Taiwan, two in China, two in the United States and one in Japan⁸. In July 2026 TSMC announced another \$100 billion for four more fabs at 2 nm or below, taking its planned investment in Arizona to \$265 billion across 12 facilities⁴.

In 2025 the biggest AI chip designers used most of the world's supply of two inputs but only a small share of its advanced chipmaking. Epoch AI estimated that the four largest used around 90 percent of the world's CoWoS packaging capacity and HBM memory supply⁴³. CoWoS is TSMC's packaging for AI chips, and HBM is the stacked memory that sits beside them. The same four used only 12 percent of advanced logic production⁴³. See Advanced packaging.

AI accelerators have usually trailed the leading edge. A die as large as theirs is more likely to hold a defect⁴⁴. So the share of dies that work, called the yield, gets high enough only once a process has run long enough to cut its defect rate.

Nvidia's Blackwell is made on an older TSMC process than AMD's MI455X. Epoch AI estimated in December 2025 that a 300 mm wafer on Blackwell's 4NP process costs \$17,000¹¹. AMD's MI455X, launched on 23 July 2026, is made on TSMC's 2 nm and 3 nm processes⁴⁵. It spreads its compute across eight separate dies⁴⁶.

07

TSMC, Intel, Samsung, SMIC and Rapidus

TSMC, Intel and Samsung build gate-all-around nodes with extreme ultraviolet (EUV) lithography. China's SMIC builds 7 nm-class nodes without it¹⁹. SemiAnalysis reported in September 2026 that Intel's Panther Lake, Samsung's Exynos 2600 and Apple's A20 Pro, which is made on TSMC's N2, all use gate-all-around transistors⁴⁷.

In August 2025 Intel called itself the only semiconductor company that both develops and manufactures leading-edge logic chips in the United States²⁰. That month the US government agreed to buy 433.3 million newly issued Intel shares at \$20.47 each, or \$8.9 billion in all, for a 9.9 percent stake²⁰. The stake is passive, with no board seat²⁰. The deal also gave the government a five-year warrant to buy a further 5 percent of

4 TSMC Announces Additional \$100 Billion Investment In Arizona. City of Phoenix, 16 July 2026. phoenix.gov

7 GIGAFAB® Facilities. TSMC, accessed 9 September 2026. tsmc.com

8 Fab Capacity. TSMC, accessed 9 September 2026. tsmc.com

11 NVIDIA's B200 costs around \$6,400 to produce. Epoch AI, 10 December 2025. epoch.ai

17 Testimony of the Semiconductor Industry Association (SIA) before the Senate... U.S. Senate Committee on Environment and Public Works, 4 March 2026, p. 3. epw.senate.gov

19 Is SMIC N+3's Metal Pitch Smaller than Intel 18A's? SemiAnalysis, 14 June 2026. newsletter.semianalysis.com

20 Intel and Trump Administration Reach Historic Agreement to Accelerate American... Intel, 22 August 2025. intc.com

43 Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip... Epoch AI, 12 March 2026. epoch.ai

44 Behrooz Parhami, Dependable Computing: A Multilevel Approach, part 2. University of California, Santa Barbara, 11 October 2020, p. 8. web.ece.ucsb.edu

45 AMD Instinct™ MI455X GPUs. AMD, accessed 9 September 2026. amd.com

46 AMD Instinct MI455X GPU. AMD, 20 July 2026. amd.com

47 Intel Panther Lake Teardown. SemiAnalysis, 26 September 2026. newsletter.semianalysis.com

Intel at \$20 a share²⁰. It can use the warrant only if Intel's ownership of its foundry business falls below 51 percent²⁰.

In 2026 Intel began high-volume manufacturing of some of its Panther Lake processors using ASML's High-NA extreme ultraviolet scanners⁴². But it is building fewer fabs than it planned. In July 2025 Intel said it would no longer go ahead with planned projects in Germany and Poland and would slow construction in Ohio⁴⁸.

In December 2024 the US Commerce Department awarded Samsung up to \$4.745 billion of CHIPS Act funding, to support more than \$37 billion of planned investment in Central Texas⁴⁹. That plan covers two new leading-edge logic fabs and a research fab in Taylor, and an expansion of Samsung's existing plant in Austin⁴⁹.

China's SMIC has the factories without the know-how for the newest transistors. Its revenue rose 16.2 percent to \$9.327 billion in 2025, at a 21 percent gross margin¹⁵. Its lines ran 93.5 percent full, on monthly capacity above a million wafers counted in the smaller 8-inch size¹⁵.

A node's name, such as 7 nm, does not measure any feature on the chip. SMIC's N+3, its third-generation 7 nm process, sets its narrowest wires 32.5 nm apart, tighter than the 36 nm in Intel's Panther Lake chips on 18A¹⁹. But the 18A process itself allows wires 32 nm apart¹⁹. SemiAnalysis called the comparison an incomplete, cherry-picked metric¹⁹. N+3 packs 113.4 million transistors per square millimeter, against 107.7 for TSMC's N6¹⁹.

Two research groups disagree about where Huawei's Ascend AI chips are made. Georgetown University's Center for Security and Emerging Technology (CSET) reported in June 2024 that the Ascend 910B was believed to be made on SMIC's N+2 process⁵⁰. But the research firm SemiAnalysis judged in April 2025 that most Ascend 910B and 910C chips were made on TSMC's 7 nm process⁵¹. It said Huawei got around the sanctions that barred it from TSMC by buying about \$500 million of 7 nm wafers through another company, Sophgo⁵¹.

IBM shows the opposite split. Its 2 nm technology yields no chips until Rapidus, a state-backed newcomer in Japan, finishes a factory to run it. The two firms agreed in December 2022 to develop that technology further for production at Rapidus's plant in Japan⁵².

In July 2025 Rapidus said it had started making 2 nm prototypes at the plant, in Chitose, Hokkaido, and would begin mass production in 2027⁵³. In February 2026 it raised 267.6 billion yen from the Japanese government and 32 companies to reach 2 nm

15 SMIC Announces 2025 Annual Results. SMIC, 26 March 2026. smics.com

19 Is SMIC N+3's Metal Pitch Smaller than Intel 18A's? SemiAnalysis, 14 June 2026. newsletter.semianalysis.com

20 Intel and Trump Administration Reach Historic Agreement to Accelerate American... Intel, 22 August 2025. intel.com

42 Intel Reports Second-Quarter 2026 Financial Results. Intel, 23 July 2026. intel.com

48 Intel Reports Second-Quarter 2025 Financial Results. Intel, 24 July 2025. intel.com

49 Biden-Harris Administration Announces CHIPS Incentives Award with Samsung... NIST, 20 December 2024. nist.gov

50 Pushing the Limits: Huawei's AI Chip Tests U.S. Export Controls. Center for Security and Emerging Technology, 17 June 2024. cset.georgetown.edu

51 Huawei AI CloudMatrix 384. SemiAnalysis, 16 April 2025. newsletter.semianalysis.com

52 IBM and Rapidus Form Strategic Partnership to Build Advanced Semiconductor... Rapidus, 13 December 2022. rapidus.inc

53 Rapidus Achieves Significant Milestone at its State-of-the-Art Foundry with... Rapidus, 18 July 2025. rapidus.inc

mass production by 2027¹⁶. By June 2026 Rapidus had raised 424.95 billion yen in equity⁵⁴.

08

Why leading-edge chipmaking is so concentrated

A firm that wants to make the newest chips has to develop its own process, because TSMC, Intel and Samsung do not sell their leading-edge process flows. A process flow sets the steps, their order and the tools for each. In September 2024 the United States began requiring a license to share the know-how for building gate-all-around transistors, except with countries that impose matching controls¹.

China has money for chipmaking but cannot buy EUV scanners. It launched its third National Integrated Circuit Fund in May 2024 with 344 billion yuan, about \$47 billion⁵⁵. China's 7 nm chips have been made on deep-ultraviolet machines, a generation behind EUV². China had stockpiled those machines from ASML, the Dutch scanner maker, before export restrictions took effect². SMIC gets fine features out of them by building its tightest layers in several patterning steps (see figure 04.2)¹⁹.

In July 2026 Reuters reported that a Shanghai state firm had begun making home-grown immersion deep-ultraviolet scanners⁵⁶. Reuters's own source said the firm's machine still needed testing and was far from matching ASML's models⁵⁶.

Domestic EUV is further off. China has announced \$43 billion to develop it². In September 2025 the Center for Strategic and International Studies (CSIS) judged that EUV remains firmly out of reach despite massive state investment². See Lithography.

The factories are concentrated too. In 2022 South Korea and Taiwan held almost all of the world's logic capacity below 10 nm, and the United States had almost none⁵⁷. Taiwan alone held 69 percent⁵. In May 2024 SIA and BCG projected that the US share of that capacity would reach 28 percent by 2032⁵.

China leads the world in capacity for logic chips made at 28 nm or older, but little of its capacity is advanced⁵⁸. Most of the world's wafers come off such older lines, which make power devices, analog chips and microcontrollers. Across all nodes, old and new, the industry association SEMI forecast in June 2024 that China would have installed capacity of 10.1 million wafers a month in 2025, the most of any region⁵⁹. It forecast 5.8 million for Taiwan, out of a world total of 33.7 million, all counted in the 8-inch size⁵⁹.

1 Commerce Control List Additions and Revisions; Implementation of Controls on... Federal Register, 6 September 2024. [federalregister.gov](https://www.federalregister.gov)

2 Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements. Center for Strategic and International Studies, 24 September 2025. [csis.org](https://www.csis.org)

5 Emerging Resilience in the Semiconductor Supply Chain. Boston Consulting Group and Semiconductor Industry..., May 2024, p. 14. [semiconductors.org](https://www.semiconductors.org)

16 Rapidus Secures 267.6 Billion Yen in Funding from Japan Government and Private... Rapidus, 27 February 2026. rapidus.inc

19 Is SMIC N+3's Metal Pitch Smaller than Intel 18A's? SemiAnalysis, 14 June 2026. newsletter.semianalysis.com

54 Rapidus Completes 150 Billion Yen Funding Round from Japan Government. Rapidus, 5 June 2026. rapidus.inc

55 China launches \$47bn chip fund to counter U.S. restrictions. Nikkei Asia, 27 May 2024. asia.nikkei.com

56 China starts production of home-grown immersion DUV chipmaking tools, source... Reuters, 28 July 2026. reuters.com

57 Emerging Resilience in the Semiconductor Supply Chain. Boston Consulting Group and Semiconductor Industry..., May 2024, p. 13. [semiconductors.org](https://www.semiconductors.org)

58 Emerging Resilience in the Semiconductor Supply Chain. Boston Consulting Group and Semiconductor Industry..., May 2024, p. 30. [semiconductors.org](https://www.semiconductors.org)

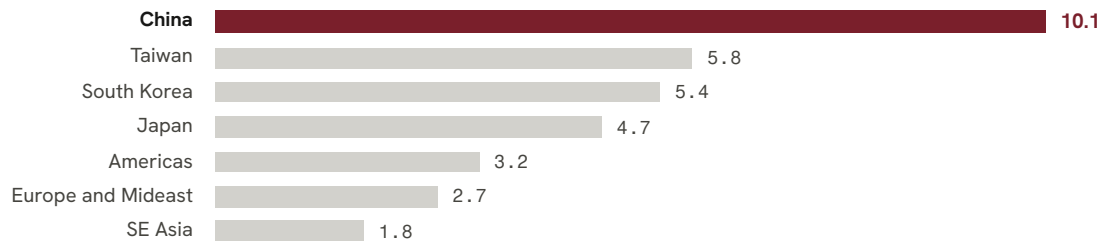
59 Global Semiconductor Fab Capacity Projected to Expand 6% in 2024 and 7% in... SEMI, 18 June 2024. semi.org

In the third-quarter 2026 update of its World Fab Forecast, SEMI projected that China would keep the largest installed capacity in 2026 and 2027³.

Figure 08.5

China led SEMI's 2025 capacity forecast at 10.1 million 8-inch-equivalent wafers monthly

SEMI's June 2024 forecast of installed wafer fab capacity by region in 2025, all nodes million 8-inch-equivalent wafers per month



Source: SEMI World Fab Forecast, June 2024 [59]

Chip production in Taiwan faces three risks:

- **Seismic.** Taiwan sits on an active plate boundary, and after an earthquake in January 2025 TSMC had to scrap some wafers in process⁶⁰.
- **Power.** TSMC says power outages, dips or surges caused by problems at its electricity supplier have at times interrupted its operations⁶¹.
- **Political.** In December 2025 SemiAnalysis put Taiwan's share of the world's advanced-node capacity at over 90 percent, though it did not say which node sizes count as advanced¹⁸. So a blockade or conflict would cut most of that output off from the world market at once. See Who Controls the Chain.

Building capacity outside Taiwan is slow, and TSMC has yet to build a gigafab anywhere else⁸. SemiAnalysis wrote in December 2025 that a foundry needs highly skilled engineers to get the most working chips from each wafer¹⁸. It judged that finding enough workers remained a major challenge for TSMC in Arizona¹⁸.

Five questions to answer from memory

1. What does a chip factory do? see How it works
2. Why do the newest transistors wrap the gate around the channel? see How it works
3. What two things does a chipmaker need to make the newest chips? see How it works
4. What is a foundry, and which is the biggest? see Capacity and cost
5. How does China's SMIC make advanced chips without EUV? see The chokepoint

³ World Fab Forecast. SEMI, accessed 9 September 2026. [semi.org](https://www.semi.org)

⁸ Fab Capacity. TSMC, accessed 9 September 2026. [tsmc.com](https://www.tsmc.com)

¹⁸ TSMC Overseas Fabs – A Success? SemiAnalysis, 1 December 2025. newsletter.semianalysis.com

⁵⁹ Global Semiconductor Fab Capacity Projected to Expand 6% in 2024 and 7% in... SEMI, 18 June 2024. [semi.org](https://www.semi.org)

⁶⁰ TSMC January 2025 Revenue Report and the Statement on the Impact of Earthquake. TSMC, 10 February 2025. pr.tsmc.com

⁶¹ TSMC, annual report on Form 20-F for the fiscal year ended 31 December 2025. U.S. Securities and Exchange Commission, 16 April 2026. [sec.gov](https://www.sec.gov)

Five things to remember

- The newest chips need both the know-how to build the newest transistors and factories that cost tens of billions of dollars, and in 2026 only TSMC, Intel and Samsung had both.
- The newest transistors wrap the gate around all four sides of the channel to cut the current that leaks when the switch is off.
- A foundry makes chips for other companies, because no chip company sells enough of one product to fill a fab alone.
- All six of TSMC's largest plants are in Taiwan, which held 69 percent of the world's logic capacity below 10 nm in 2022.
- China's SMIC makes 7 nm-class chips without EUV by building its tightest layers in several patterning steps.

Sources (61)

1. A Commerce Control List Additions and Revisions; Implementation of Controls on Advanced Technologies Consistent With Controls Implemented by International Partners. Federal Register (Commerce Department; Industry and Security Bureau) · 6 September 2024
www.federalregister.gov/documents/2024/09/06/2024-19633/commerce-control-list-additions-and-revisions-implementation-of-controls-on-advanced-technologies
2. A Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements. Center for Strategic and International Studies · 24 September 2025
www.csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chinese-lithography
3. A World Fab Forecast. SEMI · Accessed 9 September 2026
www.semi.org/en/products-services/market-data/world-fab-forecast
4. A TSMC Announces Additional \$100 Billion Investment In Arizona. City of Phoenix · 16 July 2026
www.phoenix.gov/newsroom/ced-news/tsmc-announces-additional--100-billion-investment-in-arizona.html
5. A Emerging Resilience in the Semiconductor Supply Chain. Boston Consulting Group and Semiconductor Industry Association · May 2024 · p. 14
www.semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconductor-Supply-Chain.pdf#page=14
6. A NVIDIA Blackwell Architecture. Nvidia · 18 December 2025
www.nvidia.com/en-us/data-center/technologies/blackwell-architecture/
7. A GIGAFAB® Facilities. TSMC · Accessed 9 September 2026
www.tsmc.com/english/dedicatedFoundry/manufacturing/gigafab
8. A Fab Capacity. TSMC · Accessed 9 September 2026
www.tsmc.com/english/dedicatedFoundry/manufacturing/fab_capacity
9. A Intel, quarterly report on Form 10-Q for the quarter ended 27 June 2026. U.S. Securities and Exchange Commission (filing by Intel) · 24 July 2026
www.sec.gov/Archives/edgar/data/50863/000005086326000157/intc-20260627.htm
10. A Navigating the Costly Economics of Chip Making. Boston Consulting Group · 28 September 2023
www.bcg.com/publications/2023/navigating-the-semiconductor-manufacturing-costs
11. A NVIDIA's B200 costs around \$6,400 to produce. Epoch AI · 10 December 2025
epoch.ai/data-insights/b200-cost-breakdown
12. A 2nm Technology. TSMC · Accessed 9 September 2026
www.tsmc.com/english/dedicatedFoundry/technology/logic/l_2nm
13. A Intel 18A: See Our Biggest Process Innovation. Intel · Accessed 18 October 2026
www.intel.com/content/www/us/en/foundry/process/18a.html
14. A Samsung Begins Chip Production Using 3nm Process Technology With GAA Architecture. Samsung Global Newsroom · 30 June 2022
news.samsung.com/global/samsung-begins-chip-production-using-3nm-process-technology-with-gaa-architecture
15. A SMIC Announces 2025 Annual Results. SMIC · 26 March 2026
www.smics.com/en/site/news_read/7951
16. A Rapidus Secures 267.6 Billion Yen in Funding from Japan Government and Private Sector Companies. Rapidus · 27 February 2026
www.rapidus.inc/en/news_topics/information/rapidus-secures-267-6-billion-yen-in-funding-from-japan-government-and-private-sector-companies/
17. A Testimony of the Semiconductor Industry Association (SIA) before the Senate Committee on Environment & Public Works. U.S. Senate Committee on Environment and Public Works · 4 March 2026 · p. 3
www.epw.senate.gov/public/_cache/files/a/c/ac4552ff-551b-40d5-bea6-19dd17a1cfea/1F7BCD91016CBE352434701BE58395874BEA6A892A23ABEE1D7214EC924EC0EB.03-04-2026-isaacs-testimony.pdf#page=3

18. B **TSMC Overseas Fabs – A Success?**. SemiAnalysis · 1 December 2025
newsletter.semianalysis.com/p/tsmc-overseas-fabs-a-success
19. B **Is SMIC N+3's Metal Pitch Smaller than Intel 18A's?**. SemiAnalysis · 14 June 2026
newsletter.semianalysis.com/p/steel-smic-n3-teardown
20. A **Intel and Trump Administration Reach Historic Agreement to Accelerate American Technology and Manufacturing Leadership**. Intel · 22 August 2025
www.intel.com/news-events/press-releases/detail/1748/intel-and-trump-administration-reach-historic-agreement-to
21. A **Intel's Transistor Technology Breakthrough Represents Biggest Change to Computer Chips in 40 Years**. Intel · 27 January 2007
www.intel.com/pressroom/archive/releases/2007/20070128comp.htm
22. A **Entering the nanosheet transistor era**. imec · 11 February 2022
www.imec-int.com/en/articles/entering-nanosheet-transistor-era-0
23. A **Development of SiGe Indentation Process Control for Gate-All-Around FET Technology Enablement**. arXiv · 12 January 2022
arxiv.org/abs/2201.04725
24. A **Applied Materials Unveils Next-Gen Chipmaking Products to Supercharge AI Performance**. Applied Materials · 7 October 2025
ir.appliedmaterials.com/news-releases/news-release-details/applied-materials-unveils-next-gen-chipmaking-products
25. A **Applied Materials Technologies Enable 2D Scaling with EUV and 3D Gate-All-Around Transistors**. Applied Materials · 21 April 2022
ir.appliedmaterials.com/news-releases/news-release-details/applied-materials-technologies-enable-2d-scaling-euv-and-3d-gate
26. A **HPC Platform – Advanced Technologies**. TSMC · Accessed 9 September 2026
www.tsmc.com/english/dedicatedFoundry/technology/platform_HPC_tech_advancedTech
27. B **The Future of the Transistor**. SemiAnalysis · 21 February 2023
newsletter.semianalysis.com/p/the-future-of-the-transistor
28. B **Clash of the Foundries: Gate All Around + Backside Power at 2nm**. SemiAnalysis · 1 October 2024
newsletter.semianalysis.com/p/clash-of-the-foundries
29. A **A 38.1Mb/mm² SRAM in a 2nm-CMOS-Nanosheet Technology for High-Density and Energy-Efficient Compute**. TSMC · 2025
research.tsmc.com/page/memory/4.html
30. A **Intel Foundry Details Process Milestones and Future Innovation at VLSI Symposium**. Intel · 16 June 2026
www.intel.com/news-events/press-releases/detail/1772/intel-foundry-details-process-milestones-and-future
31. A **TSMC Unveils Next-Generation A14 Process at North America Technology Symposium**. TSMC · 24 April 2025
pr.tsmc.com/english/news/3228
32. A **TSMC Debuts A13 Technology at 2026 North America Technology Symposium**. TSMC · 23 April 2026
pr.tsmc.com/english/news/3302
33. A **CFET (complementary FET)**. imec · 16 June 2022
www.imec-int.com/en/articles/imec-puts-complementary-fet-cfet-logic-technology-roadmap
34. A **Semi-damascene metallization**. imec · 31 October 2024
www.imec-int.com/en/articles/semi-damascene-metallization-inflection-point-back-end-line-processing
35. A **16nm Ru lines using semi-damascene integration approach**. imec · 3 June 2025
www.imec-int.com/en/press/imec-demonstrates-16nm-pitch-ru-lines-record-low-resistance-obtained-using-semi-damascene
36. A **Molybdenum's Role in Ultra-Fast Computing: The Metal Behind the Speed**. Entegris · 18 May 2026
blog.entegris.com/molybdenums-role-in-ultra-fast-computing-the-metal-behind-the-speed
37. A **TSMC, company profile page**. TSMC · Accessed 9 September 2026
www.tsmc.com/english/aboutTSMC/company_profile
38. A **A300 FOUps: Front opening unified pod platform with super microenvironment control**. Entegris · 2021
www.entegris.com/content/dam/product-assets/a300foups/datasheet-a300foups.pdf
39. A **Testimony of David Isaacs, Semiconductor Industry Association, hearing on “Trade in Critical Supply Chains”**. U.S. Senate Committee on Finance · 14 May 2025 · p. 2
www.finance.senate.gov/download/051425-isaacs-testimony&download=1#page=2
40. A **Chipmakers Are Ramping Up Production to Address Semiconductor Shortage. Here's Why that Takes Time**. Semiconductor Industry Association · 26 February 2021
www.semiconductors.org/chipmakers-are-ramping-up-production-to-address-semiconductor-shortage-heres-why-that-takes-time/
41. A **TSMC Reports Third Quarter EPS of NT\$29.43**. U.S. Securities and Exchange Commission (filing by TSMC) · 15 October 2026
www.sec.gov/Archives/edgar/data/1046179/000104617926000726/a3q26e_withguidancexfinal.htm
42. A **Intel Reports Second-Quarter 2026 Financial Results**. Intel · 23 July 2026
www.intel.com/news-events/press-releases/detail/1776/intel-reports-second-quarter-2026-financial-results
43. A **Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip production in 2025**. Epoch AI · 12 March 2026
epoch.ai/data-insights/ai-chip-supply-chain-constraints
44. A **Behrooz Parhami, Dependable Computing: A Multilevel Approach, part 2**. University of California, Santa Barbara · 11 October 2020 · p. 8
web.ece.ucsb.edu/~parhami/docs_folder/f33-book-dep-comp-pt2.pdf#page=8
45. A **AMD Instinct™ MI455X GPUs**. AMD · Accessed 9 September 2026
www.amd.com/en/products/accelerators/instinct/mi400/mi455x.html

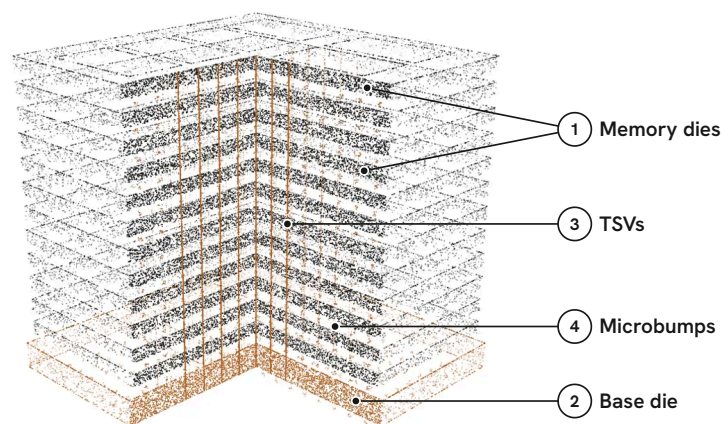
46. A **AMD Instinct MI455X GPU**. AMD · 20 July 2026
www.amd.com/content/dam/amd/en/documents/products/accelerators/instinct/amd-instinct-mi455x_brochure.pdf
47. B **Intel Panther Lake Teardown**. SemiAnalysis · 26 September 2026
newsletter.semianalysis.com/p/intel-panther-lake-teardown
48. A **Intel Reports Second-Quarter 2025 Financial Results**. Intel · 24 July 2025
www.intc.com/news-events/press-releases/detail/1745/intel-reports-second-quarter-2025-financial-results
49. A **Biden-Harris Administration Announces CHIPS Incentives Award with Samsung Electronics to Solidify U.S. Leadership in Leading-Edge Semiconductor Production**. NIST · 20 December 2024
www.nist.gov/news-events/news/2024/12/biden-harris-administration-announces-chips-incentives-award-samsung
50. A **Pushing the Limits: Huawei's AI Chip Tests U.S. Export Controls**. Center for Security and Emerging Technology (CSET) · 17 June 2024
cset.georgetown.edu/publication/pushing-the-limits-huaweis-ai-chip-tests-u-s-export-controls/
51. B **Huawei AI CloudMatrix 384**. SemiAnalysis · 16 April 2025
newsletter.semianalysis.com/p/huawei-ai-cloudmatrix-384-chinas-answer-to-nvidia-gb200-nvl72
52. A **IBM and Rapidus Form Strategic Partnership to Build Advanced Semiconductor Technology and Ecosystem in Japan**. Rapidus · 13 December 2022
www.rapidus.inc/en/news_topics/information/ibm-and-rapidus-form-strategic-partnership-to-build-advanced-semiconductor-technology-and-ecosystem-in-japan/
53. A **Rapidus Achieves Significant Milestone at its State-of-the-Art Foundry with Prototyping of Leading-Edge 2nm GAA Transistors**. Rapidus · 18 July 2025
www.rapidus.inc/en/news_topics/information/rapidus-achieves-significant-milestone-at-its-state-of-the-art-foundry-with-prototyping-of-leading-edge-2nm-gaa-transistors/
54. A **Rapidus Completes 150 Billion Yen Funding Round from Japan Government**. Rapidus · 5 June 2026
www.rapidus.inc/en/news_topics/information/20260605-2/
55. B **China launches \$47bn chip fund to counter U.S. restrictions**. Nikkei Asia · 27 May 2024
asia.nikkei.com/spotlight/supply-chain/china-launches-47bn-chip-fund-to-counter-u.s.-restrictions
56. B **China starts production of home-grown immersion DUV chipmaking tools, source says**. Reuters · 28 July 2026
www.reuters.com/world/china/china-starts-production-home-grown-immersion-duv-chipmaking-tools-source-2026-07-28/
57. A **Emerging Resilience in the Semiconductor Supply Chain**. Boston Consulting Group and Semiconductor Industry Association · May 2024 · p. 13
www.semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconductor-Supply-Chain.pdf#page=13
58. A **Emerging Resilience in the Semiconductor Supply Chain**. Boston Consulting Group and Semiconductor Industry Association · May 2024 · p. 30
www.semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconductor-Supply-Chain.pdf#page=30
59. A **Global Semiconductor Fab Capacity Projected to Expand 6% in 2024 and 7% in 2025, SEMI Reports**. SEMI · 18 June 2024
www.semi.org/en/news-media-press-releases/semi-press-releases/global-semiconductor-fab-capacity-projected-to-expand-6%25-in-2024-and-7%25-in-2025-semi-reports
60. A **TSMC January 2025 Revenue Report and the Statement on the Impact of Earthquake**. TSMC · 10 February 2025
pr.tsmc.com/english/news/3204
61. A **TSMC, annual report on Form 20-F for the fiscal year ended 31 December 2025**. U.S. Securities and Exchange Commission (filing by TSMC) · 16 April 2026
www.sec.gov/Archives/edgar/data/1046179/000162828026025362/tsm-20251231.htm



01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Memory and HBM

SK hynix, Samsung and Micron make nearly all high bandwidth memory (HBM), the stacked memory beside AI chips. SK hynix took 63.2 percent of HBM revenue in 2025.



Specimen 09 · Memory and HBM

A twelve-high HBM stack, pulled apart and cut open: a logic die at the base, shown in copper, and twelve memory dies above it. The finished part is 11 by 11 mm and 0.72 mm tall. Each memory die is ground to about 30 micrometers, thinner than a human hair. The footprint is to scale, but the heights are exaggerated about fifteen times.

Parts, as numbered on the drawing

- ① Memory dies: SK hynix (KR), Samsung (KR), Micron (US)
- ② Base die: SK hynix (KR) through HBM3E, TSMC (TW) for SK hynix's HBM4
- ③ TSVs (through-silicon vias): etched and filled with copper by the memory maker
- ④ Microbumps: joined by the memory maker, [see How a stack is built](#)

In plain terms

High bandwidth memory, or HBM, is where an AI chip keeps the numbers it is working on, and it is built to hand them over fast. A memory maker etches tiny holes into each memory wafer, fills them with copper and grinds the wafer until the copper shows through its back. It tests each of the wafer's chips and stacks up to sixteen good ones into a cube, with every layer wired to the ones below. The cube then sits beside the processor, the chip that does the calculating. Stacking is the hard part because each chip is ground thinner than a

human hair and the finished cube has to stay within a height limit of less than a millimeter. One chip that fails after stacking can scrap the whole cube. Only SK hynix, Samsung and Micron make HBM in volume. One US export rule covers HBM from all three, including the two based in South Korea.

In short

US-based Micron went from 5.8 percent of HBM revenue in 2024 to 23.1 percent in the first quarter of 2026, according to IDC figures in SK hynix's US prospectus¹. Over the same period, Samsung's share fell from 37.8 percent to 20.5 percent¹.

Since December 2024, a US license has been required, unless an exception applies, to export to China any HBM moving more than 2 GB per second per square millimeter of its area². The Institute for Progress reported in October 2025 that China's CXMT planned to produce HBM3 in 2026³. Even so, working from TrendForce's estimate of world HBM shipments, the institute projected that producers outside China would make 70 times as much HBM as China in 2026³. In June 2026 SemiAnalysis judged that CXMT was still struggling to stabilize supply of eight-high HBM3⁴.

An AI accelerator moves numbers from memory to its arithmetic units and back. The US export control office wrote in December 2024 that a processor cannot reach its full capabilities unless its memory capacity and bandwidth rise with its speed².

Chokepoint card		Memory and HBM
<div>Concentration</div> <div> Extreme</div> <div>Three or fewer firms could supply this stage today, or one firm holds more than half of it.</div>	<div>Substitutability</div> <div>Hard</div> <div>In June 2026 SemiAnalysis judged that CXMT, China's strongest DRAM maker, was still struggling to stabilize supply of eight-high HBM3⁴.</div>	<div>Price or market size</div> <div>About \$35 billion</div> <div>HBM market in 2025, Micron's December 2025 estimate⁵</div>
Who leads	<div>KR SK hynix</div> <div>KR Samsung</div> <div>US Micron</div>	<div>63.2 percent of HBM revenue in 2025¹</div> <div>19.3 percent of HBM revenue in 2025¹</div> <div>17.4 percent of HBM revenue in 2025¹</div>
Where it is made	<div>KR South Korea</div> <div>US United States</div> <div>TW Taiwan</div> <div>JP Japan</div> <div>SG Singapore</div>	<div>SK hynix in Cheongju and Icheon, Samsung in Pyeongtaek and Hwaseong</div> <div>Micron headquarters and R&D, and an SK hynix packaging plant under construction in Indiana</div> <div>Micron DRAM and HBM production</div> <div>Micron Hiroshima, 1-gamma DRAM</div> <div>Micron HBM advanced packaging plant, adding capacity from 2027</div>
Why substitution is slow	<div>SK hynix says only a few firms have the expertise and resources to design, make and package memory chips¹. It says HBM also needs advanced processes such as packaging with through-silicon vias (TSVs), the copper-filled holes that link the layers, and must pass customers' rigorous testing and approval¹.</div>	

1 SK hynix, prospectus on Form 424B4 dated 10 July 2026. U.S. Securities and Exchange Commission, 10 July 2026. sec.gov
2 Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... Federal Register, 5 December 2024. federalregister.gov
3 Should the US Sell Blackwell Chips to China? Institute for Progress, 25 October 2025. ifp.org
4 China's CXMT Is Set to Challenge DRAM Incumbents. SemiAnalysis, 23 June 2026. newsletter.semianalysis.com
5 Fiscal Q1 2026 Earnings Call Prepared Remarks. Micron Technology, 17 December 2025. s25.q4cdn.com

Where China stands

The Institute for Progress estimated in October 2025 that China would make virtually no HBM that year³. Huawei said in September 2025 that its Ascend 950 chips would use two HBM designs of its own, without saying who would manufacture the memory⁶.

Where the US stands

Micron is the only American HBM maker¹. As of October 2026, License Exception HBM lets US and allied exporters ship HBM below 3.3 GB per second per square millimeter without a license, including to China when the chip designer buys it directly and it goes straight to the packaging site⁷.

01

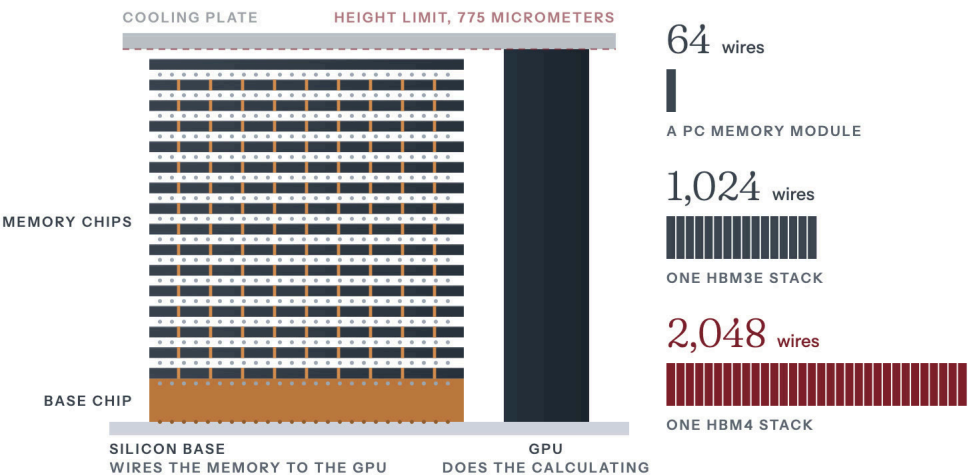
How HBM works and why AI needs it

Each layer in the cube is a DRAM chip, the ordinary kind of computer memory. Each layer is ground thin and bonded to the one below through tiny metal bumps called microbumps. The whole stack sits on a base die, a chip that manages it. The copper-filled holes are called through-silicon vias, or TSVs. They let a signal reach any layer without a wire running around the outside.

An HBM3E cube has a 1,024-bit interface, meaning it exchanges data with the processor over 1,024 wires at once⁸. That is sixteen times wider than a standard DDR5 memory module, the memory stick in a PC⁸. HBM4 doubles that to 2,048 wires⁹. Ordinary memory cannot be made that wide, because the pins would not fit on a circuit board. The stack can, since its wires run down through the TSVs and across a silicon interposer to the processor beside it, with no board in the way⁸. The interposer is a slice of silicon carrying fine wiring, set under both the memory and the processor (see Advanced packaging).

Figure 09.1 · Explainer, 21 seconds

Inside a memory stack



1 SK hynix, prospectus on Form 424B4 dated 10 July 2026. U.S. Securities and Exchange Commission, 10 July 2026. [sec.gov](#)

3 Should the US Sell Blackwell Chips to China? Institute for Progress, 25 October 2025. [ifp.org](#)

6 Groundbreaking SuperPoD Interconnect: Leading a New Paradigm for AI... Huawei, 18 September 2025. [huawei.com](#)

7 15 CFR 740.25 -- License Exception High Bandwidth Memory (HBM). Electronic Code of Federal Regulations, 5 December 2024. [ecfr.gov](#)

8 High-bandwidth memory (HBM). Micron Technology, accessed 9 September 2026. [micron.com](#)

9 JEDEC® and Industry Leaders Collaborate to Release JESD270-4 HBM4 Standard... JEDEC Solid State Technology Association, 16 April 2025. [jedec.org](#)

1. **Base chip.** A memory stack sits beside the GPU on a shared silicon base. It starts with a base chip, which controls the memory chips above it.
2. **Thin.** Each memory chip is ground to about 30 micrometers, thinner than a human hair.
3. **Stack.** Twelve chips are joined by dots of solder, and copper-filled holes run straight down through all but the top one.
4. **Height.** The stack has to fit under the cooling plate. Twelve chips reach 0.72 mm, the old limit. HBM4 raised the limit to 775 micrometers and fits up to sixteen chips.
5. **Width.** An HBM3E stack talks to the processor over 1,024 wires at once, sixteen times as many as a PC memory module. HBM4 doubles that to 2,048.

Note: Simplified cross-section. Heights follow the HBM height limits of 720 and 775 micrometers and are drawn to one vertical scale. Widths are not to scale.

A chip needs the width most when it answers a prompt. Training reuses each stored number across a huge multiplication, so a chip can fetch little and compute a lot. But to generate one word of an answer, the chip reads the whole model from memory, plus the whole record of the conversation so far. Then it does a little arithmetic and waits for the next read. That record grows with the length of the conversation and the number of users served at once. So memory size and speed usually set how many people one chip can serve.

02

HBM3E and HBM4 compared

Generation	Interface	Bandwidth per stack	Capacity per stack
HBM3E	1,024-bit, 16 channels (32 pseudo-channels)	over 1.2 TB/s	24 GB (8 chips), 36 GB (12 chips)
HBM4	2,048-bit, 32 channels	over 2.0 TB/s, up to 3.3 TB/s	up to 64 GB (16 chips, 32 Gb dies)

HBM3E

Micron's HBM3E comes in two sizes, 24 GB with eight chips stacked and 36 GB with twelve¹⁰.

HBM4

All three HBM makers run their HBM4 faster than the 8 Gb/s per pin in the industry standard. The standards body JEDEC published JESD270-4 in April 2025, setting the 2,048-bit interface and 2 TB/s per stack at 8 Gb/s per pin⁹. SK hynix says it was first to complete HBM4 development, in September 2025, at over 10 Gb/s per pin¹¹. Samsung says it began mass production and shipped the first commercial HBM4 in February 2026, at 11.7 Gb/s per pin, with a 4 nm logic base die¹². It gives that HBM4 a maximum of 3.3 TB/s per stack¹². Micron's parts run above 11 Gb/s for more than 2.8 TB/s per stack¹³. Micron says it began volume production of its 36 GB twelve-high HBM4 in

9 JEDEC® and Industry Leaders Collaborate to Release JESD270-4 HBM4 Standard... JEDEC Solid State Technology Association, 16 April 2025. [jedec.org](https://www.jedec.org)

10 Micron, HBM3E product page. Micron Technology, accessed 9 September 2026. [micron.com](https://www.micron.com)

11 SK hynix Completes World's First HBM4 Development and Readies Mass Production. SK hynix, 12 September 2025. news.skhynix.com

12 Samsung Ships Industry-First Commercial HBM4 With Ultimate Performance for AI... Samsung Global Newsroom, 12 February 2026. news.samsung.com

13 Micron, HBM4 product page. Micron Technology, accessed 9 September 2026. [micron.com](https://www.micron.com)

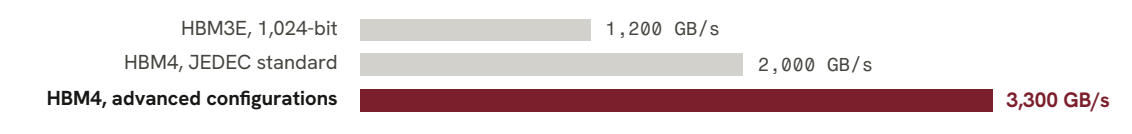
fiscal 2026 and expects to ramp volume of HBM4E, the next generation, in calendar 2027¹⁴.

Through HBM3E, SK hynix made its own base dies, the chips at the bottom of each stack¹⁵. For HBM4 it chose TSMC's advanced logic process, so the base die can hold more functions¹⁵. As a result, TSMC, which does not make HBM, makes the base die for SK hynix's HBM4.

Figure 09.2

As of April 2026, HBM4 reaches up to 3,300 GB/s per stack, against 2,000 in the JEDEC standard

Bandwidth per HBM stack



Source: Siemens EDA, HBM3E and HBM4 IC design guide, April 2026 [16]

03

How an HBM stack is built

- **Etch and thin.** Etch vertical holes, the through-silicon vias, into a memory wafer, fill them with copper, then grind the wafer from behind until the copper comes through.
- **Stack and join.** Makers join the chips through metal bumps by methods such as TC-NCF and MR-MUF¹⁷. In MR-MUF, short for mass reflow molded underfill, the chips are first connected through microbumps and stacked, and a liquid underfill is then injected to fill every gap at once and cured¹⁷. SK hynix uses its own version, Advanced MR-MUF, which stacks the chips, injects a liquid protective material between them and hardens it¹¹. SK hynix says the process controls warping and dissipates heat well¹¹. Samsung said in February 2024 that its twelve-high HBM3E uses TC-NCF, thermocompression with a thin non-conductive film between the chips¹⁸. Samsung expected TC-NCF to help limit warping as chips get thinner¹⁸.
- **Stay under the height limit.** The package specification for HBM4 raised the height allowed for a finished cube from 720 micrometers to 775, still under a millimeter¹⁷.

Hybrid bonding is the next step, but it is not ready. It would join the chips copper to copper and insulator to insulator, with no solder and no filler¹⁷. A tech note on SK hynix's newsroom gives about 20 micrometers as the typical spacing between microbumps, against less than 1 micrometer for hybrid bonds¹⁷. It says full-scale adoption in HBM is most likely at HBM4E or HBM5, where stacks are projected to pass twenty layers¹⁷. Taller stacks trap more heat, and removing it becomes a major

11 SK hynix Completes World's First HBM4 Development and Readies Mass Production. SK hynix, 12 September 2025. news.skhynix.com
14 Micron Technology, annual report on Form 10-K for the fiscal year ended 3... U.S. Securities and Exchange Commission, 9 October 2026. sec.gov
15 SK hynix Partners with TSMC to Strengthen HBM Technological Leadership. SK hynix, 19 April 2024. news.skhynix.com
16 HBM3e and HBM4: IC design guide for next-generation high bandwidth memory. Siemens Digital Industries Software, 24 April 2026. blogs.sw.siemens.com
17 [Tech Note] Hybrid Bonding: Evolving into a Foundational Technology for... SK hynix, 25 August 2026. news.skhynix.com
18 Samsung Develops Industry-First 36GB HBM3E 12H DRAM. Samsung Global Newsroom, 27 February 2024. news.samsung.com

challenge at 16 to 20 layers¹⁷. The same tech note says hybrid bonding manages that heat more efficiently¹⁷.

04

Who makes HBM

Three firms took more than 90 percent of the revenue from ordinary computer memory, or DRAM, in the first quarter of 2026, according to IDC figures in SK hynix's US prospectus¹. HBM comes from the same three, SK hynix, Samsung and Micron¹. No other company has both leading-edge DRAM and a stacking line of its own. SK hynix says only a few firms have the expertise and resources to design, make and package memory chips¹. It says HBM also needs advanced production processes, such as TSV packaging, and must pass the rigorous testing and approval processes its customers set¹.

SK hynix says it was the first company to mass-produce several generations of HBM, including HBM3 and HBM3E¹.

SK hynix and Micron are both adding HBM capacity. SK hynix broke ground in August 2026 on an advanced packaging plant in West Lafayette, Indiana, an investment of over \$4 billion¹⁹. Micron is modernizing and expanding its DRAM and HBM production capacity in Taiwan¹⁴. It has also broken ground on an HBM advanced packaging plant in Singapore to expand its packaging capacity from early 2027¹⁴.

SK hynix led HBM revenue in 2024, in 2025 and in the first quarter of 2026, and in that quarter Micron passed Samsung for second place. In 2024 SK hynix took 56.4 percent, Samsung 37.8 and Micron 5.8¹. In 2025 the three took 63.2, 19.3 and 17.4 percent¹. In the first quarter of 2026 they stood at 56.4, 20.5 and 23.1 percent, which put SK hynix back at its 2024 share¹. The split is public because SK hynix registered shares in the United States, and its US prospectus credits the research firm IDC¹.

Figure 09.3

SK hynix took 63.2 percent of global HBM revenue in 2025

Global HBM revenue by supplier, 2025



Source: SK hynix Form 424B4 prospectus, 10 July 2026, on IDC data [1]

¹ SK hynix, prospectus on Form 424B4 dated 10 July 2026. U.S. Securities and Exchange Commission, 10 July 2026. sec.gov

¹⁴ Micron Technology, annual report on Form 10-K for the fiscal year ended 3... U.S. Securities and Exchange Commission, 9 October 2026. sec.gov

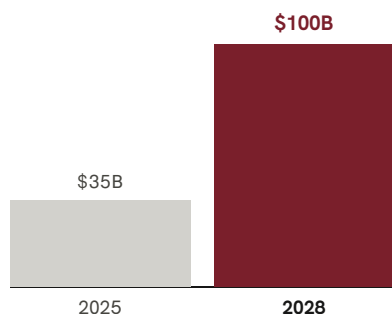
¹⁷ [Tech Note] Hybrid Bonding: Evolving into a Foundational Technology for... SK hynix, 25 August 2026. news.skhynix.com

¹⁹ SK hynix breaks ground on \$4 billion advanced packaging production facility in... Purdue University, 27 August 2026. purdue.edu

Figure 09.4

Micron sees HBM reaching \$100 billion in 2028, from an estimated \$35 billion

HBM market, Micron's estimate for 2025 and forecast for 2028



Source: Micron prepared remarks, fiscal first quarter 2026, 17 December 2025 [5]

As HBM grows, memory makers have less factory capacity left for traditional DRAM. In December 2025 Micron put the HBM market at about \$35 billion in 2025 and forecast that it would reach around \$100 billion in 2028⁵. Micron says HBM needs more wafers than traditional DRAM, the kind used in PCs and phones, to make the same number of bits¹⁴. SK hynix says the industry's shift of production capacity to HBM has left traditional DRAM undersupplied¹. The shortage, it says, helped drive a significant price recovery for that DRAM from the third quarter of 2025¹.

05

HBM export controls and China's efforts

The leading accelerators made outside China use HBM from SK hynix, Samsung or Micron. A US export rule of 5 December 2024 covers every HBM stack that was in production when it was published, including stacks made outside the United States². China's strongest DRAM maker, CXMT, was still struggling to make HBM in steady supply by June 2026. That month SemiAnalysis judged that CXMT had yet to stabilize supply of eight-high HBM3 and faced even greater challenges at twelve-high⁴.

Nvidia's GB300 NVL72 rack carries 20 TB of HBM3E at up to 576 TB/s²⁰. Each Nvidia Rubin GPU carries up to 288 GB of HBM4 at up to 22 TB/s²¹. AMD's MI355X carries 288 GB of HBM3E at 8 TB/s²².

The Bureau of Industry and Security (BIS), the US export control office, published the rule on 5 December 2024². It added an export classification, ECCN 3A090.c, for "High bandwidth memory (HBM) having a 'memory bandwidth density' greater than 2 gigabytes per second per square millimeter"². Its technical note defines that density as

¹ SK hynix, prospectus on Form 424B4 dated 10 July 2026. U.S. Securities and Exchange Commission, 10 July 2026. sec.gov

² Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... Federal Register, 5 December 2024. federalregister.gov

⁴ China's CXMT Is Set to Challenge DRAM Incumbents. SemiAnalysis, 23 June 2026. newsletter.semianalysis.com

⁵ Fiscal Q1 2026 Earnings Call Prepared Remarks. Micron Technology, 17 December 2025. s25.q4cdn.com

¹⁴ Micron Technology, annual report on Form 10-K for the fiscal year ended 3... U.S. Securities and Exchange Commission, 9 October 2026. sec.gov

²⁰ NVIDIA GB300 NVL72. Nvidia, 23 July 2026. nvidia.com

²¹ Inside NVIDIA Rubin GPU Architecture: Powering the Era of Agentic AI. Nvidia, 21 July 2026. developer.nvidia.com

²² AMD Instinct™ MI355X GPUs. AMD, accessed 9 September 2026. amd.com

the memory bandwidth in gigabytes per second divided by the area of the package or stack in square millimeters². The rule also covers stacks made outside the United States, through a foreign direct product rule, which applies US controls to goods made abroad with American technology². BIS stated in the rule that all HBM stacks then in production exceeded that threshold².

BIS reviews license applications to ship controlled HBM to Macau or a Country Group D:5 destination such as China according to where the buyer is headquartered²³. It presumes it will deny a license when the buyer or its ultimate parent is headquartered in one of those places, and presumes approval otherwise²³.

Two provisions narrow the control. License Exception HBM, at 15 CFR 740.25, applies to exporters headquartered in the United States or a Country Group A:5 ally⁷. It lets them ship HBM below 3.3 GB per second per square millimeter without a license, including to Macau and Country Group D:5 destinations such as China⁷. HBM sent to those destinations must be bought directly by the designer of the chip it will be packaged into⁷. Every shipment under the exception must go straight to the packaging site⁷. The rule also excludes co-packaged chips that combine HBM and logic and whose main function is processing, which other chip controls may cover instead².

The think tank CSIS said in December 2024 that the rules still allowed HBM2, a generation introduced in 2016, to go to China, with limits on who could buy it and what for²⁴. It also said Nvidia's H20, whose HBM3 is packaged with the processor, was then still exportable under the performance limits for AI chips²⁴.

In December 2024 CSIS called CXMT one of only two Chinese firms with a credible path to producing advanced HBM, though it did not name the other²⁴. The Institute for Progress reported in October 2025 that CXMT was planning to produce HBM3 in 2026³. It also estimated that China would make virtually no HBM in 2025³.

Huawei plans to use HBM of its own design in its Ascend 950 AI chips, but when it announced the designs in September 2025 it did not say who would make the memory⁶. The two designs are called HiBL 1.0 and HiZQ 2.0⁶. Huawei said the 950DT, due in the fourth quarter of 2026, would carry 144 GB of HiZQ 2.0 at 4 TB/s⁶.

Four questions to answer from memory

1. What is HBM? see How it works
 2. Why does an AI chip need such fast memory? see How it works
 3. What is the hard part of making HBM? see How it works
 4. Who makes HBM? see Who makes it
-

Four things to remember

- HBM is memory stacked into a cube beside the processor and wired to pass data fast.
-

² Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for... Federal Register, 5 December 2024. [federalregister.gov](https://www.federalregister.gov)

³ Should the US Sell Blackwell Chips to China? Institute for Progress, 25 October 2025. ifp.org

⁶ Groundbreaking SuperPoD Interconnect: Leading a New Paradigm for AI... Huawei, 18 September 2025. huawei.com

⁷ 15 CFR 740.25 -- License Exception High Bandwidth Memory (HBM). Electronic Code of Federal Regulations, 5 December 2024. ecfr.gov

²³ 15 CFR 742.6, Regional stability. Electronic Code of Federal Regulations, 23 July 2026. ecfr.gov

²⁴ Understanding the Biden Administration's Updated Export Controls. Center for Strategic and International Studies, 11 December 2024. csis.org

- An AI chip reads its whole model from memory for each word, so memory speed limits it.
- SK hynix, Samsung and Micron make nearly all HBM.
- Since December 2024 US controls have covered the HBM stacks then in production, with two exceptions. The Institute for Progress estimated that China made virtually no HBM in 2025.

Sources (24)

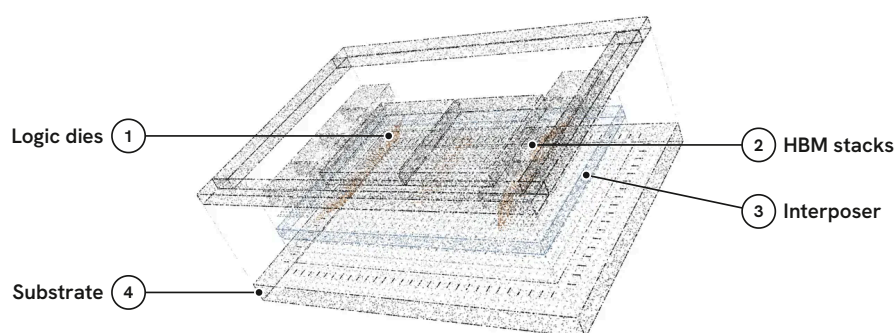
1. A SK hynix, prospectus on Form 424B4 dated 10 July 2026. U.S. Securities and Exchange Commission (filing by SK hynix) · 10 July 2026
www.sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm
2. A Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items. Federal Register (Commerce Department; Industry and Security Bureau) · 5 December 2024
www.federalregister.gov/documents/2024/12/05/2024-28270/foreign-produced-direct-product-rule-additions-and-refinements-to-controls-for-advanced-computing
3. A Should the US Sell Blackwell Chips to China?. Institute for Progress · 25 October 2025
ifp.org/the-b30a-decision/
4. B China's CXMT Is Set to Challenge DRAM Incumbents. SemiAnalysis · 23 June 2026
newsletter.semianalysis.com/p/chinas-cxmt-is-set-to-challenge-dram
5. A Fiscal Q1 2026 Earnings Call Prepared Remarks. Micron Technology · 17 December 2025
s25.q4cdn.com/621799436/files/doc_financials/2026/q1/Micron_Q1-2026-Prepared-Remarks.pdf
6. A Groundbreaking SuperPoD Interconnect: Leading a New Paradigm for AI Infrastructure. Huawei · 18 September 2025
www.huawei.com/en/news/2025/9/hc-xu-keynote-speech
7. A 15 CFR 740.25 -- License Exception High Bandwidth Memory (HBM).. Electronic Code of Federal Regulations · 5 December 2024
www.ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-740/section-740.25
8. A High-bandwidth memory (HBM). Micron Technology · Accessed 9 September 2026
www.micron.com/products/memory/hbm
9. A JEDEC® and Industry Leaders Collaborate to Release JESD270-4 HBM4 Standard: Advancing Bandwidth, Efficiency, and Capacity for AI and HPC. JEDEC Solid State Technology Association · 16 April 2025
www.jedec.org/news/pressreleases/jedec%2%AE-and-industry-leaders-collaborate-release-jesd270-4-hbm4-standard-advancing
10. A Micron, HBM3E product page. Micron Technology · Accessed 9 September 2026
www.micron.com/products/memory/hbm/hbm3e
11. A SK hynix Completes World's First HBM4 Development and Readies Mass Production. SK hynix · 12 September 2025
news.skhyunx.com/en/sk-hynix-completes-worlds-first-hbm4-development-and-readies-mass-production/
12. A Samsung Ships Industry-First Commercial HBM4 With Ultimate Performance for AI Computing. Samsung Global Newsroom · 12 February 2026
news.samsung.com/global/samsung-ships-industry-first-commercial-hbm4
13. A Micron, HBM4 product page. Micron Technology · Accessed 9 September 2026
www.micron.com/products/memory/hbm/hbm4
14. A Micron Technology, annual report on Form 10-K for the fiscal year ended 3 September 2026. U.S. Securities and Exchange Commission (filing by Micron Technology) · 9 October 2026
www.sec.gov/Archives/edgar/data/723125/000072312526000023/mu-20260903.htm
15. A SK hynix Partners with TSMC to Strengthen HBM Technological Leadership. SK hynix · 19 April 2024
news.skhyunx.com/sk-hynix-partners-with-tsmc-to-strengthen-hbm-technological-leadership/
16. A HBM3e and HBM4: IC design guide for next-generation high bandwidth memory. Siemens Digital Industries Software · 24 April 2026
blogs.sw.siemens.com/semiconductor-packaging/2026/04/24/hbm3e-hbm4-ic-design-guide/
17. A [Tech Note] Hybrid Bonding: Evolving into a Foundational Technology for Improving Semiconductor Performance. SK hynix · 25 August 2026
news.skhyunx.com/en/tech-note-series-ep2/
18. A Samsung Develops Industry-First 36GB HBM3E 12H DRAM. Samsung Global Newsroom · 27 February 2024
news.samsung.com/global/samsung-develops-industry-first-36gb-hbm3e-12h-dram
19. A SK hynix breaks ground on \$4 billion advanced packaging production facility in Purdue Research Park. Purdue University · 27 August 2026
www.purdue.edu/newsroom/2026/Q3/sk-hynix-breaks-ground-on-4-billion-advanced-packaging-production-facility-in-purdue-research-park/
20. A NVIDIA GB300 NVL72. Nvidia · 23 July 2026
www.nvidia.com/en-us/data-center/gb300-nvl72/
21. A Inside NVIDIA Rubin GPU Architecture: Powering the Era of Agentic AI. Nvidia · 21 July 2026
developer.nvidia.com/blog/inside-nvidia-rubin-gpu-architecture-powering-the-era-of-agentic-ai/
22. A AMD Instinct™ MI355X GPUs. AMD · Accessed 9 September 2026
www.amd.com/en/products/accelerators/instinct/mi350/mi355x.html

23. A **15 CFR 742.6, Regional stability.** Electronic Code of Federal Regulations · 23 July 2026
www.ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-742/section-742.6
24. A **Understanding the Biden Administration's Updated Export Controls.** Center for Strategic and International Studies · 11 December 2024
www.csis.org/analysis/understanding-biden-administrations-updated-export-controls

01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Advanced Packaging

Epoch AI estimates that in 2025 Nvidia, Google, AMD and Amazon used around 90 percent of the capacity for CoWoS, TSMC's packaging for AI chips.



Specimen 10 · Advanced Packaging

A CoWoS-L package, pulled apart. Two logic dies and eight HBM stacks sit on the interposer, shown in silver with its copper wiring. In CoWoS-L the interposer is fine redistribution wiring with small embedded silicon bridges. It sits on a resin substrate with a grid of solder balls underneath. The chips together cover about 2,700 mm², a little over three reticle fields. Footprints are to scale. Thicknesses and the gaps between layers are exaggerated.

Parts, as numbered on the drawing

- ① Logic dies, two: [see stage 08, Foundries and Fabs](#)
- ② HBM stacks, eight: [see stage 09, Memory and HBM](#)
- ③ Interposer: TSMC (TW), as CoWoS
- ④ Substrate: [see stage 11, Substrates and PCBs](#)

In plain terms

Packaging joins finished chips into one component and mounts them on a small circuit board, called a substrate, wired far more coarsely than the chips themselves. A lithography machine, which prints a chip's circuits, can cover only a rectangle about the size of a postage stamp in one shot. Many leading accelerators, Nvidia's Blackwell among them, need more logic than fits in that rectangle. So they are built from several chips, called dies, set side by side on an interposer, a layer of much finer wiring that links them and sits on the substrate.

Stacks of memory chips sit on the same interposer, a few millimeters away. The interposer is either one piece of silicon or layers of fine copper wiring that often carry small silicon bridges where the links are densest. Silicon expands less than the resin substrate beneath it when heated, so the package can warp and its joints crack. Preventing that in high volume is hard. Nvidia, Google, AMD and Amazon all use TSMC's interposer packaging, called CoWoS, made in Taiwan.

In short

Epoch AI estimates that in 2025 Nvidia used 60.3 percent of all capacity for CoWoS, TSMC's interposer packaging¹. On the July 2026 earnings call, TSMC's chief executive, C.C. Wei, said its packaging capacity was so tight that it limited customers' growth². Asked about Intel's EMIB-T packaging, he said he hoped it would take some of the load off TSMC².

In a TrendForce ranking by 2024 revenue, which CSET cites, four of the top ten outsourced firms that package and test chips are headquartered in China³. But in 2025 Chinese firms had 5.3 percent of the market for advanced packaging fabrication tools, against 65.8 percent for US firms, by CSET's analysis of TechInsights data⁴.

A lithography scanner prints a rectangle 26 mm by 33 mm, or 858 mm², in one exposure⁵. That area is called the reticle field. Every leading AI accelerator, counting its memory stacks, covers more area than that. Packaging is the stage that lets an accelerator be larger than one reticle field, and the packaging method limits how much larger it can be.

Chokepoint card			Advanced Packaging
<div>Concentration</div> <div> Extreme</div> <div>Three or fewer firms could supply this stage today, or one firm holds more than half of it.</div>	<div>Substitutability</div> <div>Hard</div> <div>Rated on CoWoS capacity, which TSMC said in July 2026 was so tight that it limited its customers' growth².</div>	<div>Price or market size</div> <div>About \$1,100</div> <div>for the CoWoS-L packaging of one Nvidia B200, plus about \$1,000 for the dies and memory lost in failed packages, against about \$900 for its two logic dies, by Epoch AI's December 2025 estimate⁶</div>	

1

Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip... Epoch AI, 12 March 2026. epoch.ai

2

Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese... LSEG StreetEvents, 16 July 2026, p. 10. investor.tsmc.com

3

Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology, 14 July 2025. cset.georgetown.edu

4

Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 20 October 2026. chipexplorer.eto.tech

5

TWINSCAN NXE:3400C. ASML, accessed 9 September 2026. asml.com

6

NVIDIA's B200 costs around \$6,400 to produce. Epoch AI, 10 December 2025. epoch.ai

Who leads	TW	TSMC	CoWoS packaging used by Nvidia, Google, AMD and Amazon in 2025 ¹
	US	Intel	Foveros 3D packaging in volume at Rio Rancho, New Mexico, since January 2024 ⁷
	TW	ASE Technology	NT\$389.2 billion assembly, test and materials revenue, 2025 ⁸
	US	Amkor	\$6.71 billion net sales, 2025 ⁹
	CN	JCET	RMB 38.87 billion revenue, 2025 ¹⁰
Where it is made	SG	ASMPT	Thermocompression bonders, with \$532.1 million of advanced packaging revenue in 2025 ¹¹
	TW	Taiwan	TSMC advanced packaging fabs and a cluster of outsourced assembly and test firms
	US	United States	Intel Foveros packaging in volume at Rio Rancho, New Mexico
	CN	China	Four of the top ten outsourced assembly and test firms by 2024 revenue are Chinese, in a TrendForce ranking cited by CSET
	NL	Netherlands	Besi hybrid bonders
Why substitution is slow	JP	Japan	Disco grinders and dicers
	CoWoS packaging has been outsourced to assembly firms such as ASE and Amkor before ¹² . Intel's EMIB, which links chips through silicon bridges embedded in the substrate, is another option, and Amazon's Trainium and Google's TPU were both adopting it as of March 2026 ¹² . But a newcomer would have to match TSMC, which said in April 2026 that it was producing CoWoS at 5.5 times the area a scanner prints in one shot ¹³ .		
Where China stands		Where the US stands	
Chinese firms had 5.3 percent of the market for fabrication tools built for advanced packaging in 2025, by CSET's analysis of TechInsights data ⁴ . Between 2019 and 2024 they gained 5 percentage points of share in test tools but lost share in bonding and other conventional assembly and packaging tools ³ .		Intel opened Fab 9 in Rio Rancho, New Mexico, in January 2024 to make its Foveros 3D packages in volume ⁷ . Amkor broke ground in October 2025 on a \$7 billion packaging and test campus in Peoria, Arizona, and expects production to start in early 2028 ¹⁴ .	

01

How advanced packaging and CoWoS work

A second reason for the interposer is high bandwidth memory (HBM). An HBM4 stack connects through 2,048 data signals, packed too tightly for a standard resin substrate, so the memory sits beside the logic on the interposer¹⁵. Even Nvidia's H100, whose single logic die is 814 mm² and fits inside one reticle field, carries five HBM stacks¹⁶. Epoch AI counts TSMC's CoWoS packaging among the three inputs the H100 needs, along with its logic die and its HBM¹.

Figure 10.1 · Explainer, 19 seconds

1 Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip... Epoch AI, 12 March 2026. epoch.ai

3 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology, 14 July 2025. cset.georgetown.edu

4 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 20 October 2026. chipexplorer.eto.tech

7 Intel Opens Fab 9 in New Mexico. Intel, 24 January 2024. intel.com

8 ASE Technology Holding Co., Ltd. Reports Its Unaudited Consolidated Financial... PR Newswire, 5 February 2026. prnewswire.com

9 Amkor Technology, current report on Form 8-K dated 9 February 2026. U.S. Securities and Exchange Commission, 9 February 2026. sec.gov

10 JCET Releases 2025 Annual Report, Posts Record-High Full-Year Revenue and... JCET Group, 9 April 2026. jcetglobal.com

11 ASMPT Announces 2025 Annual Results AI-Driven Structural Growth Underpins Group... ASMPT, 4 March 2026. asmpt.com

12 The Great AI Silicon Shortage. SemiAnalysis, 12 March 2026. newsletter.semianalysis.com

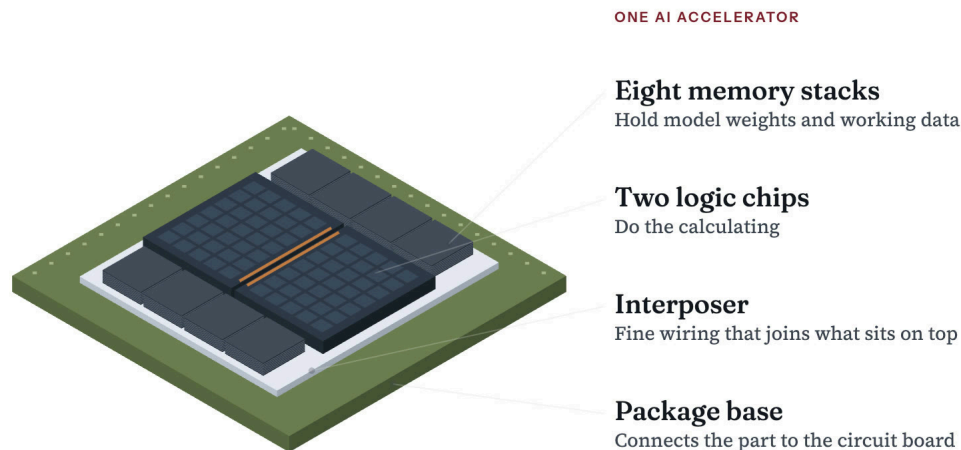
13 TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC, 23 April 2026. pr.tsmc.com

14 Amkor Technology Breaks Ground on New Semiconductor Advanced Packaging and Test... Amkor Technology, 6 October 2025. ir.amkor.com

15 New JEDEC® SPHBM4 Standard Enables HBM4-Class Bandwidth on Organic Substrates. JEDEC Solid State Technology Association, 13 July 2026. jedec.org

16 NVIDIA Hopper Architecture In-Depth. Nvidia, 22 March 2022. developer.nvidia.com

The parts of an AI accelerator



1. **Package base.** An AI chip is built from several parts. First comes the package base, a layered board that connects everything to the circuit board below.
2. **Interposer.** On it sits an interposer, a thin layer of very fine wiring that joins everything placed on top.
3. **Logic chips.** Two logic chips go in the middle. They do the calculating, and each is as large as a chipmaking machine can print.
4. **Memory.** Eight stacks of memory go beside them, a few millimeters away. They hold the AI model's weights and the record of each conversation so far.
5. **One package.** Together they make one AI accelerator. Most are put together by TSMC, in Taiwan.

Note: Simplified view of a two-die, eight-stack accelerator. Footprints follow the sizes given in this chapter and chapter 9. Heights are exaggerated so each layer shows.

CoWoS stands for chip on wafer on substrate, the order in which the parts are joined. For CoWoS-S, the version whose interposer is one piece of silicon, TSMC makes a silicon wafer that carries wiring and vertical copper vias but no transistors. Vias are metal-filled holes that join one layer of wiring to the next.

TSMC bonds the logic dies and memory stacks face down onto that wafer with microbumps. These are dots of solder, and each dot is one electrical joint. In Intel's Foveros 2.5D packaging, which can also set dies side by side on a silicon interposer, the microbumps sit 36 micrometers apart, less than half a hair's width¹⁷. The spacing differs by design, and SK hynix gives about 20 micrometers as typical for microbumps¹⁸. Then TSMC cuts the interposer out of the wafer and attaches it to the resin substrate, which later goes onto a circuit board.

One cracked joint can scrap a package holding eight tested HBM stacks and two large, expensive logic dies. Epoch AI estimated in December 2025 that CoWoS-L packaging, the version built with small silicon bridges, added about \$1,100 to the cost of building one Nvidia B200⁶. That is more than its estimate of about \$900 for the B200's two logic dies⁶. Epoch AI adds about \$1,000 more to each B200 for the packages that fail testing, whose logic dies and memory stacks are lost⁶.

⁶ NVIDIA's B200 costs around \$6,400 to produce. Epoch AI, 10 December 2025. epoch.ai

¹⁷ Foveros Direct 3D Technology Brief. Intel, 6 February 2026. intel.com

¹⁸ [Tech Note] Hybrid Bonding: Evolving into a Foundational Technology for... SK hynix, 25 August 2026. news.skhynix.com

02

Types of advanced packaging

Family	Carrier	Size limit	Used for
CoWoS-S	Full silicon interposer	Up to 3.3× reticle	H100-class parts
CoWoS-R	Resin interposer with fine redistribution wiring	Above 3.3× reticle	Cost-sensitive, fewer HBM stacks
CoWoS-L	Redistribution wiring with local silicon bridges	5.5× reticle in production, 9.5× in development	Blackwell

2.5D: silicon, RDL and bridges

In 2.5D packaging the chips sit side by side and connect through an interposer or silicon bridges beneath them. TSMC has run CoWoS in volume since 2012¹⁹. CoWoS-S has the finest wiring, but its interposer is one unbroken piece of silicon whose yield (the share of interposers that work) falls as the area grows. CoWoS-L replaces that piece of silicon with redistribution layers (RDL) of fine copper wiring and embeds small silicon bridges where the wiring is densest²⁰.

Intel's EMIB embeds similar silicon bridges in the resin substrate¹⁷. SemiAnalysis reported in March 2026 that EMIB was gaining traction, with Amazon's Trainium and Google's TPU both adopting it¹².

Blackwell was the first high-volume design on CoWoS-L, and packaging problems at TSMC and in Nvidia's design limited its supply²¹. The bridges that carry the 10 TB/s link between the two logic dies must be placed very precisely²¹. The dies, bridges, interposer and substrate also expand at different rates, and that mismatch caused warpage²¹.

3D: SoIC and Foveros

In 3D packaging one die sits on top of another, and the joints between them are moving from solder microbumps to hybrid bonding. Intel's Foveros stacks dies face to face and joins them with solder microbumps¹⁷. Its newer Foveros Direct drops the solder and bonds the copper pads directly, a method called hybrid bonding¹⁷. Hybrid bonding joins the insulating layer around the pads as well as the copper, with no bumps in between¹⁸. That lets the connections sit far closer together than microbumps allow¹⁷. TSMC's SoIC also uses hybrid bonding, and AMD's 3D V-Cache processors use SoIC to attach an extra cache die to the processor die²². Stacking also changes how power reaches the top die, which has to draw it up through vertical wires in the die below, called through-silicon vias (TSVs)²².

¹² The Great AI Silicon Shortage. SemiAnalysis, 12 March 2026. newsletter.semianalysis.com

¹⁷ Foveros Direct 3D Technology Brief. Intel, 6 February 2026. [intel.com](https://www.intel.com)

¹⁸ [Tech Note] Hybrid Bonding: Evolving into a Foundational Technology for... SK hynix, 25 August 2026. news.skhynix.com

¹⁹ TSMC, CoWoS technology page. TSMC, accessed 9 September 2026. 3dfabric.tsmc.com

²⁰ TSMC 2025 Annual Report, chapter 5. TSMC, 16 April 2026, p. 3. investor.tsmc.com

²¹ Nvidia's Blackwell Reworked - Shipment Delays & GB200A Reworked Platforms. SemiAnalysis, 4 August 2024. semianalysis.com

²² Hybrid Bonding Process Flow - Advanced Packaging Part 5. SemiAnalysis, 9 February 2024. newsletter.semianalysis.com

TSMC put SoIC into volume production in 2022, stacking SRAM memory chips on logic wafers²³. Its 3 nm SoIC entered volume production in 2025²⁰. An A14-on-A14 version, stacking dies made on TSMC's 1.4 nm process, is due in 2029¹³. It will carry 1.8 times the die-to-die connection density of SoIC that stacks 2 nm dies on 2 nm dies¹³.

SoIC bonding also brings optics into the package. TSMC's COUPE uses SoIC to join a silicon photonics chip, which sends data as light, to its electrical control chip²⁰. In April 2026 TSMC planned to begin producing COUPE on substrate later that year¹³. It also said that putting COUPE inside the package gives twice the power efficiency of a pluggable version on the circuit board¹³.

Two ways off the silicon interposer

Panel-level packaging builds packages on a large rectangular panel instead of a round wafer, so rectangular packages fit it with less waste at the edges. See Test and assembly. JEDEC, the semiconductor standards body, published a standard called SPHBM4 on 13 July 2026. It puts HBM4 memory on a base chip carrying 512 data signals instead of 2,048, each running four times as fast to keep the same bandwidth¹⁵. With fewer signals, the connections can be spaced widely enough to mount the stack on a standard resin substrate instead of the silicon interposer¹⁵.

03

TSMC's CoWoS capacity and its buyers

TSMC does not publish its CoWoS capacity¹. Industry estimates from SemiWiki and TrendForce, compiled by Epoch AI, put it at about 65,000 to 75,000 wafers a month at the end of 2025, up from 35,000 to 40,000 a year earlier¹.

On the July 2024 earnings call, TSMC's chief executive, C.C. Wei, said TSMC was more than doubling CoWoS capacity in 2024 and would more than double it again in 2025²⁴. He said he could not yet balance supply and demand²⁴. At its 2024 symposium TSMC had said CoWoS capacity would grow at a 60 percent compound annual rate over the next few years²⁴. Asked about that rate on the call, Wei did not repeat it²⁴.

In October 2025 Wei would say only that TSMC was still working to increase CoWoS capacity for 2026, and he gave no figure²⁵. He said front-end capacity (making the chips) and back-end capacity (packaging them) were both, in his words, very tight²⁵.

By Epoch AI's estimate, four chip designers used most of the world's CoWoS capacity in 2025 but only a small share of its advanced chipmaking. Epoch AI compared each chip designer's use of components with world supply¹. It puts Nvidia at 60.3 percent of all CoWoS capacity in 2025, with a 90 percent confidence interval of 56.5 to 64.3¹. Google took 13.5 percent, AMD 8.4 and Amazon 7.4¹. The four also used around 90 percent of

¹ Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip... Epoch AI, 12 March 2026. epoch.ai

¹³ TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC, 23 April 2026. pr.tsmc.com

¹⁵ New JEDEC® SPHBM4 Standard Enables HBM4-Class Bandwidth on Organic Substrates. JEDEC Solid State Technology Association, 13 July 2026. jedec.org

²⁰ TSMC 2025 Annual Report, chapter 5. TSMC, 16 April 2026, p. 3. investor.tsmc.com

²³ TSMC 2022 Annual Report, page 97. TSMC, accessed 18 October 2026. investor.tsmc.com

²⁴ Q2 2024 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese... Refinitiv StreetEvents, 18 July 2024, p. 6. investor.tsmc.com

²⁵ Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese... Refinitiv StreetEvents, 16 October 2025, p. 7. investor.tsmc.com

global HBM supply in 2025, measured by value¹. But they used only 12 percent of advanced logic die production¹.

Figure 10.2

Nvidia used an estimated 60.3 percent of CoWoS capacity in 2025

Estimated share of CoWoS capacity used, 2025



Source: Epoch AI, advanced packaging and HBM were the bottlenecks on AI chip production in 2025 [1]

In March 2026 the research firm SemiAnalysis judged that front-end capacity had become the dominant bottleneck and that CoWoS constraints were easing¹². It said TSMC was planning CoWoS capacity around how many wafers N3, its 3 nm process, could produce, because added packaging capacity is of no use without front-end wafers to fill it¹².

TSMC gave a different account four months later. On the July 2026 earnings call, Wei said back-end capacity was still in shortage²⁶. Asked about Intel's EMIB-T, he said he welcomed the extra flexibility and hoped it would take some of the load off TSMC².

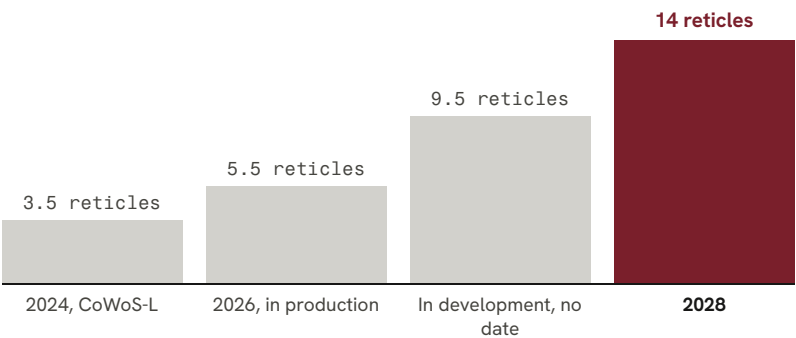
04

Who makes advanced packages

Figure 10.3

TSMC plans 14-reticle CoWoS interposers for 2028, up from 3.5 in 2024

CoWoS interposer size on TSMC's roadmap



Source: TSMC 2025 annual report and 2026 technology symposium [13]

Note: The 2024 column is CoWoS-L. CoWoS-S, whose interposer is one piece of silicon, reaches up to 3.3 reticles.

1 Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip... Epoch AI, 12 March 2026. epoch.ai
2 Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese... LSEG StreetEvents, 16 July 2026, p. 10. investor.tsmc.com
12 The Great AI Silicon Shortage. SemiAnalysis, 12 March 2026. newsletter.semianalysis.com
13 TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC, 23 April 2026. pr.tsmc.com
26 Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese... LSEG StreetEvents, 16 July 2026, p. 17. investor.tsmc.com

Three kinds of firm package chips. TSMC, which makes chips for others, and Intel, which makes its own, do it in their own back-end fabs. Outsourced assembly and test firms do the rest. Intel opened Fab 9 in Rio Rancho, New Mexico, in January 2024 to make its Foveros 3D packages in volume⁷. It called the plant the only US factory producing the most advanced packaging at scale⁷.

ASE leads the outsourced assembly and test firms, and Amkor is the largest one headquartered in the United States. ASE Technology Holding had revenue of NT\$645.4 billion in 2025, about 40 percent of it from its electronics manufacturing arm, a business separate from assembly and test⁸. Its assembly, test and materials business brought in NT\$389.2 billion, up from NT\$325.9 billion in 2024⁸. Amkor had net sales of \$6.71 billion in 2025⁹.

Each of the key packaging tools comes from a small number of makers.

- **Thermocompression bonding.** Pressing dies together under heat and force. ASMPT's advanced packaging revenue reached \$532.1 million in 2025, with thermocompression bonder revenue up about 146 percent¹¹. ASMPT targets 35 to 40 percent of a market it puts at \$1.6 billion in 2028¹¹.
- **Hybrid bonding.** Copper pads and the insulator around them bond directly, with no solder. Applied Materials co-developed its Kinex hybrid bonding system with Besi, which Applied calls the industry leader in hybrid bonding²⁷.
- **Grinding and dicing.** Disco held 87 percent of the \$1.9 billion world market for dicing tools in 2025, by CSET's count from TechInsights data²⁸. The category covers the grinders that thin wafers and the saws that cut them into chips²⁸. See Test and assembly.

TSMC and Amkor both plan advanced packaging plants in Arizona. TSMC's Arizona commitment reached \$265 billion in July 2026 and covers two advanced packaging plants alongside 10 fabs²⁹. Amkor started building a \$7 billion campus in Peoria, Arizona, in October 2025 and expects production from early 2028¹⁴. The US Commerce Department awarded Amkor up to \$407 million in CHIPS Act funding for the site in December 2024³⁰. In October 2025 Wei said a large outsourced packaging partner, which he did not name, was already breaking ground in Arizona³¹. He said its plant was on an earlier schedule than TSMC's own two packaging fabs there³¹.

⁷ Intel Opens Fab 9 in New Mexico. Intel, 24 January 2024. [intel.com](https://www.intel.com)

⁸ ASE Technology Holding Co., Ltd. Reports Its Unaudited Consolidated Financial... PR Newswire, 5 February 2026. [prnewswire.com](https://www.prnewswire.com)

⁹ Amkor Technology, current report on Form 8-K dated 9 February 2026. U.S. Securities and Exchange Commission, 9 February 2026. [sec.gov](https://www.sec.gov)

¹¹ ASMPT Announces 2025 Annual Results AI-Driven Structural Growth Underpins Group... ASMPT, 4 March 2026. [asmpt.com](https://www.asmpt.com)

¹⁴ Amkor Technology Breaks Ground on New Semiconductor Advanced Packaging and Test... Amkor Technology, 6 October 2025. ir.amkor.com

²⁷ Applied Materials, Kinex integrated die-to-wafer hybrid bonding system product... Applied Materials, accessed 9 September 2026. [appliedmaterials.com](https://www.appliedmaterials.com)

²⁸ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

²⁹ TSMC Announces Additional \$100 Billion Investment in Arizona. Arizona Commerce Authority, 16 July 2026. [azcommerce.com](https://www.azcommerce.com)

³⁰ Amkor Technology, annual report on Form 10-K for the fiscal year ended 31... U.S. Securities and Exchange Commission, 20 February 2026. [sec.gov](https://www.sec.gov)

³¹ Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese... Refinitiv StreetEvents, 16 October 2025, p. 13. investor.tsmc.com

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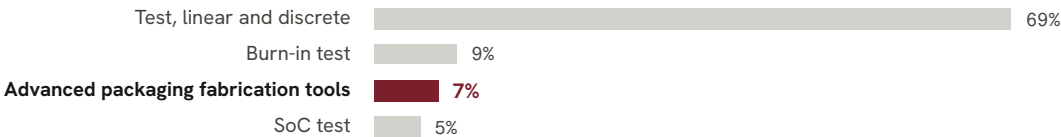
The chokepoint

Nvidia, Google, AMD and Amazon all use TSMC's interposer packaging, called CoWoS, made in Taiwan. By Epoch AI's estimate, those four used around 90 percent of global CoWoS capacity in 2025¹. In 2024 TSMC was more than doubling CoWoS capacity and still could not keep up with demand²⁴. On the July 2026 earnings call, TSMC's chief executive, C.C. Wei, said its packaging capacity was so tight that it limited customers' growth². CoWoS packaging can be, and has been, outsourced to assembly firms such as ASE and Amkor¹².

Figure 10.4

China-based suppliers held 7 percent of the market for advanced packaging fabrication tools in 2024

China-based suppliers' share of advanced packaging fabrication tools and three test tool segments, 2024



Source: CSET, Inside Beijing's Chipmaking Offensive [3]

Four of the top ten outsourced assembly and test firms by 2024 revenue are headquartered in China, by a TrendForce ranking that CSET cites³. JCET, a leading Chinese assembly and test firm, had record revenue of RMB 38.87 billion in 2025, up 8.1 percent¹⁰. JCET says its XDFOI packaging platform has entered high-volume manufacturing with redistribution-layer interposer, silicon interposer and silicon bridge options³². Those are the same three kinds of carrier that TSMC sells as CoWoS-R, CoWoS-S and CoWoS-L.

Chinese firms had a small share of the market for advanced packaging tools in 2024 and 2025, and they lost ground in bonding. In 2024 Chinese firms had 7 percent of the market for advanced packaging fabrication tools³. Between 2019 and 2024, they gained 5 percentage points of share in test tools and 4 points in fabrication tools built for advanced packaging, by CSET's analysis of TechInsights data³. But they lost share in bonding and other conventional assembly and packaging tools, the category where CSET counts hybrid and thermocompression bonders³. Within the advanced packaging fabrication tools, Chinese firms gained 10 points in etch and clean tools and 3 points in deposition tools³. They lost 2 points each in lithography and polishing (CMP) tools³. CSET's Chip Explorer, a separate data tool also built on TechInsights data, puts Chinese firms at 5.3 percent of the \$6.2 billion world market for advanced

1 Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip... Epoch AI, 12 March 2026. epoch.ai
2 Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese... LSEG StreetEvents, 16 July 2026, p. 10. investor.tsmc.com
3 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology, 14 July 2025. cset.georgetown.edu
10 JCET Releases 2025 Annual Report, Posts Record-High Full-Year Revenue and... JCET Group, 9 April 2026. jcetglobal.com
12 The Great AI Silicon Shortage. SemiAnalysis, 12 March 2026. newsletter.semianalysis.com
24 Q2 2024 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese... Refinitiv StreetEvents, 18 July 2024, p. 6. investor.tsmc.com
32 JCET Accelerates Strategic Shift Toward High-End Advanced Packaging, 2025... JCET Group, 21 April 2026. jcetglobal.com

packaging fabrication tools in 2025⁴. It puts US firms at 65.8 percent and Japanese firms at 15.3 percent⁴.

TSMC said in April 2026 that it was producing CoWoS at 5.5 times the size of a reticle field and planning larger versions¹³. Each generation on TSMC's roadmap needs a larger interposer.

- **2028.** A 14-reticle interposer, about the area of a compact disc, carrying about ten large compute dies and 20 HBM stacks¹³.
- **2029.** More than 14 reticles, plus a 40-reticle System-on-Wafer¹³. TSMC describes System-on-Wafer as joining different data center chips at the scale of a whole wafer³³.

Four questions to answer from memory

1. Why is an AI accelerator built from several chips in one package? see How it works
 2. Why is packaging hard? see How it works
 3. Which company packages the leading AI chips? see How it works
 4. Why has packaging limited how many AI chips can be made? see Capacity
-

Four things to remember

- Many leading accelerators, Nvidia's Blackwell among them, need more logic than one chip can hold, so packaging joins several chips and their memory.
 - Nvidia, Google, AMD and Amazon all rely on TSMC, in Taiwan, to package their accelerators.
 - Packaging was one of the main limits on AI chip output in 2025. In July 2026 TSMC said its packaging capacity was still so tight that it limited customers' growth.
 - No US site yet packages Nvidia-class accelerators with HBM on CoWoS, though Intel makes its own Foveros 3D packages in volume in New Mexico.
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Sources (33)

1. A Advanced packaging and HBM, not logic dies, were the bottlenecks on AI chip production in 2025. Epoch AI · 12 March 2026
epoch.ai/data-insights/ai-chip-supply-chain-constraints
2. A Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. LSEG StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 July 2026 · p. 10
investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897aa044415e21d93486cc4/TSMC%202026%20Transcript.pdf#page=10
3. A Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology (CSET) · 14 July 2025
cset.georgetown.edu/article/inside-beijings-chipmaking-offensive/
4. A Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 20 October 2026
chipexplorer.eto.tech/?parentNode=N69&selectedNode=N109
5. A TWINSCAN NXE:3400C. ASML · Accessed 9 September 2026
www.asml.com/en/products/euv-lithography-systems/twinscan-nxe3400c
6. A NVIDIA's B200 costs around \$6,400 to produce. Epoch AI · 10 December 2025
epoch.ai/data-insights/b200-cost-breakdown
7. A Intel Opens Fab 9 in New Mexico. Intel · 24 January 2024
www.intel.com/content/www/us/en/newsroom/news/intel-opens-fab-9-new-mexico.html

⁴ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 20 October 2026. chipexplorer.eto.tech

¹³ TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC, 23 April 2026. pr.tsmc.com

³³ TSMC 2025 Annual Report, chapter 5. TSMC, 16 April 2026, p. 4. investor.tsmc.com

8. A ASE Technology Holding Co., Ltd. Reports Its Unaudited Consolidated Financial Results for the Fourth Quarter and the Full Year of 2025. PR Newswire · 5 February 2026
www.prnewswire.com/news-releases/ase-technology-holding-co-ltd-reports-its-unaudited-consolidated-financial-results-for-the-fourth-quarter-and-the-full-year-of-2025-302679779.html
9. A Amkor Technology, current report on Form 8-K dated 9 February 2026. U.S. Securities and Exchange Commission (filing by Amkor Technology) · 9 February 2026
www.sec.gov/Archives/edgar/data/1047127/000104712726000007/amkr123125erex-991.htm
10. A JCET Releases 2025 Annual Report, Posts Record-High Full-Year Revenue and Higher Profit Before Tax. JCET Group · 9 April 2026
www.jcetglobal.com/en/site/news-detail?id=2048
11. A ASMPT Announces 2025 Annual Results AI-Driven Structural Growth Underpins Group Performance. ASMPT · 4 March 2026
www.asmpt.com/en/investor-relations/news-events/asmpt-announces-2025-annual-results/
12. B The Great AI Silicon Shortage. SemiAnalysis · 12 March 2026
newsletter.semanalysis.com/p/the-great-ai-silicon-shortage
13. A TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC · 23 April 2026
pr.tsmc.com/english/news/3302
14. A Amkor Technology Breaks Ground on New Semiconductor Advanced Packaging and Test Campus in Arizona; Expands Investment to \$7 Billion. Amkor Technology · 6 October 2025
ir.amkor.com/news-releases/news-release-details/amkor-technology-breaks-ground-new-semiconductor-advanced
15. A New JEDEC® SPHBM4 Standard Enables HBM4-Class Bandwidth on Organic Substrates. JEDEC Solid State Technology Association · 13 July 2026
www.jedec.org/news/pressreleases/new-jedec%2%AE-sphbm4-standard-enables-hbm4-class-bandwidth-organic-substrates
16. A NVIDIA Hopper Architecture In-Depth. Nvidia · 22 March 2022
developer.nvidia.com/blog/nvidia-hopper-architecture-in-depth/
17. A Foveros Direct 3D Technology Brief. Intel · 6 February 2026
www.intel.com/content/dam/www/central-libraries/us/en/documents/2025-11/foveros-direct-3d-tech-brief.pdf
18. A [Tech Note] Hybrid Bonding: Evolving into a Foundational Technology for Improving Semiconductor Performance. SK hynix · 25 August 2026
news.skhyunix.com/en/tech-note-series-ep2/
19. A TSMC, CoWoS technology page. TSMC · Accessed 9 September 2026
3dfabric.tsmc.com/english/dedicatedFoundry/technology/cowos.htm
20. A TSMC 2025 Annual Report, chapter 5. TSMC · 16 April 2026 · p. 3
investor.tsmc.com/static/annualReports/2025/english/pdf/2025_tsmc_ar_e_ch5.pdf#page=3
21. B Nvidia's Blackwell Reworked - Shipment Delays & GB200A Reworked Platforms. SemiAnalysis · 4 August 2024
semanalysis.com/2024/08/04/nvidias-blackwell-reworked-shipment/
22. B Hybrid Bonding Process Flow - Advanced Packaging Part 5. SemiAnalysis · 9 February 2024
newsletter.semanalysis.com/p/hybrid-bonding-process-flow-advanced
23. A TSMC 2022 Annual Report, page 97. TSMC · Accessed 18 October 2026
investor.tsmc.com/static/annualReports/2022/english/ebook/files/basic-html/page97.html
24. A Q2 2024 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 18 July 2024 · p. 6
investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2024-08/5122725a56670882d777a8e8bfe0ed247cc55330/TSMC%202Q24%20Transcript.pdf#page=6
25. A Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 October 2025 · p. 7
investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2025-10/6860312f04fd291d0f26b46c1234f84e6332717e/TSMC%203Q25%20Transcript.pdf#page=7
26. A Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. LSEG StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 July 2026 · p. 17
investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897aa044415e21d93486cc4/TSMC%202Q26%20Transcript.pdf#page=17
27. A Applied Materials, Kinex integrated die-to-wafer hybrid bonding system product page. Applied Materials · Accessed 9 September 2026
www.appliedmaterials.com/eu/en/product-library/kinex-integrated-die-to-wafer-hybrid-bonding-system.html
28. A Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N69&selectedNode=N71
29. A TSMC Announces Additional \$100 Billion Investment in Arizona. Arizona Commerce Authority · 16 July 2026
www.azcommerce.com/news-events/news/2026/7/tsmc-announcement/
30. A Amkor Technology, annual report on Form 10-K for the fiscal year ended 31 December 2025. U.S. Securities and Exchange Commission (filing by Amkor Technology) · 20 February 2026
www.sec.gov/Archives/edgar/data/1047127/000104712726000014/amkr-20251231.htm
31. A Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 October 2025 · p. 13
investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2025-10/6860312f04fd291d0f26b46c1234f84e6332717e/TSMC%203Q25%20Transcript.pdf#page=13
32. A JCET Accelerates Strategic Shift Toward High-End Advanced Packaging, 2025 Advanced Packaging Revenue Hits Record High. JCET Group · 21 April 2026
www.jcetglobal.com/en/site/news-detail?id=2052
33. A TSMC 2025 Annual Report, chapter 5. TSMC · 16 April 2026 · p. 4
investor.tsmc.com/static/annualReports/2025/english/pdf/2025_tsmc_ar_e_ch5.pdf#page=4



01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Substrates and PCBs

Ajinomoto, a Japanese food company, told investors in June 2026 that its build-up film, the insulation inside high-end chip packages, has held over 95 percent of its market since its launch.

Specimen 11 · Substrates and PCBs

A build-up substrate, the board a chip sits on, with a quarter cut away. It is about 100 by 72 mm and 1.5 mm thick, with eighteen copper layers inside. The olive-green bands are the build-up film between the copper layers. The footprint is to scale, but the thickness is exaggerated about twenty times.

In plain terms

A package substrate is the adapter between a chip and the circuit board under it. The chip's connections are finer than a human hair, but the board is wired in millimeters. The substrate is built in layers, like plywood, around a stiff core of glass cloth and resin. Thin sheets of epoxy film are pressed onto both faces of the core. A laser burns holes through each sheet, and copper plated into the holes carries signals from one layer to the next. Every added layer is another set of holes that can fail. A handful of firms build these substrates, and two of the materials inside them come mainly from Japanese makers. Ajinomoto dominates the film, and Nitto Boseki dominates the low-expansion glass cloth in the core.

In short

Ajinomoto's third site for making its build-up film, in Gifu Prefecture, is scheduled to start operating in 2032 to meet demand after 2030¹. Nitto Boseki says market demand seems to have risen about two to three times since it set its plan for fiscal 2024 to 2027². In January 2026 Nikkei Asia reported that Apple and Qualcomm were among the customers worried about Japanese glass cloth supply³. In August 2026 Ibiden said it had prospects of a third and fourth glass cloth supplier and expected its material procurement risks to decrease⁴.

The silicon interposer wires chips together inside a package. Beyond the interposer, the wiring runs through a build-up substrate made of epoxy

¹ Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto, 30 June 2026, p. 20. ajinomoto.co.jp

² Nittobo Group Integrated Report 2025. Nitto Boseki (Nittobo), 16 September 2025, p. 4. nittobo.co.jp

³ Apple and Qualcomm fret over strained supplies of Japan's glass cloth. Nikkei Asia, 14 January 2026. asia.nikkei.com

⁴ Ibiden, questions and answers from the financial presentation for the first... Ibiden, 5 August 2026. ibiden.com

and glass, then a printed circuit board that can have more than 30 layers, then a server rack⁵.

Chokepoint card		Substrates and PCBs	
<div>Concentration</div> <div> Extreme</div> <div>Three or fewer firms could supply this stage today, or one firm holds more than half of it.</div>		<div>Substitutability</div> <div>Hard</div> <div>Rated on the insulating film inside the substrate, because chipmakers and device makers would have to approve any rival film before substrate makers could use it⁶.</div>	
		<div>Price or market size</div> <div>\$7.5 billion</div> <div>market for FC-BGA substrates in 2025, up 18 percent, in a Prismark estimate cited by AT&S⁷</div>	
Who leads	JP	Ajinomoto	Told investors in June 2026 that its build-up film has held over 95 percent of its market since its launch ⁸
	JP	Nitto Boseki	Claimed an overwhelming advantage in low thermal expansion glass in its 2025 integrated report ²
	JP	Ibiden	Said in May 2026 that it typically takes close to 100 percent of each new generation of interposer-type substrates at launch ⁹
	TW	Unimicron	Build-up substrates were 52 percent of sales in Q2 2026 ¹⁰
	KR	Samsung Electro-Mechanics	Package solution sales KRW 771.6bn in Q2 2026, up 37 percent ¹¹
Where it is made	JP	Japan	Build-up film, low-expansion glass cloth, Ibiden and Shinko substrate plants in Gifu and Nagano
	TW	Taiwan	Unimicron and Nan Ya PCB, substrate makers that sell to outside customers
	KR	South Korea	Samsung Electro-Mechanics and a planned glass-core joint venture with Sumitomo Chemical's Dongwoo Fine-Chem
	CN	China	Most of TTM's circuit board competitors are based in China and Taiwan
	AT	Austria	AT&S
Why substitution is slow	Ajinomoto makes the thin insulating film between the substrate's wiring layers ¹² . Chipmakers and device makers approve substrate materials such as laminate, so a rival film would need their approval too ⁶ .		
Where China stands		Where the US stands	
TTM, an American circuit board maker, said in its annual report for 2025 that its circuit board competitors are mostly based in China and Taiwan ⁵ . Nitto Boseki, a Japanese glass fiber maker, said in its 2025 integrated report that Chinese and Taiwanese companies are aggressively catching up with it in the special glass sector ² .		The White House's 2021 supply chain review listed no American firm among the key substrate makers ¹³ . In December 2024 the US Commerce Department finalized an award of up to \$75 million to Absolics, an affiliate of Korea's SKC, for a glass substrate plant in Covington, Georgia ¹⁴ .	

2

Nittobo Group Integrated Report 2025. Nitto Boseki (Nittobo), 16 September 2025, p. 4. nittobo.co.jp

5

TTM Technologies, annual report on Form 10-K for the fiscal year ended 29... U.S. Securities and Exchange Commission, 17 February 2026. sec.gov

6

Electronics Materials Business (Mitsubishi Gas Chemical business briefing). Mitsubishi Gas Chemical, 2 October 2024, p. 12. mgc.co.jp

7

AT&S Annual Report 2025/26. AT&S, 10 June 2026, p. 33. ats.net

8

Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto, 30 June 2026, p. 3. ajinomoto.co.jp

9

Ibiden, questions and answers from the financial presentation for the year... Ibiden, 12 May 2026. ibiden.com

10

Unimicron 2026 Q2 Earnings Conference. Unimicron Technology, July 2026. unimicron.com

11

Samsung Electro-Mechanics, Q2 2026 business results. Samsung Electro-Mechanics, 30 July 2026. m.samsungsem.com

12

Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto, 30 June 2026, p. 9. ajinomoto.co.jp

13

Building Resilient Supply Chains, Revitalizing American Manufacturing, and... The White House (Biden administration archive), June 2021, p. 43. bidenwhitehouse.archives.gov

14

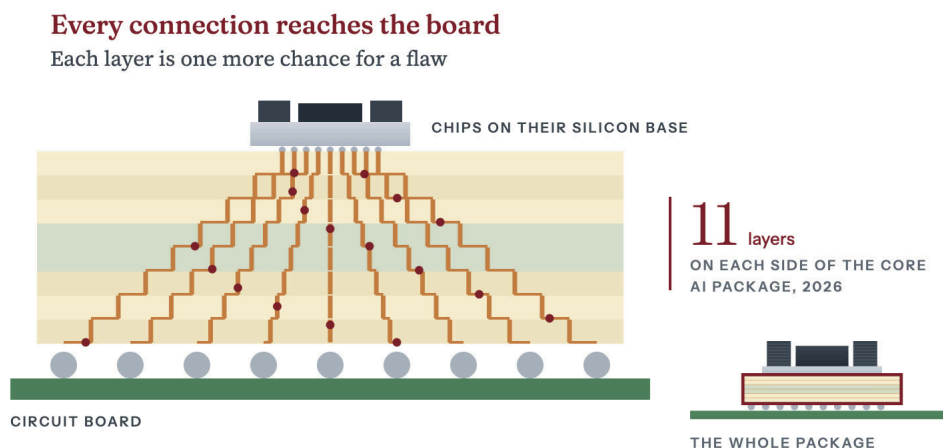
Biden-Harris Administration Announces CHIPS Incentives Awards with Absolics and... NIST, 5 December 2024. nist.gov

01

How a package substrate is built

Figure 11.1 · Explainer, 22 seconds

How a substrate fans out



1. **The package.** An AI chip is more than the chip itself. It sits in a package: the chips on a silicon base, and under them the substrate, which connects everything to the circuit board.
2. **Tight to wide.** The connections on top are packed tight. The circuit board below is wired in millimeters. The substrate has to join the two.
3. **Layer by layer.** The substrate does it in layers, built outward from a stiff core. Each layer carries the copper a little further out.
4. **Connected.** Stacked together, the layers fan the tight grid out to the board's wide one. Ajinomoto counts 11 layers of its film on each side of the core in a 2026 AI package substrate, against three on each side for a PC in 1999. Every layer is another chance for a flaw, which is what makes these substrates hard to build.

Note: Simplified. Three layers of film are drawn on each side of the core, and every thickness is exaggerated.

The substrate maker drills the core and plates it with copper before the build-up starts. In each cycle the maker then presses on a film of epoxy, burns holes through it with a laser to connect the layers, and adds copper wiring on top¹⁵. Each film is about 10 micrometers thick, and a human hair is about 80 micrometers across¹⁶.

Substrates for AI chips are larger and carry more layers of film than older ones. Ajinomoto counts 11 layers of its film on each side of the core in a 2026 AI package substrate about 100 mm square¹⁷. A high-performance computing substrate about 70 mm square had nine on each side around 2023¹⁷. PC substrates had three layers of the film on each side when PCs first adopted it in 1999¹⁷.

Silicon and epoxy expand at different rates when heated, so the larger the package, the more it warps. Nitto Boseki says its low-expansion T-glass cloth is highly rated as an

¹⁵ Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto, 30 June 2026, p. 18. ajinomoto.co.jp

¹⁶ The Ajinomoto Group's Unexpected Role in Semiconductor Manufacturing: The... Ajinomoto, 5 March 2026. ajinomoto.com

¹⁷ Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto, 30 June 2026, p. 11. ajinomoto.co.jp

effective fix for that warping¹⁸. It says use of the cloth in substrates has increased significantly, without giving a figure¹⁸.

02

Types of package substrates

BT substrates

Substrates built on bismaleimide-triazine laminate, or BT, are the other main family. Mitsubishi Gas Chemical, which makes BT materials, says they go mostly into thin packages for smartphone processors, radio modules and memory¹⁹. The company says BT also goes into flip-chip substrates for computer CPUs and GPUs¹⁹. In these the chip is mounted face down, and BT laminate also serves as the core of a build-up substrate, between layers of build-up film²⁰. In an October 2024 investor presentation, the company estimated that its BT resins held about 40 percent of what it calls the substrate materials market, the top share²¹.

ABF build-up substrates

One company, Ajinomoto, supplies nearly all the insulating film inside package substrates for logic chips. Ajinomoto Build-up Film, or ABF, is the insulating film between the layers of package substrates for logic chips, used in PCs, network equipment, servers and AI equipment¹². Ajinomoto first developed it in 1999 and says major chipmakers have used it as the de facto standard ever since²². On Ajinomoto's own site, its electronic materials division said practically all high-performance computers and servers rely on the film¹⁶. In June 2026 Ajinomoto told investors that the film has held over 95 percent of its market since its launch⁸.

8 Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto, 30 June 2026, p. 3. ajinomoto.co.jp

12 Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto, 30 June 2026, p. 9. ajinomoto.co.jp

16 The Ajinomoto Group's Unexpected Role in Semiconductor Manufacturing: The... Ajinomoto, 5 March 2026. ajinomoto.com

18 Nittobo Group Integrated Report 2025. Nitto Boseki (Nittobo), 16 September 2025, p. 17. nittobo.co.jp

19 Electronics Materials Business (Mitsubishi Gas Chemical business briefing). Mitsubishi Gas Chemical, 2 October 2024, p. 16. mgc.co.jp

20 Electronics Materials Business (Mitsubishi Gas Chemical business briefing). Mitsubishi Gas Chemical, 2 October 2024, p. 18. mgc.co.jp

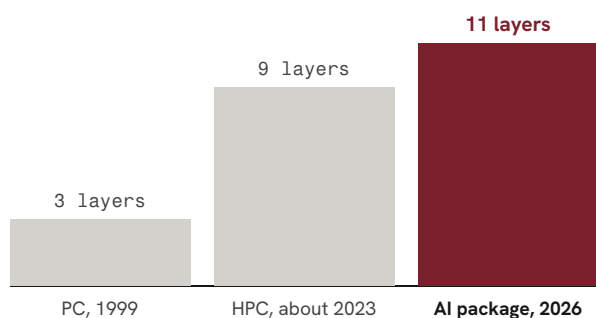
21 Electronics Materials Business (Mitsubishi Gas Chemical business briefing). Mitsubishi Gas Chemical, 2 October 2024, p. 11. mgc.co.jp

22 Ajinomoto, Business Briefing: ABF-Based Growth Strategy in ICT, 12 June 2023. Ajinomoto, 12 June 2023, p. 4. ajinomoto.co.jp

Figure 11.2

Substrate film layers rose from 3 in 1999 to 11 in 2026

Layers of build-up film on each side of a package substrate's core



Source: Ajinomoto, Growth Strategy for the Electronic Materials Business, June 2026 [17]

Glass core substrates

A glass core expands less with heat than a resin core and stays flatter, so chipmakers and substrate makers are both trying it²³.

- **Absolics**, a subsidiary of Korea's SKC, has a final US Commerce Department award of up to \$75 million for a 120,000-square-foot glass substrate plant in Covington, Georgia²⁴. The department finalized the award in December 2024¹⁴. As of October 2026, the award's project page at NIST, a Commerce Department agency, still said first deliveries to customers were expected in 2025 and production capacity in 2027, without saying whether those deliveries had happened²⁴.
- **Intel** said in September 2023 that it planned glass substrates for the latter part of the 2020s²⁵.
- **Samsung Electro-Mechanics** signed a joint venture agreement with Sumitomo Chemical's subsidiary Dongwoo Fine-Chem in July 2026 to make glass core substrates²⁶. The partners plan to have a supply system in place by the second half of fiscal 2027²⁶.

03

Ajinomoto's film and Nitto Boseki's glass cloth

Ajinomoto's electronic materials revenue is rising, and it is adding film capacity, but its third production site is not scheduled to open until 2032. Ajinomoto's Healthcare and Others segment, which includes electronic materials such as the film, lifted business profit 45.1 percent to JPY 66.2 billion in the year to March 2026²⁷. Ajinomoto attributes the rise mainly to higher electronic materials revenue and higher profit in Bio-Pharma Services & Ingredients²⁷. It has set an investment budget of JPY 25 billion

14 Biden-Harris Administration Announces CHIPS Incentives Awards with Absolics and... NIST, 5 December 2024. [nist.gov](https://www.nist.gov)

17 Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto, 30 June 2026, p. 11. ajinomoto.co.jp

23 Samsung Electro-Mechanics Signs MOU with Sumitomo Chemical Group to Establish a... Samsung Electro-Mechanics, 5 November 2025. samsungsem.com

24 Absolics (Georgia). NIST, 5 July 2024. [nist.gov](https://www.nist.gov)

25 Intel Unveils Industry-Leading Glass Substrates to Meet Demand for More... Intel, 18 September 2023. download.intel.com

26 Sumitomo Chemical Subsidiary to Establish a Joint Venture with Samsung... Sumitomo Chemical, 2 July 2026. sumitomo-chem.co.jp

27 Consolidated Financial Results for the Fiscal Year Ended March 31, 2026 (Under... Ajinomoto, 7 May 2026, p. 8. ajinomoto.co.jp

between 2023 and 2030 to expand film production²⁸. It says it has no concerns about its current supply chain overall and will steadily expand its supply capacity over the medium to long term⁸. In May 2026 it announced the acquisition of land in Gifu Prefecture for a third production site, scheduled to start operating in 2032 to meet demand after 2030¹.

The glass cloth in the core also has a dominant supplier. Nitto Boseki's T-glass is stiff and expands little when heated, and the company calls it essential for making high-density package substrates²⁹. Laminate makers such as Mitsubishi Gas Chemical coat the glass cloth with resin and press it with copper foil into the core laminate that substrate makers build on³⁰.

Nitto Boseki says market demand seems to have risen about two to three times since it set its plan for fiscal 2024 to 2027². That plan included about JPY 80 billion of capital spending³¹. The company claims an overwhelming advantage in quality and capacity for low-expansion glass². In August 2025 it decided to expand glass fiber cloth production at its Fukushima Enterprise Center, with production scheduled to begin in the fourth quarter of its fiscal 2026³². In May 2026 it forecast capital investment of JPY 45,000 million for the year to March 2027, up from JPY 21,702 million in the year to March 2026³³.

In January 2026 Nikkei Asia reported that Apple and Qualcomm were among the customers worried about Japanese glass cloth supply³. In August 2026 Ibidem, a Japanese substrate maker, said it had used only two glass cloth suppliers, in Japan and Taiwan, but now had prospects of a third and fourth for mass production⁴. Because a Japanese supplier, which Ibidem did not name, also plans to add capacity, Ibidem said it expected its material procurement risks to decrease⁴.

Nitto Boseki says Chinese and Taiwanese companies are aggressively catching up with it in the special glass sector². In July 2026 Nikkei Asia reported that Chinese chip materials makers were competing with Japanese rivals in the market for chip materials, which the industry association SEMI put at \$73.2 billion in 2025³⁴.

04

Who makes package substrates

Most of the firms that build substrates for others are Asian. The White House's 2021 hundred-day supply chain review listed build-up substrate among the materials that commenters called vulnerable³⁵. It named key substrate makers including Ibidem,

1 Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto, 30 June 2026, p. 20. ajinomoto.co.jp

2 Nittobo Group Integrated Report 2025. Nitto Boseki (Nittobo), 16 September 2025, p. 4. nittobo.co.jp

3 Apple and Qualcomm fret over strained supplies of Japan's glass cloth. Nikkei Asia, 14 January 2026. asia.nikkei.com

4 Ibidem, questions and answers from the financial presentation for the first... Ibidem, 5 August 2026. ibidem.com

8 Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto, 30 June 2026, p. 3. ajinomoto.co.jp

28 Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto, 30 June 2026, p. 21. ajinomoto.co.jp

29 Nittobo Group Integrated Report 2025. Nitto Boseki (Nittobo), 16 September 2025, p. 3. nittobo.co.jp

30 Electronics Materials Business (Mitsubishi Gas Chemical business briefing). Mitsubishi Gas Chemical, 2 October 2024, p. 28. mgc.co.jp

31 Nittobo Group Integrated Report 2025. Nitto Boseki (Nittobo), 16 September 2025, p. 5. nittobo.co.jp

32 Nittobo Group Integrated Report 2025. Nitto Boseki (Nittobo), 16 September 2025, p. 12. nittobo.co.jp

33 Consolidated Financial Results for the Fiscal Year Ended March 31, 2026. Nitto Boseki (Nittobo), 12 May 2026, p. 5. ssl4.eir-parts.net

34 China chip material makers battle Japan rivals for \$73bn market. Nikkei Asia, 1 July 2026. asia.nikkei.com

35 Building Resilient Supply Chains, Revitalizing American Manufacturing, and... The White House (Biden administration archive), June 2021, p. 45. bidenwhitehouse.archives.gov

Nanya, Shinko, Samsung, Unimicron, Shennan Circuits, Zhuhai Yueya and AKM, none of them American¹³.

A May 2024 report by the Semiconductor Industry Association and Boston Consulting Group found that every major package substrate vendor was headquartered in Japan, Taiwan or mainland China³⁶. It counted two in Japan, two in Taiwan, one in mainland China and none in the United States³⁶. But TTM Technologies, an American circuit board maker, says it offers package substrates too⁵.

- **Ibiden** will invest about JPY 500 billion in high-performance package substrates from fiscal 2026 to fiscal 2028, starting with about JPY 220 billion, mainly at its Gama plant in Gifu Prefecture³⁷. In August 2026 it said the Gama plant was scheduled to start operating in stages from the end of fiscal 2027 and to add to its results from fiscal 2028⁴. In May 2026 management said Ibiden typically takes close to 100 percent of each new generation of what it calls interposer-type substrates at launch⁹. It added that this share may decline by 20 to 30 percent after about three to six months⁹. On silicon-bridge substrates, it said wiring the underside is hard enough that Ibiden expects to keep its technical lead at least through fiscal 2030⁹.
- **Unimicron** reported NT\$42.9 billion of sales in the second quarter of 2026¹⁰. By technology, 52 percent came from build-up substrates, and by application, 61 percent came from AI data center work¹⁰.
- **Samsung Electro-Mechanics** grew package solution sales 37 percent year on year to KRW 771.6 billion in the second quarter of 2026, on substrates for AI accelerators, server processors and cars¹¹.
- **AT&S**, an Austrian firm, calls itself a globally leading maker of high-end package substrates³⁸. It makes them in China and Malaysia, and since its 2025/26 financial year also in Austria³⁹. Citing the research firm Prismark, its annual report for 2025/26 valued the market for flip-chip ball grid array (FC-BGA) substrates at \$7.5 billion in 2025, up 18 percent from 2024⁷.

In February 2025 a company owned mainly by funds of JIC Capital launched a tender offer to take Shinko, a Japanese substrate maker, private⁴⁰. JIC Capital is a wholly owned subsidiary of Japan Investment Corporation, an investment company set up in September 2018 under Japan's Industrial Competitiveness Enhancement Act to pursue policy goals such as stronger industrial competitiveness⁴¹. Fujitsu, which owned 50.02

4 Ibiden, questions and answers from the financial presentation for the first... Ibiden, 5 August 2026. [ibiden.com](https://www.ibiden.com)

5 TTM Technologies, annual report on Form 10-K for the fiscal year ended 29... U.S. Securities and Exchange Commission, 17 February 2026. [sec.gov](https://www.sec.gov)

7 AT&S Annual Report 2025/26. AT&S, 10 June 2026, p. 33. [ats.net](https://www.ats.net)

9 Ibiden, questions and answers from the financial presentation for the year... Ibiden, 12 May 2026. [ibiden.com](https://www.ibiden.com)

10 Unimicron 2026 Q2 Earnings Conference. Unimicron Technology, July 2026. [unimicron.com](https://www.unimicron.com)

11 Samsung Electro-Mechanics, Q2 2026 business results. Samsung Electro-Mechanics, 30 July 2026. [m.samsungsem.com](https://www.m.samsungsem.com)

13 Building Resilient Supply Chains, Revitalizing American Manufacturing, and... The White House (Biden administration archive), June 2021, p. 43. [bidenwhitehouse.archives.gov](https://www.bidenwhitehouse.archives.gov)

36 Emerging Resilience in the Semiconductor Supply Chain. Boston Consulting Group and Semiconductor Industry..., May 2024, p. 19. [semiconductors.org](https://www.semiconductors.org)

37 Ibiden, Notice Regarding Capital Investment Plan for High-Performance IC... Ibiden, 3 February 2026. [ibiden.com](https://www.ibiden.com)

38 AT&S Annual Report 2025/26. AT&S, 10 June 2026, p. 67. [ats.net](https://www.ats.net)

39 AT&S Annual Report 2025/26. AT&S, 10 June 2026, p. 53. [ats.net](https://www.ats.net)

40 Announcement Regarding Commencement of the Tender Offer for the Shares of... Japan Investment Corporation, 17 February 2025, p. 1. [jiccapital.co.jp](https://www.jiccapital.co.jp)

41 Announcement Regarding Commencement of the Tender Offer for the Shares of... Japan Investment Corporation, 17 February 2025, p. 17. [jiccapital.co.jp](https://www.jiccapital.co.jp)

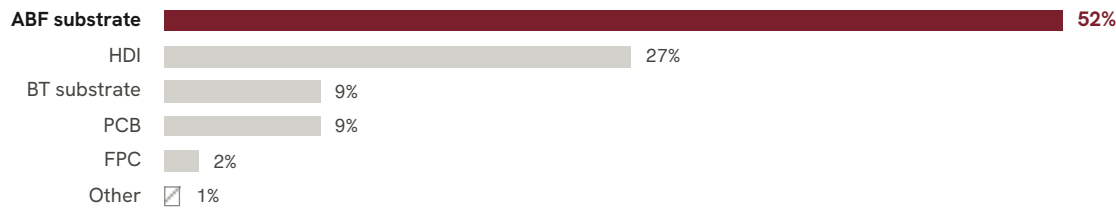
percent of Shinko, agreed to sell that stake back to Shinko, and the offer covered the shares Fujitsu did not own⁴². The tender offer succeeded in March 2025⁴³.

In September 2026 Shinko agreed to buy a plant in Mobara, Chiba Prefecture, from Japan Display, a display maker⁴⁴. Shinko said it would make the site a new core plant for its flip-chip package substrates and would also expand capacity at its plants in Nagano⁴⁴. Production at the Mobara plant is scheduled to start in fiscal 2028⁴⁴.

Figure 11.3

ABF substrates were 52 percent of Unimicron's second-quarter 2026 sales

Unimicron sales by technology, second quarter 2026



Source: Unimicron 2026 Q2 earnings conference [10]

05

Printed circuit boards for AI data centers

TTM Technologies says it regularly builds printed circuit boards of more than 30 layers and can go past 70⁵. Those layers carry power to the GPUs and route fast signals between them, so how much signal the laminate absorbs is a main design constraint. Nitto Boseki also makes NE-glass, a low-dielectric glass cloth that absorbs less signal, used in switches and routers in data centers⁴⁵.

Data center computing was 24 percent of TTM's fiscal 2025 revenue of about \$2.9 billion, against 14 percent two years earlier⁵.

Board makers are adding plants outside China and Taiwan, where TTM says most of its circuit board competitors are based⁵. In its annual report for 2025, TTM said it was building a plant in Syracuse, New York, to make ultra-high-density circuit boards for national security needs⁵. It expected volume production there in the second half of 2026⁵. Nikkei Asia reported in September 2025 that Thailand aimed to become the biggest circuit board hub outside China as board makers moved to diversify production⁴⁶.

5 TTM Technologies, annual report on Form 10-K for the fiscal year ended 29... U.S. Securities and Exchange Commission, 17 February 2026. sec.gov

10 Unimicron 2026 Q2 Earnings Conference. Unimicron Technology, July 2026. unimicron.com

42 Announcement Regarding Commencement of the Tender Offer for the Shares of... Japan Investment Corporation, 17 February 2025, p. 3. jiccapital.co.jp

43 (Progress Report on Disclosed Matters) Notice Regarding Completion of JICC-04's... Fujitsu, 19 March 2025. pr.fujitsu.com

44 Notice Concerning the Acquisition of Japan Display Inc.'s Mobara Fab. Shinko Electric Industries, 30 September 2026. shinko.co.jp

45 Nittobo Group Integrated Report 2025. Nitto Boseki (Nittobo), 16 September 2025, p. 7. nittobo.co.jp

46 Thailand carves out a less-glamorous AI niche: printed circuit boards. Nikkei Asia, 3 September 2025. asia.nikkei.com

06

Why substrate supply is hard to expand

The few firms that build substrates are spending to add capacity, but it takes years. In August 2026 Ibiden said that, with supply short across the industry, the average price of package substrates had risen more than it expected⁴. The materials inside the substrate are harder to replace than the firms that build it. Mitsubishi Gas Chemical, a laminate maker, says chipmakers and electronic device makers further down the chain approve the materials it sells to substrate makers⁶. So a rival to Ajinomoto's film or to Nitto Boseki's low-expansion glass cloth would first need approval from those chipmakers and device makers.

Packages are also getting bigger. TSMC told investors in July 2026 that its CoWoS packaging roadmap goes beyond 14 times the area a lithography machine can print in one shot⁴⁷. A bigger package warps more and needs more layers, so it has more holes that can break the circuit. That lowers yield, the share of substrates that come out working.

Four questions to answer from memory

1. What does a package substrate do? see How it works
 2. How is a substrate built? see How it works
 3. Which company makes nearly all the insulating film in substrates?
see ABF build-up substrates
 4. Why is Ajinomoto's film hard to replace? see Chokepoint card
-

Four things to remember

- A package substrate connects a chip's fine contacts to a circuit board wired in millimeters.
 - One Japanese supplier leads the market for the substrate's insulating film, and another leads the market for its glass cloth.
 - Replacing the film would mean re-approval by every substrate maker and chip customer.
 - The White House's 2021 supply chain review named no American firm among the key substrate makers. Absolics is building a glass substrate plant in Georgia, and a Commerce Department agency expects its production capacity to come online in 2027.
-

⁴ Ibiden, questions and answers from the financial presentation for the first... Ibiden, 5 August 2026. [ibiden.com](https://www.ibiden.com)

⁶ Electronics Materials Business (Mitsubishi Gas Chemical business briefing). Mitsubishi Gas Chemical, 2 October 2024, p. 12. [mgc.co.jp](https://www.mgc.co.jp)

⁴⁷ Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese... LSEG StreetEvents, 16 July 2026, p. 16. investor.tsmc.com

Sources (47)

1. A **Ajinomoto, Growth Strategy for the Electronic Materials Business**, 30 June 2026. Ajinomoto · 30 June 2026 · p. 20
www.ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList/03/link/20260630_presentation_E.pdf#page=20
2. A **Nittobo Group Integrated Report 2025**. Nitto Boseki (Nittobo) · 16 September 2025 · p. 4
www.nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf#page=4
3. B **Apple and Qualcomm fret over strained supplies of Japan's glass cloth**. Nikkei Asia · 14 January 2026
asia.nikkei.com/business/technology/tech-asia/apple-and-qualcomm-fret-over-strained-supplies-of-japan-s-glass-cloth
4. A **Ibiden, questions and answers from the financial presentation for the first quarter of the year ending 31 March 2027**. Ibiden · 5 August 2026
www.ibiden.com/ir/items/en_QA_FY2026Q1.pdf
5. A **TTM Technologies, annual report on Form 10-K for the fiscal year ended 29 December 2025**. U.S. Securities and Exchange Commission (filing by TTM Technologies) · 17 February 2026
www.sec.gov/Archives/edgar/data/1116942/000119312526051976/ttmi-20251229.htm
6. A **Electronics Materials Business (Mitsubishi Gas Chemical business briefing)**. Mitsubishi Gas Chemical · 2 October 2024 · p. 12
www.mgc.co.jp/eng/ir/files/2410022e.pdf#page=12
7. A **AT&S Annual Report 2025/26**. AT&S · 10 June 2026 · p. 33
ats.net/en/download/annual-report-2025-26/?wpdmdl=61788#page=33
8. A **Ajinomoto, Growth Strategy for the Electronic Materials Business**, 30 June 2026. Ajinomoto · 30 June 2026 · p. 3
www.ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList/03/link/20260630_presentation_E.pdf#page=3
9. A **Ibiden, questions and answers from the financial presentation for the year ended 31 March 2026**. Ibiden · 12 May 2026
www.ibiden.com/ir/items/en_QA_FY25Q4.pdf
10. A **Unimicron 2026 Q2 Earnings Conference**. Unimicron Technology · July 2026
www.unimicron.com/files/money/Earnings/en/2026-Q2-consolidated-en.pdf
11. A **Samsung Electro-Mechanics, Q2 2026 business results**. Samsung Electro-Mechanics · 30 July 2026
m.samsungsem.com/global/newsroom/news/view.do?id=10462
12. A **Ajinomoto, Growth Strategy for the Electronic Materials Business**, 30 June 2026. Ajinomoto · 30 June 2026 · p. 9
www.ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList/03/link/20260630_presentation_E.pdf#page=9
13. A **Building Resilient Supply Chains, Revitalizing American Manufacturing, and Fostering Broad-Based Growth: 100-Day Reviews under Executive Order 14017**. The White House (Biden administration archive) · June 2021 · p. 43
bidenwhitehouse.archives.gov/wp-content/uploads/2021/06/100-day-supply-chain-review-report.pdf#page=43
14. A **Biden-Harris Administration Announces CHIPS Incentives Awards with Absolics and Entegris to Support Development of Advanced Packaging Technology and Onshore Material for Leading-Edge Chip Production**. NIST · 5 December 2024
www.nist.gov/news-events/news/2024/12/biden-harris-administration-announces-chips-incentives-awards-absolics-and
15. A **Ajinomoto, Growth Strategy for the Electronic Materials Business**, 30 June 2026. Ajinomoto · 30 June 2026 · p. 18
www.ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList/03/link/20260630_presentation_E.pdf#page=18
16. A **The Ajinomoto Group's Unexpected Role in Semiconductor Manufacturing: The Insulating Film “ABF” Born from “AminoScience”**. Ajinomoto · 5 March 2026
www.ajinomoto.com/stories/the-ajinomoto-groups-unexpected-role-in-semiconductor-manufacturing-the-insulating-film-abf-born-from-aminoscience
17. A **Ajinomoto, Growth Strategy for the Electronic Materials Business**, 30 June 2026. Ajinomoto · 30 June 2026 · p. 11
www.ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList/03/link/20260630_presentation_E.pdf#page=11
18. A **Nittobo Group Integrated Report 2025**. Nitto Boseki (Nittobo) · 16 September 2025 · p. 17
www.nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf#page=17
19. A **Electronics Materials Business (Mitsubishi Gas Chemical business briefing)**. Mitsubishi Gas Chemical · 2 October 2024 · p. 16
www.mgc.co.jp/eng/ir/files/2410022e.pdf#page=16
20. A **Electronics Materials Business (Mitsubishi Gas Chemical business briefing)**. Mitsubishi Gas Chemical · 2 October 2024 · p. 18
www.mgc.co.jp/eng/ir/files/2410022e.pdf#page=18
21. A **Electronics Materials Business (Mitsubishi Gas Chemical business briefing)**. Mitsubishi Gas Chemical · 2 October 2024 · p. 11
www.mgc.co.jp/eng/ir/files/2410022e.pdf#page=11
22. A **Ajinomoto, Business Briefing: ABF-Based Growth Strategy in ICT**, 12 June 2023. Ajinomoto · 12 June 2023 · p. 4
www.ajinomoto.co.jp/company/en/ir/event/business_briefing/main/01113/teaserItems1/01/linkList/00/link/3_ICT_E.pdf#page=4
23. A **Samsung Electro-Mechanics Signs MOU with Sumitomo Chemical Group to Establish a Joint Venture for Glass Core Used in Package Substrates**. Samsung Electro-Mechanics · 5 November 2025
samsungsem.com/global/newsroom/news/view.do?id=9850

24. A **Absolics (Georgia).** NIST · 5 July 2024
www.nist.gov/chips/absolics-georgia-covington
25. A **Intel Unveils Industry-Leading Glass Substrates to Meet Demand for More Powerful Compute.** Intel · 18 September 2023
download.intel.com/newsroom/archive/2025/en-us-2023-09-18-intel-unveils-industry-leading-glass-substrates-to-meet-demand-for-more-powerful-compute.pdf
26. A **Sumitomo Chemical Subsidiary to Establish of a Joint Venture with Samsung Electro-Mechanics for the Glass Core Substrate Business.** Sumitomo Chemical · 2 July 2026
www.sumitomo-chem.co.jp/english/news/detail/20260702e_2.html
27. A **Consolidated Financial Results for the Fiscal Year Ended March 31, 2026 (Under IFRS).** Ajinomoto · 7 May 2026 · p. 8
www.ajinomoto.co.jp/company/en/ir/library/result/main/014/teaserItems1/0/linkList/06/link/FY25Q4_Tanshin_E.pdf#page=8
28. A **Ajinomoto, Growth Strategy for the Electronic Materials Business,** 30 June 2026. Ajinomoto · 30 June 2026 · p. 21
www.ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList/03/link/20260630_presentation_E.pdf#page=21
29. A **Nittobo Group Integrated Report 2025.** Nitto Boseki (Nittobo) · 16 September 2025 · p. 3
www.nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf#page=3
30. A **Electronics Materials Business (Mitsubishi Gas Chemical business briefing).** Mitsubishi Gas Chemical · 2 October 2024 · p. 28
www.mgc.co.jp/eng/ir/files/2410022e.pdf#page=28
31. A **Nittobo Group Integrated Report 2025.** Nitto Boseki (Nittobo) · 16 September 2025 · p. 5
www.nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf#page=5
32. A **Nittobo Group Integrated Report 2025.** Nitto Boseki (Nittobo) · 16 September 2025 · p. 12
www.nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf#page=12
33. A **Consolidated Financial Results for the Fiscal Year Ended March 31, 2026.** Nitto Boseki (Nittobo) · 12 May 2026 · p. 5
ssl4.eir-parts.net/doc/3110/ir_material_for_fiscal_ym2/202884/00.pdf#page=5
34. B **China chip material makers battle Japan rivals for \$73bn market.** Nikkei Asia · 1 July 2026
asia.nikkei.com/business/tech/semiconductors/china-chip-material-makers-battle-japan-rivals-for-73bn-market
35. A **Building Resilient Supply Chains, Revitalizing American Manufacturing, and Fostering Broad-Based Growth: 100-Day Reviews under Executive Order 14017.** The White House (Biden administration archive) · June 2021 · p. 45
bidenwhitehouse.archives.gov/wp-content/uploads/2021/06/100-day-supply-chain-review-report.pdf#page=45
36. A **Emerging Resilience in the Semiconductor Supply Chain.** Boston Consulting Group and Semiconductor Industry Association · May 2024 · p. 19
www.semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconductor-Supply-Chain.pdf#page=19
37. A **Ibiden, Notice Regarding Capital Investment Plan for High-Performance IC Package Substrates.** Ibiden · 3 February 2026
www.ibiden.com/company/2026/02/notice-regarding-capital-investment-plan-for-high-performance-ic-package-substrates.html
38. A **AT&S Annual Report 2025/26.** AT&S · 10 June 2026 · p. 67
ats.net/en/download/annual-report-2025-26/?wpdmdl=61788#page=67
39. A **AT&S Annual Report 2025/26.** AT&S · 10 June 2026 · p. 53
ats.net/en/download/annual-report-2025-26/?wpdmdl=61788#page=53
40. A **Announcement Regarding Commencement of the Tender Offer for the Shares of Shinko Electric Industries Co., Ltd. (Securities Code: 6967) by JICC-04, Ltd..** Japan Investment Corporation · 17 February 2025 · p. 1
www.jiccapital.co.jp/en/news/.assets/E_20250217_JIC_JICC_PressRelease.pdf#page=1
41. A **Announcement Regarding Commencement of the Tender Offer for the Shares of Shinko Electric Industries Co., Ltd. (Securities Code: 6967) by JICC-04, Ltd..** Japan Investment Corporation · 17 February 2025 · p. 17
www.jiccapital.co.jp/en/news/.assets/E_20250217_JIC_JICC_PressRelease.pdf#page=17
42. A **Announcement Regarding Commencement of the Tender Offer for the Shares of Shinko Electric Industries Co., Ltd. (Securities Code: 6967) by JICC-04, Ltd..** Japan Investment Corporation · 17 February 2025 · p. 3
www.jiccapital.co.jp/en/news/.assets/E_20250217_JIC_JICC_PressRelease.pdf#page=3
43. A **(Progress Report on Disclosed Matters) Notice Regarding Completion of JICC-04's Tender Offer for Shares of a Consolidated Subsidiary of Fujitsu Limited (SHINKO ELECTRIC INDUSTRIES CO., LTD.).** Fujitsu · 19 March 2025
pr.fujitsu.com/jp/news/2025/03/en/19-1.pdf
44. A **Notice Concerning the Acquisition of Japan Display Inc.'s Mobara Fab.** Shinko Electric Industries · 30 September 2026
www.shinko.co.jp/english/news/docs/20260930-01_en.pdf
45. A **Nittobo Group Integrated Report 2025.** Nitto Boseki (Nittobo) · 16 September 2025 · p. 7
www.nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf#page=7
46. B **Thailand carves out a less-glamorous AI niche: printed circuit boards.** Nikkei Asia · 3 September 2025
asia.nikkei.com/business/technology/tech-asia/thailand-carves-out-a-less-glamorous-ai-niche-printed-circuit-boards
47. A **Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript.** LSEG StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 July 2026 · p. 16
investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897aa044415e21d93486cc4/TSMC%202Q26%20Transcript.pdf#page=16



01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Test and Assembly

Testing finds bad chips before they go into an expensive package. Japan's Advantest took about 65 percent of 2025 spending on chip testers, by its own estimate.

Specimen 12 · Test and Assembly

A vertical probe card over a wafer. It is called vertical because its needles point straight down at the wafer. The card is round, about 305 mm across, a little wider than the 300 mm wafer beneath it. Thousands of needles under it land on four dies at once, and those four dies are picked out in blue-violet. The gap between card and wafer is exaggerated. The real gap is a millimeter or two.

In plain terms

Before a chip can be sold, a machine called a tester has to check that it works. While the chips are still on the wafer, thousands of needles press onto small metal pads on each one. The tester sends signals through the needles and reads what comes back, and any chip that fails goes no further. A modern AI accelerator is a dozen expensive pieces bonded into one package, and if one piece is bad, all of them are thrown away. So the industry now tests chips earlier, at higher temperatures and for longer, to make weak ones fail during testing before they reach a finished product. Two firms, Advantest in Japan and Teradyne in the United States, sell most of the testers.

In short

In a TrendForce ranking cited by CSET, four of the ten largest chip assembly and test contractors by 2024 revenue are headquartered in China¹. Georgetown's CSET, analyzing TechInsights data, finds that between 2019 and 2024 Chinese toolmakers gained 5 percentage points of world market share in test tools¹. Across assembly, test and packaging tools, they still lag significantly behind foreign suppliers in market share¹. Advantest says that switching to another tester maker means rebuilding a customer's whole test setup, at significant extra cost².

Turning silicon into a finished, packaged chip takes 1,000 to 1,500 steps, depending on how complex the chip is, the Semiconductor Industry Association estimated in 2025³. Of all those steps, only test puts electrical signals through the chip, Advantest's investor guide of July 2026 says⁴. The

1 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology, 14 July 2025. cset.georgetown.edu

2 Investors Guide July 29, 2026. Advantest, 30 July 2026, p. 12. advantest.com

3 Testimony of David Isaacs, Semiconductor Industry Association, hearing on... U.S. Senate Committee on Finance, 14 May 2025, p. 2. finance.senate.gov

4 Investors Guide July 29, 2026. Advantest, 30 July 2026, p. 10. advantest.com

earlier stages of chipmaking make dies, the individual chips on a wafer. The back end of the industry, assembly and test, checks which of them work and puts the good ones into packages.

Chokepoint card		Test and Assembly	
Concentration		Substitutability	Price or market size
 High Four to six firms could supply this stage today, and the top two take most of the revenue.		Moderate Rated on test tools, where Advantest held 62.7 percent of the market in 2025 and Teradyne 21.8 percent, by CSET's analysis of TechInsights data ⁵ .	About \$9.0 billion market for chip testers in 2025, by Advantest's estimate ⁶
Who leads	JP	Advantest	About 65 percent of the tester market in 2025, by its own estimate ⁶
	US	Teradyne	\$2.52 billion of semiconductor test revenue in 2025, service included ⁷
	TW	ASE	Ran 8,348 testers in Q2 2026, up from 6,797 a year earlier ⁸
	US	Amkor	\$6.71 billion of 2025 revenue ⁹
	JP	Disco	87 percent of the \$1.9 billion market for dicing saws and grinders in 2025, on CSET's analysis of TechInsights data ¹⁰
Where it is made	TW	Taiwan	Taiwanese firms such as ASE and Powertech lead outsourced assembly and test
	JP	Japan	Advantest testers, Accretech and Tokyo Electron probers, Disco and Accretech dicing and grinding
	US	United States	Test equipment from Teradyne, FormFactor, Cohu and Aehr, and Amkor's planned Arizona packaging plant
	CN	China	Four of the top ten assembly and test firms by 2024 revenue, in a TrendForce ranking cited by CSET
	MY	Malaysia	Malaysia said in July 2026 that it ships 13 percent of the world's packaged chips
Why substitution is possible	Customers such as ASE already buy testers from both firms ¹¹ . The barrier is cost, because switching means rebuilding a customer's whole test setup, Advantest says ² .		

2 Investors Guide July 29, 2026. Advantest, 30 July 2026, p. 12. [advantest.com](#)

5 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 20 October 2026. [chipexplorer.eto.tech](#)

6 Advantest, presentation notes for the FY2025 (year ended 31 March 2026) results... Advantest, 27 April 2026, p. 13. [advantest.com](#)

7 Teradyne, annual report on Form 10-K for the fiscal year ended 31 December 2025. U.S. Securities and Exchange Commission, 19 February 2026. [sec.gov](#)

8 ASE Technology Holding, report on Form 6-K dated 30 July 2026. U.S. Securities and Exchange Commission, 30 July 2026. [sec.gov](#)

9 Amkor Technology, current report on Form 8-K dated 9 February 2026. U.S. Securities and Exchange Commission, 9 February 2026. [sec.gov](#)

10 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. [chipexplorer.eto.tech](#)

11 ASE Technology Holding, annual report on Form 20-F for the fiscal year ended 31... U.S. Securities and Exchange Commission, 1 April 2026. [sec.gov](#)

Where China stands

Georgetown's CSET, analyzing TechInsights data, finds that between 2019 and 2024 Chinese toolmakers gained 5 percentage points of world market share in test tools and 4 points in fabrication tools built for advanced packaging¹. But they lost share in bonding and other conventional assembly and packaging tools¹.

Where the US stands

American firms held 23.5 percent of the market for test tools in 2025 and Japanese firms 63.0 percent, by CSET's analysis of TechInsights data⁵. Amkor raised its planned investment in an Arizona packaging and test campus to \$7 billion in October 2025¹². In June 2026 it announced a long-term partnership with TSMC, which will buy packaging and test services from it in Arizona¹³.

01

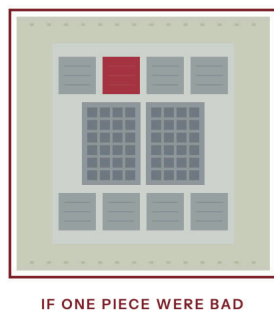
How chips are tested before they ship

Figure 12.1 · Explainer, 23 seconds

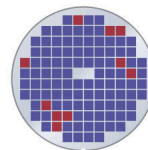
How a chip is tested

One bad piece would waste them all

So each chip is tested before it goes in



A dozen pieces
IN ONE ACCELERATOR



1. **The wafer.** Earlier stages make the chips. Before any of them can be sold, a machine tests each one, starting while the chips are still on the wafer.
2. **Needles.** Thousands of needles on a probe card press onto one chip. They touch small metal pads on its surface.
3. **Questions and answers.** Through the needles, the tester sends signals into the chip and reads what comes back. It checks every answer.
4. **Chip by chip.** The wafer moves under the needles, chip by chip. The tester marks any chip that answers wrong, and that chip goes no further.
5. **Into the package.** Only chips that pass go on to be packaged. A modern accelerator bonds together a dozen expensive pieces, and one bad piece throws away all of them, so each piece is tested before it goes in.

Note: Simplified. Nine needles stand for thousands. A real prober, the machine that moves the wafer under the card, holds the card still and raises the wafer to meet the needles. The failed chips are placed for illustration and do not reflect a real yield. The package follows chapter 10: two logic chips and eight memory stacks on an interposer and a package base.

¹ Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology, 14 July 2025. cset.georgetown.edu

⁵ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 20 October 2026. chipexplorer.eto.tech

¹² Amkor Technology Breaks Ground on New Semiconductor Advanced Packaging and Test... Amkor Technology, 6 October 2025. ir.amkor.com

¹³ TSMC and Amkor Technology Announce Long Term Partnership to Accelerate Advanced... Amkor Technology, 16 June 2026. ir.amkor.com

Each round of test catches failures the round before it cannot see.

- **Wafer sort.** Thousands of needles land on each die while it is still on the wafer. A tester sends in test patterns and checks the answers, and dies that fail go no further.
- **Burn-in.** The part runs hot and at raised voltage for minutes to days, on the wafer or in the package, so that early-life failures happen in the factory, before the part ships¹⁴.
- **Final test.** The tester checks the packaged part again, because packaging adds failures of its own.
- **System-level test.** The finished part sits in a socket and runs something close to a real workload, because some failures appear only when everything runs at once.

As the parts in a package grow more valuable, finding a bad die before packaging matters more¹⁵. Aehr, an American maker of burn-in equipment, sells wafer-level burn-in systems that look for early-life and hidden failures before dies are cut from the wafer¹⁵. Catching those failures early lowers the risk of packaging high-bandwidth memory and an expensive substrate with a processor that may later fail¹⁵. Aehr says its lead AI customer is moving all burn-in of that customer's AI accelerators from the system level, after packaging, to the wafer¹⁶. The FOX-XP systems that customer ordered from Aehr in August 2026 each burn in nine 300 mm wafers at a time¹⁵.

02

The stages of chip testing

Wafer sort and known-good die

The hard part of wafer sort is the probe card, the circuit board that holds the needles. For a large logic die every needle must sit in the same plane, survive repeated touchdowns without drifting, and do it hot. Each card is built for one chip design, so every new design needs a new card and a new qualification. FormFactor, an American probe card maker, says its cards work at high enough frequencies to compete well in testing high-bandwidth memory, a stack of eight, twelve or sixteen memory dies¹⁷.

Final test, burn-in and system-level test

The bigger the package, the more one bad die can cost. TSMC told investors in July 2026 that its CoWoS roadmap includes packages larger than 14 times the area a lithography machine can print in one shot¹⁸. A die that fails after assembly wastes the memory and substrate joined to it¹⁵.

¹⁴ Aehr Test Systems, annual report on Form 10-K for the fiscal year ended 29 May... U.S. Securities and Exchange Commission, 27 July 2026. [sec.gov](#)

¹⁵ Aehr Receives \$22 Million Follow-On Order for AI Processor Wafer-Level Burn-In... Aehr Test Systems, 12 August 2026. [aehr.com](#)

¹⁶ Aehr Test Systems Reports Fiscal 2026 Fourth Quarter and Full Year Financial... Aehr Test Systems, 14 July 2026. [aehr.com](#)

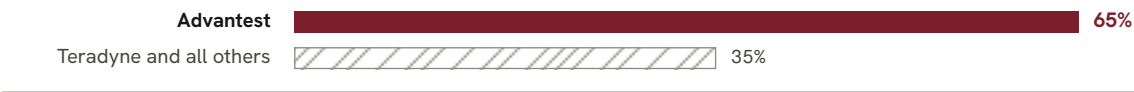
¹⁷ FormFactor, annual report on Form 10-K for the fiscal year ended 27 December... U.S. Securities and Exchange Commission, 20 February 2026. [sec.gov](#)

¹⁸ Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese... LSEG StreetEvents, 16 July 2026, p. 16. [investor.tsmc.com](#)

Figure 12.2

Advantest put its tester market share at about 65 percent in 2025

Automated test equipment: share of the ~\$9.0 billion tester market, 2025



Source: Advantest FY2025 results briefing, April 2026 [6]

03

Who makes test and assembly tools

Advantest puts its own share at about 65 percent of an estimated \$9.0 billion tester market in 2025⁶. Its share of system-on-chip (SoC) testers, the machines that test processors and other non-memory chips, rose about ten points in a year to 66 percent⁶. It held about 60 percent of memory test⁶.

Teradyne, Advantest's main rival, took \$2.52 billion of semiconductor test revenue in 2025, service included⁷. Of that, \$1.89 billion came from SoC testers and \$505 million from memory testers⁷. Teradyne's total revenue grew 13 percent to \$3.19 billion in 2025, with fourth-quarter revenue up 44 percent on AI demand¹⁹.

Georgetown University's Center for Security and Emerging Technology (CSET) makes a second estimate, from data by the research firm TechInsights⁵. It gives Advantest 62.7 percent of a \$9.1 billion market for test tools in 2025 and Teradyne 21.8 percent⁵. Japanese firms held 63.0 percent of that market and American firms 23.5 percent⁵.

Figure 12.3

SoC testers took an estimated \$6.9 billion in 2025, memory \$2.1 billion

Where the tester money went in calendar 2025



Source: Advantest FY2025 results briefing, April 2026 [6]

The rest of the test and assembly equipment market splits into niches, each with its own suppliers.

- **Probe cards.** FormFactor took \$785.0 million of revenue in fiscal 2025, most of it from probe cards¹⁷. Technoprobe's revenue grew 15.7 percent to EUR 628.4 million in 2025, about 38 percent of it from AI²⁰. It aims to double its manufacturing capacity by the end of 2027²⁰.

5 Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 20 October 2026. chipexplorer.eto.tech

6 Advantest, presentation notes for the FY2025 (year ended 31 March 2026) results... Advantest, 27 April 2026, p. 13. advantest.com

7 Teradyne, annual report on Form 10-K for the fiscal year ended 31 December 2025. U.S. Securities and Exchange Commission, 19 February 2026. sec.gov

17 FormFactor, annual report on Form 10-K for the fiscal year ended 27 December... U.S. Securities and Exchange Commission, 20 February 2026. sec.gov

19 Teradyne Reports Fourth Quarter and Full Year 2025 Results. Teradyne, 2 February 2026. investors.teradyne.com

20 Technoprobe, press release: the Board of Directors approves the draft statutory... Technoprobe, 18 March 2026, p. 1. technoprobe.com

- **Probers**, the machines that move each wafer under the probe card and keep it at a set temperature. Tokyo Seimitsu, which sells under the Accretech name, says its own research gives it the largest global share in probers²¹. Tokyo Electron makes probers too²². CSET's analysis of TechInsights data counts handlers and probers as one market, worth \$2.9 billion in 2025, and gives Tokyo Electron 19.9 percent of it and Accretech 17.1 percent²³.
- **Handlers and burn-in**, the machines that feed packaged parts into a tester and hold them at a set temperature, and the systems that run burn-in. Cohu took \$453.0 million of revenue in fiscal 2025²⁴. Aehr's revenue was \$50.0 million in fiscal 2026, but it booked a record \$60.7 million of orders in the fourth quarter alone¹⁶. It expects revenue of \$130 million to \$150 million in fiscal 2027¹⁶.
- **Dicing and grinding**. Dicing saws cut wafers into dies, and grinders thin them. CSET's analysis of TechInsights data found that in 2025 Disco held 87 percent and Accretech 8.1 percent of the \$1.9 billion market for these machines¹⁰. Panel-level packaging builds packages on large panels in place of 300 mm wafers, to make more of them at once²⁵. In December 2025 Disco announced a saw that cuts such panels, as large as 400 by 400 mm, into individual packages²⁵.
- **Bonding**. Kulicke and Soffa took \$654.1 million of revenue in fiscal 2025²⁶. Besi's second-quarter 2026 revenue rose 68.7 percent to EUR 249.9 million on hybrid bonding and data center demand²⁷.

Thermocompression bonders use heat and force to press memory dies into a stack and to attach chiplets to substrates. ASMPT says it remained the leader in that market in 2025 and aims for a 35 to 40 percent share²⁸. In its 2025 results it said it expects the market to reach \$1.6 billion by 2028²⁸. In July 2026 ASMPT announced new bulk orders for more than 50 of its chip-to-substrate bonders for AI chips, from outsourced assembly and test firms²⁹. Hanmi Semiconductor in South Korea also sells thermocompression bonders for high-bandwidth memory³⁰. See Memory and HBM.

04

Where chips are assembled and tested

Taiwanese firms lead outsourced assembly and test, the OSAT business, and Chinese firms are large challengers. Taiwan's ASE billed \$20,573.4 million in 2025¹¹. Packaging made up about 48 percent of that, testing about 11 percent and its electronics

¹⁰ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

¹¹ ASE Technology Holding, annual report on Form 20-F for the fiscal year ended 31... U.S. Securities and Exchange Commission, 1 April 2026. sec.gov

¹⁶ Aehr Test Systems Reports Fiscal 2026 Fourth Quarter and Full Year Financial... Aehr Test Systems, 14 July 2026. aehr.com

²¹ Tokyo Seimitsu Integrated Report 2025. Accretech, 3 December 2025, p. 6. accretech.com

²² Precio™ Series. Tokyo Electron, accessed 9 September 2026. tel.com

²³ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 20 October 2026. chipexplorer.eto.tech

²⁴ Cohu, annual report on Form 10-K for the fiscal year ended 27 December 2025. U.S. Securities and Exchange Commission, 17 February 2026. sec.gov

²⁵ DISCO develops the DFD6080 fully automatic dicing saw for work sizes up to 400... DISCO Corporation, 15 December 2025. disco.co.jp

²⁶ Kulicke and Soffa, results for the fourth quarter and fiscal 2025 (Form 8-K... U.S. Securities and Exchange Commission, 19 November 2025. sec.gov

²⁷ BE Semiconductor Industries N.V. Announces Q2-26 and H1-26 Results. BE Semiconductor Industries (Besi), 23 July 2026. besi.com

²⁸ ASMPT Announces 2025 Annual Results AI-Driven Structural Growth Underpins Group... ASMPT, 4 March 2026. asmpt.com

²⁹ ASMPT Secures Significant Wins for More than 50 Chip-to-Substrate... ASMPT, 29 July 2026. asmpt.com

³⁰ Hanmi Semiconductor, products page. Hanmi Semiconductor, accessed 9 September 2026. hanmisemi.com

manufacturing arm about 40 percent³¹. In a TrendForce ranking that CSET cites, four of the top ten OSATs by 2024 revenue are headquartered in China¹.

Malaysia is a large center for chip assembly and test. Its investment agency said in July 2026 that the country ships 13 percent of the world's packaged chips³². It said a consortium of five Malaysian firms aims to help the country capture 7 percent of world advanced packaging shipments by 2035³². A 2024 study by the Semiconductor Industry Association and Boston Consulting Group used a different measure, capacity³³. It gave Malaysia 7 percent of global assembly, test and packaging capacity in 2022, the largest share in Southeast Asia³³. The study measured capacity by factory floor space at contractors and chipmakers' own plants³⁴.

Taiwan's assembly and test contractors are expanding. ASE ran 6,797 testers in the second quarter of 2025 and 8,348 a year later⁸. It spent \$2.7 billion on machinery and \$1.4 billion on buildings, facilities and automation in the first half of 2026³⁵. In July 2026 it said revenue from leading-edge advanced packaging was running ahead of its \$3.5 billion forecast for 2026³⁵. Powertech, another Taiwanese assembly and test firm, aims to run the first panel-level packaging line for AI chips in 2027³⁶.

Amkor, an American assembly and test contractor, took \$6.71 billion of revenue in 2025⁹. Its revenue in the second quarter of 2026 alone was \$1.90 billion, up 26 percent year on year³⁷. By October 2025 it had raised the planned investment in its Arizona campus to \$7 billion¹².

In October 2024 TSMC and Amkor signed a memorandum of understanding for TSMC to buy packaging and test services from Amkor's planned plant in Peoria, Arizona³⁸. TSMC would use those services for its customers, especially those using its Phoenix fabs³⁸. The two announced a long-term partnership in June 2026¹³.

1 Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology, 14 July 2025. cset.georgetown.edu

8 ASE Technology Holding, report on Form 6-K dated 30 July 2026. U.S. Securities and Exchange Commission, 30 July 2026. sec.gov

9 Amkor Technology, current report on Form 8-K dated 9 February 2026. U.S. Securities and Exchange Commission, 9 February 2026. sec.gov

12 Amkor Technology Breaks Ground on New Semiconductor Advanced Packaging and Test... Amkor Technology, 6 October 2025. ir.amkor.com

13 TSMC and Amkor Technology Announce Long Term Partnership to Accelerate Advanced... Amkor Technology, 16 June 2026. ir.amkor.com

31 ASE Technology Holding, report on Form 6-K dated 5 February 2026. U.S. Securities and Exchange Commission, 5 February 2026. sec.gov

32 Advanced Packaging: How Malaysia is Packaging the Future of AI. Malaysian Investment Development Authority, 1 July 2026. mida.gov.my

33 Emerging Resilience in the Semiconductor Supply Chain. Boston Consulting Group and Semiconductor Industry..., May 2024, p. 21. semiconductors.org

34 Emerging Resilience in the Semiconductor Supply Chain. Boston Consulting Group and Semiconductor Industry..., May 2024, p. 35. semiconductors.org

35 ASE Technology Holding, report on Form 6-K dated 30 July 2026. U.S. Securities and Exchange Commission, 30 July 2026. sec.gov

36 Powertech eyes world's first panel-level packaging for AI chips in 2027. Nikkei Asia, 27 August 2026. asia.nikkei.com

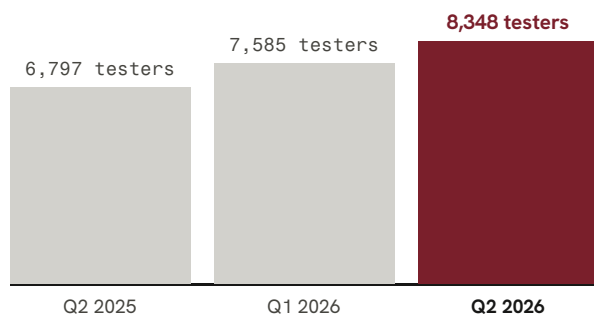
37 Amkor Technology, current report on Form 8-K dated 27 July 2026. U.S. Securities and Exchange Commission, 27 July 2026. sec.gov

38 Amkor and TSMC to Expand Partnership and Collaborate on Advanced Packaging in... TSMC, 4 October 2024. pr.tsmc.com

Figure 12.4

ASE ran 8,348 testers in mid-2026, up from 6,797 a year earlier

Testers installed at ASE, a Taiwanese assembly and test contractor



Source: ASE Technology Holding, second quarter 2026 earnings release (SEC Form 6-K) [8]

05

Tester switching costs and China's toolmakers

Customers can switch tester makers, but at a cost. Advantest says that switching to another tester maker means rebuilding the whole test setup used for development, evaluation and mass production, at significant extra cost to the customer². Still, ASE says it buys testers with similar functions from different makers, including Teradyne and Advantest¹¹.

Chinese toolmakers are gaining share in test and advanced packaging tools, but CSET finds they still lag significantly behind foreign suppliers in market share¹. Between 2019 and 2024 they gained 5 percentage points of world market share in test tools and 4 points in fabrication tools built for advanced packaging, by CSET's analysis of TechInsights data¹. But they lost share in bonding and other conventional assembly and packaging tools¹.

Assembly and test contractors such as ASE and Amkor earn a small part of what the chip industry sells. ASE's packaging business took \$9,829.2 million from outside customers in 2025, and its testing business \$2,292.0 million¹¹. Amkor's revenue was \$6.71 billion⁹. Global semiconductor sales that year were \$791.7 billion³⁹.

Four questions to answer from memory

1. What does a chip tester do? [see How it works](#)
2. Why do chipmakers test AI chips early and often? [see How it works](#)
3. Who makes most chip testers? [see Who makes it](#)

¹ Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology, 14 July 2025. cset.georgetown.edu

² Investors Guide July 29, 2026. Advantest, 30 July 2026, p. 12. advantest.com

⁸ ASE Technology Holding, report on Form 6-K dated 30 July 2026. U.S. Securities and Exchange Commission, 30 July 2026. sec.gov

⁹ Amkor Technology, current report on Form 8-K dated 9 February 2026. U.S. Securities and Exchange Commission, 9 February 2026. sec.gov

¹¹ ASE Technology Holding, annual report on Form 20-F for the fiscal year ended 31... U.S. Securities and Exchange Commission, 1 April 2026. sec.gov

³⁹ Global Annual Semiconductor Sales Increase 25.6% to \$791.7 Billion in 2025. Semiconductor Industry Association, 6 February 2026. semiconductors.org

4. Why is it costly to switch tester makers? see The chokepoint

Three things to remember

- Chips are tested early and often because one bad chip can ruin a package of expensive ones.
 - Advantest and Teradyne account for most spending on chip testers.
 - In a TrendForce ranking cited by CSET, four of the top ten outsourced assembly and test firms by 2024 revenue are based in China.
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Sources (39)

1. A Inside Beijing's Chipmaking Offensive. Center for Security and Emerging Technology (CSET) · 14 July 2025
cset.georgetown.edu/article/inside-beijings-chipmaking-offensive/
2. A Investors Guide July 29, 2026. Advantest · 30 July 2026 · p. 12
www.advantest.com/document/en/investors/ir-library/investors-guide/Investors_Guide_2607E.pdf#page=12
3. A Testimony of David Isaacs, Semiconductor Industry Association, hearing on "Trade in Critical Supply Chains". U.S. Senate Committee on Finance · 14 May 2025 · p. 2
www.finance.senate.gov/download/051425-isaacs-testimony&download=1#page=2
4. A Investors Guide July 29, 2026. Advantest · 30 July 2026 · p. 10
www.advantest.com/document/en/investors/ir-library/investors-guide/Investors_Guide_2607E.pdf#page=10
5. A Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 20 October 2026
chipexplorer.eto.tech/?parentNode=N78&selectedNode=N120
6. A Advantest, presentation notes for the FY2025 (year ended 31 March 2026) results briefing, 27 April 2026. Advantest · 27 April 2026 · p. 13
www.advantest.com/document/en/investors/ir-library/result/JE_BIZ_260427_note.pdf#page=13
7. A Teradyne, annual report on Form 10-K for the fiscal year ended 31 December 2025. U.S. Securities and Exchange Commission (filing by Teradyne) · 19 February 2026
www.sec.gov/Archives/edgar/data/97210/000119312526059002/ter-20251231.htm
8. A ASE Technology Holding, report on Form 6-K dated 30 July 2026. U.S. Securities and Exchange Commission (filing by ASE Technology Holding) · 30 July 2026
www.sec.gov/Archives/edgar/data/1122411/000095010326011351/dp250868_6k.htm
9. A Amkor Technology, current report on Form 8-K dated 9 February 2026. U.S. Securities and Exchange Commission (filing by Amkor Technology) · 9 February 2026
www.sec.gov/Archives/edgar/data/1047127/000104712726000007/amkr123125erex-991.htm
10. A Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N69&selectedNode=N71
11. A ASE Technology Holding, annual report on Form 20-F for the fiscal year ended 31 December 2025. U.S. Securities and Exchange Commission (filing by ASE Technology Holding) · 1 April 2026
www.sec.gov/Archives/edgar/data/1122411/000119312526135585/d50802d20f.htm
12. A Amkor Technology Breaks Ground on New Semiconductor Advanced Packaging and Test Campus in Arizona; Expands Investment to \$7 Billion. Amkor Technology · 6 October 2025
ir.amkor.com/news-releases/news-release-details/amkor-technology-breaks-ground-new-semiconductor-advanced
13. A TSMC and Amkor Technology Announce Long Term Partnership to Accelerate Advanced Packaging in the United States. Amkor Technology · 16 June 2026
ir.amkor.com/news-releases/news-release-details/tsmc-and-amkor-technology-announce-long-term-partnership
14. A Aehr Test Systems, annual report on Form 10-K for the fiscal year ended 29 May 2026. U.S. Securities and Exchange Commission (filing by Aehr Test Systems) · 27 July 2026
www.sec.gov/Archives/edgar/data/1040470/000165495426006919/aehr_10k.htm
15. A Aehr Receives \$22 Million Follow-On Order for AI Processor Wafer-Level Burn-In Systems. Aehr Test Systems · 12 August 2026
www.aehr.com/2026/08/aehr-receives-22-million-follow-on-order-for-ai-processor-wafer-level-burn-in-systems/
16. A Aehr Test Systems Reports Fiscal 2026 Fourth Quarter and Full Year Financial Results with Record Quarterly Bookings and \$100 Million Effective Backlog. Aehr Test Systems · 14 July 2026
www.aehr.com/2026/07/aehr-test-systems-reports-fiscal-2026-fourth-quarter-and-full-year-financial-results-with-record-quarterly-bookings-and-100-million-effective-backlog/
17. A FormFactor, annual report on Form 10-K for the fiscal year ended 27 December 2025. U.S. Securities and Exchange Commission (filing by FormFactor) · 20 February 2026
www.sec.gov/Archives/edgar/data/1039399/000103939926000009/form-20251227.htm

18. A **Q2 2026 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript.** LSEG StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 July 2026 · p. 16
investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2026-08/3e494f0c14dd0890f897aa044415e21d93486cc4/TSMC%202Q26%20Transcript.pdf#page=16
19. A **Teradyne Reports Fourth Quarter and Full Year 2025 Results.** Teradyne · 2 February 2026
investors.teradyne.com/news-events/press-releases/detail/433/teradyne-reports-fourth-quarter-and-full-year-2025-results
20. A **Technoprobe, press release: the Board of Directors approves the draft statutory and consolidated annual report as at 31 December 2025.** Technoprobe · 18 March 2026 · p. 1
technoprobe.com/wp-content/uploads/2026/03/PR-FY-2025_.pdf#page=1
21. A **Tokyo Seimitsu Integrated Report 2025.** Accretech · 3 December 2025 · p. 6
www.accrettech.com/en/ir/index/main/00/teaserItems1/00/linkList/02/link/IntegratedReport2025_E.pdf#page=6
22. A **Precio™ Series.** Tokyo Electron · Accessed 9 September 2026
www.tel.com/product/precio.html
23. A **Supply Chain Explorer: Advanced Chips.** Emerging Technology Observatory (ETO) · Accessed 20 October 2026
chipexplorer.eto.tech/?parentNode=N78&selectedNode=N83
24. A **Cohu, annual report on Form 10-K for the fiscal year ended 27 December 2025.** U.S. Securities and Exchange Commission (filing by Cohu) · 17 February 2026
www.sec.gov/Archives/edgar/data/21535/000143774926004339/cohu20251227_10k.htm
25. A **DISCO develops the DFD6080 fully automatic dicing saw for work sizes up to 400 mm square (最大400mm角のパッケージ切断に対応したダイシングソー「DFD6080」を開発).** DISCO Corporation · 15 December 2025
www.disco.co.jp/eg/news/corp/20251215_1.html
26. A **Kulicke and Soffa, results for the fourth quarter and fiscal 2025 (Form 8-K, exhibit 99.1).** U.S. Securities and Exchange Commission (filing by Kulicke and Soffa) · 19 November 2025
www.sec.gov/Archives/edgar/data/56978/000005697825000078/ex991liveq42025.htm
27. A **BE Semiconductor Industries N.V. Announces Q2-26 and H1-26 Results.** BE Semiconductor Industries (Besi) · 23 July 2026
www.besi.com/investor-relations/press-releases/2025/details-1/be-semiconductor-industries-nv-announces-q2-26-and-h1-26-results/
28. A **ASMPT Announces 2025 Annual Results AI-Driven Structural Growth Underpins Group Performance.** ASMPT · 4 March 2026
www.asmpt.com/en/investor-relations/news-events/asmpt-announces-2025-annual-results/
29. A **ASMPT Secures Significant Wins for More than 50 Chip-to-Substrate Thermo-Compression Bonding Tools.** ASMPT · 29 July 2026
www.asmpt.com/en/investor-relations/news-events/asmpt-secures-significant-wins/
30. A **Hanmi Semiconductor, products page.** Hanmi Semiconductor · Accessed 9 September 2026
www.hanmisemi.com/en/product/index.html
31. A **ASE Technology Holding, report on Form 6-K dated 5 February 2026.** U.S. Securities and Exchange Commission (filing by ASE Technology Holding) · 5 February 2026
www.sec.gov/Archives/edgar/data/1122411/000095010326001661/dp241159_6k.htm
32. A **Advanced Packaging: How Malaysia is Packaging the Future of AI.** Malaysian Investment Development Authority · 1 July 2026
www.mida.gov.my/advanced-packaging-how-malaysia-is-packaging-the-future-of-ai/
33. A **Emerging Resilience in the Semiconductor Supply Chain.** Boston Consulting Group and Semiconductor Industry Association · May 2024 · p. 21
www.semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconductor-Supply-Chain.pdf#page=21
34. A **Emerging Resilience in the Semiconductor Supply Chain.** Boston Consulting Group and Semiconductor Industry Association · May 2024 · p. 35
www.semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconductor-Supply-Chain.pdf#page=35
35. A **ASE Technology Holding, report on Form 6-K dated 30 July 2026.** U.S. Securities and Exchange Commission (filing by ASE Technology Holding) · 30 July 2026
www.sec.gov/Archives/edgar/data/1122411/000095010326011353/dp250875_6k.htm
36. B **Powertech eyes world's first panel-level packaging for AI chips in 2027.** Nikkei Asia · 27 August 2026
asia.nikkei.com/business/tech/semiconductors/powertech-eyes-world-s-first-panel-level-packaging-for-ai-chips-in-2027
37. A **Amkor Technology, current report on Form 8-K dated 27 July 2026.** U.S. Securities and Exchange Commission (filing by Amkor Technology) · 27 July 2026
www.sec.gov/Archives/edgar/data/1047127/000104712726000043/amkr6302026erex-991.htm
38. A **Amkor and TSMC to Expand Partnership and Collaborate on Advanced Packaging in Arizona.** TSMC · 4 October 2024
pr.tsmc.com/english/news/3174
39. A **Global Annual Semiconductor Sales Increase 25.6% to \$791.7 Billion in 2025.** Semiconductor Industry Association · 6 February 2026
www.semiconductors.org/global-annual-semiconductor-sales-increase-25-6-to-791-7-billion-in-2025/



01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Systems and Networking

Nvidia's and AMD's racks wire 72 AI chips together to run as one computer. Many firms can assemble the racks, but lasers for the optical links were scarce in 2026.

Specimen 13 · Systems and Networking

An eight-GPU baseboard, the board that carries eight accelerator modules and the switch chips joining them. It is about 510 by 400 mm and drawn to scale, with the module frames standing about 30 mm above the board. The two nickel-gray squares in the middle are the NVLink switch chips.

In plain terms

One AI chip is not enough to train a model. So seventy-two of them are wired together in a rack, a cabinet the size of a wardrobe, and run as one computer. Many such racks are then linked to train a large model. Each chip sits on its own board and draws more than a thousand amps, several times the current a whole house is wired to carry. The chips have to swap results with each other all the time. A copper wire can carry those signals only a few meters before they fade, so the longer links send them as light down glass fiber. Many companies can build the rack, but in 2026 the lasers that send the light were scarce.

In short

In March 2026 Nvidia agreed to invest \$2 billion in the laser maker Lumentum, alongside a multibillion-dollar purchase commitment and rights to future capacity for advanced laser components¹. Indium phosphide is used in high-speed lasers for optical communications, and China produced 70 percent of the world's indium in 2025².

On 4 February 2025 China added indium phosphide substrates, the wafers the lasers are grown on, to its export control list³. AXT, a US-listed maker of those wafers, does all its manufacturing in China³. In its filing for the quarter to June 2026, AXT said it could not estimate when it would resume shipping the wafers to the United States³.

Before a chip package can compute, it has to be built into a machine. Building that machine is a separate industry from making the package.

¹ NVIDIA Announces Strategic Partnership With Lumentum to Develop... Nvidia, 2 March 2026. nvidianews.nvidia.com

² Mineral Commodity Summaries 2026: Indium. U.S. Geological Survey, 5 February 2026. pubs.usgs.gov

³ AXT, quarterly report on Form 10-Q for the quarter ended 30 June 2026. U.S. Securities and Exchange Commission, 13 August 2026. sec.gov

Chokepoint card

Systems and Networking

Concentration



High

Four to six firms could supply this stage today, and the top two take most of the revenue.

Substitutability

Moderate

Rated on NVLink and its NVSwitch chips, which Nvidia controls and which join the accelerators in a rack⁴. Separately, lasers for the optical links were scarce in 2026⁵. Nvidia secured future capacity rights for them from Lumentum in March 2026¹.

Price or market size

\$3.1 million

for one GB200 NVL72 rack bought by a typical hyperscaler, or about \$3.9 million with networking, storage and other items, by SemiAnalysis's August 2025 estimate⁶

Who leads	US	Nvidia	NVLink, InfiniBand and Spectrum-X Ethernet, which it credited for data center growth in the quarter to April 2026 ⁷
	US	Broadcom	\$16.7 billion of AI semiconductor revenue in the quarter to August 2026, up 221 percent ⁸
	TW	Foxconn	World's largest AI server provider, its chairman said in March 2026 ⁹
	CN	InnoLight	High-speed optical modules made in Suzhou and, since 2019, Thailand ¹⁰
	US	Coherent	Lasers and optical networking products, with a \$2 billion Nvidia investment agreed in March 2026 ¹¹
Where it is made	US	United States	Switch and accelerator silicon, system design, indium phosphide lasers
	TW	Taiwan	Contract design, rack assembly and high-layer-count circuit boards
	JP	Japan	Low-loss board laminate
	CN	China	Optical module assembly and test, and most of the world's indium
	TH	Thailand	Chinese module makers' offshore transceiver plants
Why substitution is possible	UALink is an open specification for the same job as NVLink ¹² . AMD's Helios rack, launched in July 2026, runs it over Ethernet ¹³ . Since May 2025 Nvidia's NVLink Fusion program has let other firms' custom chips use NVLink, which keeps those firms tied to Nvidia's interconnect ¹⁴ .		

1 NVIDIA Announces Strategic Partnership With Lumentum to Develop... Nvidia, 2 March 2026. [nvidianews.nvidia.com](#)

4 Nvidia, annual report on Form 10-K for the fiscal year ended 25 January 2026. U.S. Securities and Exchange Commission, 25 February 2026. [sec.gov](#)

5 AI demand strains supplies of lasers, fiber and other optical tech. Nikkei Asia, 27 May 2026. [asia.nikkei.com](#)

6 H100 vs GB200 NVL72 Training Benchmarks - Power, TCO, and Reliability Analysis... SemiAnalysis, 20 August 2025. [newsletter.semianalysis.com](#)

7 Nvidia, quarterly report on Form 10-Q for the quarter ended 26 April 2026. U.S. Securities and Exchange Commission, 20 May 2026. [sec.gov](#)

8 Broadcom, current report on Form 8-K dated 2 September 2026. U.S. Securities and Exchange Commission, 2 September 2026. [sec.gov](#)

9 Hon Hai Technology Group (Foxconn) Announces FY2025 & 4Q25 Financial Results. Hon Hai Precision Industry (Foxconn), 16 March 2026. [honhai.com](#)

10 InnoLight Technology, company overview page. InnoLight Technology, accessed 9 September 2026. [innolight.com](#)

11 NVIDIA and Coherent Announce Strategic Partnership to Develop Optics Technology... Nvidia, 2 March 2026. [nvidianews.nvidia.com](#)

12 UALink™ 200G 1.0 Specification Overview. UALink Consortium, 15 May 2025. [ualinkconsortium.org](#)

13 AAI 2026: AMD Launches AMD Helios Rackscale Solution for Frontier AI. AMD Newsroom, 23 July 2026. [newsroom.amd.com](#)

14 NVIDIA Unveils NVLink Fusion for Industry to Build Semi-Custom AI... Nvidia, 18 May 2025. [nvidianews.nvidia.com](#)

Where China stands

Chinese firms such as InnoLight assemble high-speed optical modules in volume, at sites including Suzhou and, since 2019, Thailand¹⁰. In February 2025 China put indium under new export restrictions². The same month it began requiring export permits for indium phosphide substrates, the wafers that lasers for optical links are grown on³.

Where the US stands

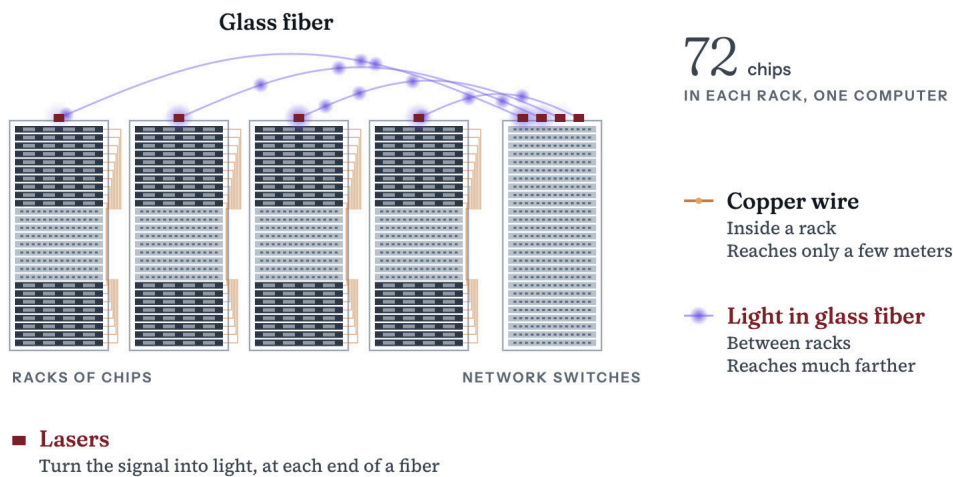
Coherent broke ground in Sherman, Texas, in June 2026 on an expansion of its factory there, which makes optical devices from indium phosphide¹⁵. In August 2026 Nvidia said that Wistron's new plant in Fort Worth, Texas, was producing its GB300 superchips and that Foxconn was building a factory in Houston¹⁶.

01

How AI racks and clusters are wired

Figure 13.1 · Explainer, 20 seconds

How AI chips are wired together



1. **One rack.** One AI chip is not enough to train a model. So 72 of them are wired together in one rack, a cabinet the size of a wardrobe, and run as one computer.
2. **Copper inside.** Inside the rack, copper wires link each tray of chips to the switch trays, which pass data between any two chips. Copper carries a signal only a few meters.
3. **Light between.** Training a large model takes many racks, most of them too far apart for copper. The links between them carry the signal as flashes of light in glass fiber.
4. **Lasers.** At each end of a fiber, a laser turns the electrical signal into flashes of light, and a detector turns them back. That lets thousands of chips in many racks work on one model.

Note: Simplified. The trays follow the layout of an Nvidia NVL72 rack. Racks and fibers are not drawn to scale.

An accelerator (the AI chip) ships as a module, the chip package on a small board with the circuits that feed it power. Nvidia calls its version SXM, and the open-standards equivalent is the Open Compute Project's accelerator module. Eight modules bolt onto a baseboard that carries their power and the links between them. On Nvidia's baseboard, switch chips pass data between any two modules at full speed.

² Mineral Commodity Summaries 2026: Indium. U.S. Geological Survey, 5 February 2026. pubs.usgs.gov

³ AXT, quarterly report on Form 10-Q for the quarter ended 30 June 2026. U.S. Securities and Exchange Commission, 13 August 2026. sec.gov

¹⁰ InnoLight Technology, company overview page. InnoLight Technology, accessed 9 September 2026. innolight.com

¹⁵ Coherent Announces a CHIPS Letter of Intent for \$50 Million to Expand... Coherent, 16 June 2026. coherent.com

¹⁶ NVIDIA and Partners Build in America, for America. Nvidia, 5 August 2026. blogs.nvidia.com

Rack-scale systems drop the baseboard and put the chips on trays stacked in the rack. An Nvidia GB300 NVL72 holds 18 compute trays plus nine switch trays, 72 GPUs in all, and draws up to 142 kW¹⁷. The newer Vera Rubin NVL72 uses the same rack footprint¹⁸. The research firm SemiAnalysis estimated in August 2025 that a rack of the earlier GB200 NVL72 model cost a typical hyperscaler \$3.1 million, or about \$3.9 million with networking, storage and other items⁶.

Inside the rack the trays reach each other over copper¹⁷. Between neighboring racks, the signal can travel up to 7 meters over active electrical cables, a type of copper cable sold by firms such as Credo¹⁹. Longer links run on glass fiber, with an optical transceiver at each end. A laser in the sending transceiver turns the electrical signal into pulses of light, and a detector in the receiving one turns the pulses back into current.

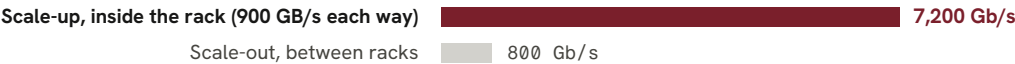
The accelerators in an AI cluster exchange data over two networks that are not interchangeable. Scale-up connects anywhere from a few dozen accelerators to thousands closely enough that they can read each other's memory. It runs at terabytes per second. Scale-out joins those groups to one another at hundreds of gigabits per second. Scale-up speeds are quoted in bytes and scale-out speeds in bits, and a byte is eight bits. Each GPU in a GB300 NVL72 can send 900 gigabytes per second each way over the scale-up network, or 7,200 gigabits per second²⁰. Over the scale-out network it can send 800 gigabits per second²⁰. So each GPU has nine times as much bandwidth for scale-up as for scale-out, SemiAnalysis calculated in January 2026²⁰.

Scale-up bandwidth limits how efficiently a large model trains. A model too big for one accelerator is split across many. The parts that exchange data constantly stay inside the scale-up group, because they need its high bandwidth²¹. Whole blocks of layers, the stages a model's calculation passes through in turn, can sit on different groups across the slower scale-out network²¹.

Figure 13.2

Each GPU has nine times as much bandwidth inside its rack as between racks

One GPU's links in an Nvidia GB300 NVL72 rack, scale-up inside the rack against scale-out between racks, drawn to scale



A model too big for one accelerator is split across many. The parts that exchange data constantly stay inside the scale-up group, and whole blocks of layers can sit on different groups across the slower scale-out network.

Source: Co-Packaged Optics (CPO) Book – Scaling with Light for the Next Wave of Interconnect [20], Nvidia NVL72 system hardware and components [17] and Nvidia NeMo parallelisms guide [21]

Note: Simplified. One GPU's two links are drawn to scale, and the racks are not.

6 H100 vs GB200 NVL72 Training Benchmarks - Power, TCO, and Reliability Analysis... SemiAnalysis, 20 August 2025. newsletter.semanalysis.com

17 System Hardware & Components. Nvidia, accessed 9 September 2026. docs.nvidia.com

18 NVIDIA, Partners Drive Next-Gen Efficient Gigawatt AI Factories in Buildup for... Nvidia, 13 October 2025. blogs.nvidia.com

19 Credo Technology Group, annual report on Form 10-K for the fiscal year ended 2... U.S. Securities and Exchange Commission, 15 June 2026. sec.gov

20 Co-Packaged Optics (CPO) Book – Scaling with Light for the Next Wave of... SemiAnalysis, 1 January 2026. newsletter.semanalysis.com

21 Parallelisms Guide — Megatron Bridge. Nvidia, accessed 9 September 2026. docs.nvidia.com

02

Types of links between AI chips

Scale-up: NVLink, UALink and Google's torus

The designs differ in how many accelerators can share one pool of memory.

- **NVLink and NVSwitch.** Nvidia's NVLink bandwidth per GPU, counting both directions, went from 900 GB/s in NVLink 4 to 1,800 GB/s in NVLink 5²². Across a whole Blackwell NVL72 rack, NVLink moves 130 TB/s²². Nvidia's Rubin launch release of January 2026 gives NVLink 6 as 3,600 GB/s per GPU and 260 TB/s for a Vera Rubin NVL72 rack²³. As of October 2026, Nvidia's NVLink product page still lists preliminary figures of 3,000 GB/s and 216 TB/s²².
- **UALink.** The open specification, from the UALink Consortium, runs 200 Gb/s per lane, and four lanes, which it calls a station, carry 800 Gb/s¹². It can address up to 1,024 endpoints, such as accelerators, in one group¹². AMD's Helios rack, launched in July 2026, joins 72 GPUs and runs UALink over Ethernet for its scale-up network¹³.
- **Google's 3D torus.** Google wires 64 of its Ironwood TPU accelerators into each rack, called a cube²⁴. Inside the cube each chip links directly to six others, in a three-dimensional grid that Google calls a 3D torus²⁴. Optical circuit switches, which steer light from one fiber to another, join cubes into superpods of 9,216 chips and can route around a failed cube or link²⁴.

Scale-out: InfiniBand versus Ethernet

Scale-out networks typically use InfiniBand or Ethernet, SemiAnalysis wrote in January 2026²⁰. InfiniBand is a specialized network long used in supercomputers. But Ethernet switch capacity has grown quickly. Broadcom's Tomahawk 4 switched 25.6 Tbps on one chip in December 2019²⁵. Tomahawk 5 reached 51.2 Tbps in August 2022, and Broadcom said it had doubled the bandwidth about every two years since 2014²⁶. Tomahawk 6 doubled it again to 102.4 Tbps in June 2025²⁷. In June 2025 the Ultra Ethernet Consortium published its 1.0 specification, a set of Ethernet-based rules for communication in AI and supercomputing²⁸. It covers how data is carried, how traffic jams are avoided and how one machine reads or writes another's memory directly²⁸.

Nvidia sells switches and network cards for both InfiniBand and Ethernet. Its data center revenue, which counts its GPUs as well as its networking gear, reached \$89.0

¹² UALink™ 200G 1.0 Specification Overview. UALink Consortium, 15 May 2025. ualinkconsortium.org

¹³ AAI 2026: AMD Launches AMD Helios Rackscale Solution for Frontier AI. AMD Newsroom, 23 July 2026. newsroom.amd.com

²⁰ Co-Packaged Optics (CPO) Book – Scaling with Light for the Next Wave of... SemiAnalysis, 1 January 2026. newsletter.semianalysis.com

²² NVLink & NVLink Switch for Advanced Multi-GPU Communication. Nvidia, 20 April 2026. nvidia.com

²³ NVIDIA Kicks Off the Next Generation of AI With Rubin. Nvidia, 5 January 2026. nvidianews.nvidia.com

²⁴ Inside the Ironwood TPU codigned AI stack. Google Cloud, 6 November 2025. cloud.google.com

²⁵ Broadcom Ships Tomahawk 4, Industry's Highest Bandwidth Ethernet Switch Chip at... Broadcom, 9 December 2019. investors.broadcom.com

²⁶ Broadcom Ships Tomahawk 5, Industry's Highest Bandwidth Switch Chip to... Broadcom, 16 August 2022. investors.broadcom.com

²⁷ Broadcom Ships Tomahawk 6: World's First 102.4 Tbps Switch. Broadcom, 3 June 2025. investors.broadcom.com

²⁸ Ultra Ethernet Consortium (UEC) Launches Specification 1.0 Transforming... Ultra Ethernet Consortium, 11 June 2025. ultraethernet.org

billion in the quarter to July 2026, up 117 percent from a year earlier²⁹. In the quarter before, it credited its data center growth to Blackwell 300 products and to demand for its "InfiniBand, Spectrum-X Ethernet, and NVLink" solutions⁷.

Optics: pluggable, then co-packaged

Broadcom and Nvidia are moving the optics out of pluggable transceivers and into the switch chip's own package, a design called co-packaged optics. A cluster needs several transceivers, the modules that turn electricity into light and back, for each accelerator. Their power cost is one reason for the change. Broadcom says its Tomahawk 6 Davison cuts the power used by optical links by 70 percent compared with traditional pluggable modules³⁰. It keeps its lasers in field-replaceable modules³⁰. Nvidia's Spectrum-X Photonics switches, announced in March 2025, have up to 512 ports of 800 gigabits per second each, and Nvidia says they use four times fewer lasers than traditional designs³¹. Nvidia builds them on its Spectrum-6 switch design²³. In August 2026 Nvidia said its Spectrum-6 switch systems, with pluggable or co-packaged optics, were arriving at AI data centers around the world³².

03

Who makes optics, switch chips and AI servers

Chinese makers of optical modules have built plants outside China. InnoLight has run a plant in Thailand since 2019, alongside its sites in Suzhou and Taiwan¹⁰. The Thai subsidiary of Eoptolink, another Chinese module maker, lists sites in Chonburi and Rayong³³.

A US rule from July 2026 may reach optical transceivers made by firms on a US security list. The list is the Federal Communications Commission's Covered List of equipment and services judged to pose an unacceptable risk to US national security or to the security and safety of US persons³⁴. Under its July 2026 order, the FCC no longer approves new devices for the US market if they contain logic-bearing hardware components made by firms on the list³⁵. The order counts as logic-bearing any part that uses digital logic, from a single chip to a whole module, and leaves out parts with no digital function, such as wiring and housings³⁶. Commenters in the record named

⁷ Nvidia, quarterly report on Form 10-Q for the quarter ended 26 April 2026. U.S. Securities and Exchange Commission, 20 May 2026. sec.gov

¹⁰ InnoLight Technology, company overview page. InnoLight Technology, accessed 9 September 2026. innolight.com

²³ NVIDIA Kicks Off the Next Generation of AI With Rubin. Nvidia, 5 January 2026. nvidianews.nvidia.com

²⁹ Nvidia, quarterly report on Form 10-Q for the quarter ended 26 July 2026. U.S. Securities and Exchange Commission, 26 August 2026. sec.gov

³⁰ Broadcom Announces Tomahawk 6 – Davison, the Industry's First 102.4-Tbps... Broadcom, 8 October 2025. investors.broadcom.com

³¹ NVIDIA Announces Spectrum-X Photonics, Co-Packaged Optics Networking Switches... Nvidia, 18 March 2025. nvidianews.nvidia.com

³² NVIDIA Announces Financial Results for Second Quarter Fiscal 2027. Nvidia, 26 August 2026. nvidianews.nvidia.com

³³ Eoptolink Technology, contacts page. Eoptolink Technology, accessed 9 September 2026. eoptolink.com

³⁴ Protecting Against National Security Threats to the Communications Supply Chain... U.S. Federal Communications Commission, 23 July 2026, p. 3. docs.fcc.gov

³⁵ Protecting Against National Security Threats to the Communications Supply Chain... U.S. Federal Communications Commission, 23 July 2026, p. 6. docs.fcc.gov

³⁶ Protecting Against National Security Threats to the Communications Supply Chain... U.S. Federal Communications Commission, 23 July 2026, p. 13. docs.fcc.gov

optical transceivers as one such component³⁷. As of 16 October 2026, the Covered List did not include InnoLight³⁸.

China produces most of the world's indium, the raw material for indium phosphide lasers, and restricts its export. Indium phosphide is used in the high-speed laser diodes and photodetectors for optical communications². China accounted for 70 percent of world indium production in 2025². In February 2025 China's Ministry of Commerce placed indium under new export restrictions².

AI data centers were straining supplies of the lasers inside optical modules and pushing up their prices, Nikkei Asia reported in May 2026⁵. Nvidia had agreed in March 2026 to invest \$2 billion in one laser maker, Lumentum, alongside a multibillion-dollar purchase commitment and rights to future capacity for advanced laser components¹. Coherent, another laser maker, broke ground in Sherman, Texas, in June 2026 on an expansion of its factory there, which makes optical devices from indium phosphide¹⁵.

Two American firms, Broadcom and Marvell, sell both custom AI chips and Ethernet switch chips. In its annual report for fiscal 2025, Broadcom said its AI chips include Ethernet switch chips as well as custom accelerators, which it builds to each customer's specifications³⁹. Its AI semiconductor revenue reached \$16.7 billion in the third quarter of fiscal 2026, up 221 percent from a year earlier⁸. Marvell also builds custom AI chips to each customer's specifications and sells Ethernet switch chips, its annual report for fiscal 2026 says⁴⁰. Marvell's five-year agreement with Amazon Web Services, announced in December 2024, covers custom AI chips alongside the optical and networking parts that go with them⁴¹.

Taiwanese firms do much of the physical assembly. Foxconn booked NT\$8.1 trillion of revenue in 2025, up 18 percent, and cloud and networking was its largest product category in the fourth quarter⁹. In the same results release, its chairman called Foxconn the world's largest AI server provider⁹.

Some assembly is moving to the United States. In April 2025 Nvidia said it was building supercomputer manufacturing plants in Texas, with Foxconn in Houston and Wistron in Dallas⁴². It expected mass production to ramp up in the following 12 to 15 months⁴². In August 2026 Nvidia said Wistron's new plant in Fort Worth, Texas, near Dallas, was producing its GB300 superchips, which pair Nvidia's Grace processor with its Blackwell

1 NVIDIA Announces Strategic Partnership With Lumentum to Develop... Nvidia, 2 March 2026. nvidianews.nvidia.com

2 Mineral Commodity Summaries 2026: Indium. U.S. Geological Survey, 5 February 2026. pubs.usgs.gov

5 AI demand strains supplies of lasers, fiber and other optical tech. Nikkei Asia, 27 May 2026. asia.nikkei.com

8 Broadcom, current report on Form 8-K dated 2 September 2026. U.S. Securities and Exchange Commission, 2 September 2026. sec.gov

9 Hon Hai Technology Group (Foxconn) Announces FY2025 & 4Q25 Financial Results. Hon Hai Precision Industry (Foxconn), 16 March 2026. honhai.com

15 Coherent Announces a CHIPS Letter of Intent for \$50 Million to Expand... Coherent, 16 June 2026. coherent.com

37 Protecting Against National Security Threats to the Communications Supply Chain... U.S. Federal Communications Commission, 23 July 2026, p. 10. docs.fcc.gov

38 List of Equipment and Services Covered By Section 2 of The Secure Networks Act. U.S. Federal Communications Commission, 16 October 2026. fcc.gov

39 Broadcom, annual report on Form 10-K for the fiscal year ended 2 November 2025. U.S. Securities and Exchange Commission, 18 December 2025. sec.gov

40 Marvell Technology, annual report on Form 10-K for the fiscal year ended 31... U.S. Securities and Exchange Commission, 11 March 2026. sec.gov

41 Marvell Technology, current report on Form 8-K dated 2 December 2024. U.S. Securities and Exchange Commission, 2 December 2024. sec.gov

42 NVIDIA to Manufacture American-Made AI Supercomputers in US for First Time. Nvidia, 14 April 2025. blogs.nvidia.com

Ultra GPUs¹⁶. It said Foxconn was building a factory in Houston to make Nvidia's AI systems¹⁶.

04

Lasers and other hard-to-source parts

Many firms can build the racks. In October 2025 Nvidia said more than 50 makers of systems and components were gearing up for the Vera Rubin NVL72, which follows MGX, Nvidia's standard design for trays and racks¹⁸. But in its filing for the quarter to July 2026, Nvidia said the complexity of producing its data center systems had caused production delays²⁹.

Four inputs to the rack are harder to source elsewhere.

- **Indium phosphide laser capacity.** Nvidia has secured rights to future capacity from laser makers. Alongside its Lumentum deal, in March 2026 Nvidia agreed to invest \$2 billion in Coherent¹¹. The deal also includes a multibillion-dollar purchase commitment and rights to future access and capacity for Coherent's advanced laser and optical networking products¹¹.
- **Indium phosphide substrates.** China added indium phosphide substrates, the wafers the lasers are grown on, to its export control list on 4 February 2025³. AXT, a US-listed maker of these wafers, does all its manufacturing in China³. In its filing for the quarter to June 2026, AXT called the need for Chinese export permits the most significant challenge it faces³. It said it could not estimate when it would resume shipping the wafers to the United States³. The same filing names Sumitomo and JX, both Japanese firms, as AXT's competitors in indium phosphide³.
- **NVSwitch.** Nvidia's annual report for fiscal 2026 lists NVLink interconnects and switches among its own networking products⁴. UALink is an open standard designed for accelerator communications within one scale-up group¹². Since May 2025 Nvidia's NVLink Fusion program has let other firms' custom chips use NVLink, including CPUs that Fujitsu and Qualcomm plan to connect to Nvidia GPUs¹⁴.
- **High-layer-count circuit boards.** TTM Technologies, an American circuit board maker, says its circuit board competitors are mostly based in China and Taiwan⁴³. Nitto Boseki, a Japanese glass fiber maker, makes NE-glass, a glass cloth that absorbs less signal, for the boards in data center switches and routers⁴⁴. See Substrates and PCBs.

³ AXT, quarterly report on Form 10-Q for the quarter ended 30 June 2026. U.S. Securities and Exchange Commission, 13 August 2026. sec.gov

⁴ Nvidia, annual report on Form 10-K for the fiscal year ended 25 January 2026. U.S. Securities and Exchange Commission, 25 February 2026. sec.gov

¹¹ NVIDIA and Coherent Announce Strategic Partnership to Develop Optics Technology... Nvidia, 2 March 2026. nvidianews.nvidia.com

¹² UALink™ 200G 1.0 Specification Overview. UALink Consortium, 15 May 2025. ualinkconsortium.org

¹⁴ NVIDIA Unveils NVLink Fusion for Industry to Build Semi-Custom AI... Nvidia, 18 May 2025. nvidianews.nvidia.com

¹⁶ NVIDIA and Partners Build in America, for America. Nvidia, 5 August 2026. blogs.nvidia.com

¹⁸ NVIDIA, Partners Drive Next-Gen Efficient Gigawatt AI Factories in Buildup for... Nvidia, 13 October 2025. blogs.nvidia.com

²⁹ Nvidia, quarterly report on Form 10-Q for the quarter ended 26 July 2026. U.S. Securities and Exchange Commission, 26 August 2026. sec.gov

⁴³ TTM Technologies, annual report on Form 10-K for the fiscal year ended 29... U.S. Securities and Exchange Commission, 17 February 2026. sec.gov

⁴⁴ Nittobo Group Integrated Report 2025. Nitto Boseki (Nittobo), 16 September 2025, p. 7. nittobo.co.jp

Optical module assembly can move, as InnoLight's high-volume plant in Thailand, opened in 2019, shows¹⁰.

Four questions to answer from memory

1. **What is an AI rack?** see How it works
 2. **Why do the longer links between AI chips carry signals as light?** see How it works
 3. **What joins the chips inside an Nvidia rack?**
see Scale-up: NVLink, UALink and Google's torus
 4. **Which part of an AI rack was scarce in 2026?** see Who makes it
-

Four things to remember

- An AI rack wires 72 chips together to run as one computer.
 - Almost every link longer than 7 meters carries its signal as light, because copper fades over longer runs.
 - Nvidia's NVLink switch chips and the lasers are the hardest parts to replace. In October 2025 more than 50 makers of systems and components were gearing up to build Nvidia's next rack.
 - China produced about 70 percent of the world's indium in 2025 and has required export permits for indium phosphide substrates since February 2025.
-

Sources (44)

1. A **NVIDIA Announces Strategic Partnership With Lumentum to Develop State-of-the-Art Optics Technology.** Nvidia · 2 March 2026
nvidianews.nvidia.com/news/nvidia-announces-strategic-partnership-with-lumentum-to-develop-state-of-the-art-optics-technology
2. A **Mineral Commodity Summaries 2026: Indium.** U.S. Geological Survey · 5 February 2026
pubs.usgs.gov/periodicals/mcs2026/mcs2026-indium.pdf
3. A **AXT, quarterly report on Form 10-Q for the quarter ended 30 June 2026.** U.S. Securities and Exchange Commission (filing by AXT) · 13 August 2026
www.sec.gov/Archives/edgar/data/1051627/000143774926027677/axti20260630_10q.htm
4. A **Nvidia, annual report on Form 10-K for the fiscal year ended 25 January 2026.** U.S. Securities and Exchange Commission (filing by Nvidia) · 25 February 2026
www.sec.gov/Archives/edgar/data/1045810/000104581026000021/nvda-20260125.htm
5. B **AI demand strains supplies of lasers, fiber and other optical tech.** Nikkei Asia · 27 May 2026
asia.nikkei.com/business/technology/tech-asia/ai-demand-strains-supplies-of-lasers-fiber-and-other-optical-tech
6. B **H100 vs GB200 NVL72 Training Benchmarks - Power, TCO, and Reliability Analysis, Software Improvement Over Time.** SemiAnalysis · 20 August 2025
newsletter.semianalysis.com/p/h100-vs-gb200-nvl72-training-benchmarks
7. A **Nvidia, quarterly report on Form 10-Q for the quarter ended 26 April 2026.** U.S. Securities and Exchange Commission (filing by Nvidia) · 20 May 2026
www.sec.gov/Archives/edgar/data/1045810/000104581026000052/nvda-20260426.htm
8. A **Broadcom, current report on Form 8-K dated 2 September 2026.** U.S. Securities and Exchange Commission (filing by Broadcom) · 2 September 2026
www.sec.gov/Archives/edgar/data/1730168/000173016826000076/avgo-08022026x8kxex99.htm
9. A **Hon Hai Technology Group (Foxconn) Announces FY2025 & 4Q25 Financial Results.** Hon Hai Precision Industry (Foxconn) · 16 March 2026
www.honhai.com/en-us/press-center/press-releases/latest-news/1978
10. A **InnoLight Technology, company overview page.** InnoLight Technology · Accessed 9 September 2026
www.innolight.com/about
11. A **NVIDIA and Coherent Announce Strategic Partnership to Develop Optics Technology to Scale Next-Generation Data Center Architecture.** Nvidia · 2 March 2026
nvidianews.nvidia.com/news/nvidia-and-coherent-announce-strategic-partnership-to-develop-optics-technology-to-scale-next-generation-data-center-architecture

¹⁰ InnoLight Technology, company overview page. InnoLight Technology, accessed 9 September 2026. [innolight.com](https://www.innolight.com)

12. A **UALink™ 200G 1.0 Specification Overview**. UALink Consortium · 15 May 2025
ualinkconsortium.org/blog/ualink-200g-1-0-specification-overview-802/
13. A **AAI 2026: AMD Launches AMD Helios Rackscale Solution for Frontier AI**. AMD Newsroom · 23 July 2026
newsroom.amd.com/news/aai-2026-helios-update/
14. A **NVIDIA Unveils NVLink Fusion for Industry to Build Semi-Custom AI Infrastructure With NVIDIA Partner Ecosystem**. Nvidia · 18 May 2025
nvidianews.nvidia.com/news/nvidia-nvlink-fusion-semi-custom-ai-infrastructure-partner-ecosystem
15. A **Coherent Announces a CHIPS Letter of Intent for \$50 Million to Expand World-Leading Manufacturing Facility for AI Infrastructure**. Coherent · 16 June 2026
www.coherent.com/news/press-releases/a-chip-letter-of-intent-for-50m-to-expand-world-leading-manufacturing-facility-for-ai-infrastructure
16. A **NVIDIA and Partners Build in America, for America**. Nvidia · 5 August 2026
blogs.nvidia.com/blog/nvidia-and-partners-build-in-america-for-america/
17. A **System Hardware & Components**. Nvidia · Accessed 9 September 2026
docs.nvidia.com/enterprise-reference-architectures/nv172-ai-factory/latest/components.html
18. A **NVIDIA, Partners Drive Next-Gen Efficient Gigawatt AI Factories in Buildup for Vera Rubin**. Nvidia · 13 October 2025
blogs.nvidia.com/blog/gigawatt-ai-factories-ocp-vera-rubin
19. A **Credo Technology Group, annual report on Form 10-K for the fiscal year ended 2 May 2026**. U.S. Securities and Exchange Commission (filing by Credo Technology Group) · 15 June 2026
www.sec.gov/Archives/edgar/data/1807794/000162828026043303/crdo-20260502.htm
20. B **Co-Packaged Optics (CPO) Book – Scaling with Light for the Next Wave of Interconnect**. SemiAnalysis · 1 January 2026
newsletter.semianalysis.com/p/co-packaged-optics-cpo-book-scaling
21. A **Parallelisms Guide – Megatron Bridge**. Nvidia · Accessed 9 September 2026
docs.nvidia.com/nemo-framework/user-guide/latest/nemotoolkit/features/parallelisms.html
22. A **NVLink & NVLink Switch for Advanced Multi-GPU Communication**. Nvidia · 20 April 2026
www.nvidia.com/en-us/data-center/nvlink/
23. A **NVIDIA Kicks Off the Next Generation of AI With Rubin**. Nvidia · 5 January 2026
nvidianews.nvidia.com/news/rubin-platform-ai-supercomputer
24. A **Inside the Ironwood TPU codesigned AI stack**. Google Cloud · 6 November 2025
cloud.google.com/blog/products/compute/inside-the-ironwood-tpu-codesigned-ai-stack
25. A **Broadcom Ships Tomahawk 4, Industry's Highest Bandwidth Ethernet Switch Chip at 25.6 Terabits per Second**. Broadcom · 9 December 2019
investors.broadcom.com/news-releases/news-release-details/broadcom-ships-tomahawk-4-industrys-highest-bandwidth-ethernet
26. A **Broadcom Ships Tomahawk 5, Industry's Highest Bandwidth Switch Chip to Accelerate AI/ML Workloads**. Broadcom · 16 August 2022
investors.broadcom.com/news-releases/news-release-details/broadcom-ships-tomahawk-5-industrys-highest-bandwidth-switch
27. A **Broadcom Ships Tomahawk 6: World's First 102.4 Tbps Switch**. Broadcom · 3 June 2025
investors.broadcom.com/news-releases/news-release-details/broadcom-ships-tomahawk-6-worlds-first-1024-tbps-switch
28. A **Ultra Ethernet Consortium (UEC) Launches Specification 1.0 Transforming Ethernet for AI and HPC at Scale**. Ultra Ethernet Consortium · 11 June 2025
ultraethernet.org/ultra-ethernet-consortium-uec-launches-specification-1-0-transforming-ethernet-for-ai-and-hpc-at-scale/
29. A **Nvidia, quarterly report on Form 10-Q for the quarter ended 26 July 2026**. U.S. Securities and Exchange Commission (filing by Nvidia) · 26 August 2026
www.sec.gov/Archives/edgar/data/1045810/000104581026000075/nvda-20260726.htm
30. A **Broadcom Announces Tomahawk 6 – Davisson, the Industry's First 102.4-Tbps Ethernet Switch with Co-Packaged Optics**. Broadcom · 8 October 2025
investors.broadcom.com/news-releases/news-release-details/broadcom-announces-tomahawk-6-davisson-industrys-first-1024
31. A **NVIDIA Announces Spectrum-X Photonics, Co-Packaged Optics Networking Switches to Scale AI Factories to Millions of GPUs**. Nvidia · 18 March 2025
nvidianews.nvidia.com/news/nvidia-spectrum-x-co-packaged-optics-networking-switches-ai-factories
32. A **NVIDIA Announces Financial Results for Second Quarter Fiscal 2027**. Nvidia · 26 August 2026
nvidianews.nvidia.com/news/nvidia-announces-financial-results-for-second-quarter-fiscal-2027
33. A **Eoptolink Technology, contacts page**. Eoptolink Technology · Accessed 9 September 2026
www.eoptolink.com/about-us/contacts
34. A **Protecting Against National Security Threats to the Communications Supply Chain through the Equipment Authorization Program: Third Report and Order and Third Further Notice of Proposed Rulemaking (FCC-26-50)**. U.S. Federal Communications Commission · 23 July 2026 · p. 3
docs.fcc.gov/public/attachments/FCC-26-50A1.pdf#page=3
35. A **Protecting Against National Security Threats to the Communications Supply Chain through the Equipment Authorization Program: Third Report and Order and Third Further Notice of Proposed Rulemaking (FCC-26-50)**. U.S. Federal Communications Commission · 23 July 2026 · p. 6
docs.fcc.gov/public/attachments/FCC-26-50A1.pdf#page=6
36. A **Protecting Against National Security Threats to the Communications Supply Chain through the Equipment Authorization Program: Third Report and Order and Third Further Notice of Proposed Rulemaking (FCC-26-50)**. U.S. Federal Communications Commission · 23 July 2026 · p. 13
docs.fcc.gov/public/attachments/FCC-26-50A1.pdf#page=13
37. A **Protecting Against National Security Threats to the Communications Supply Chain through the Equipment Authorization Program: Third Report and Order and Third Further Notice of Proposed Rulemaking (FCC-26-50)**. U.S. Federal Communications Commission · 23 July 2026 · p. 10
docs.fcc.gov/public/attachments/FCC-26-50A1.pdf#page=10

38. A **List of Equipment and Services Covered By Section 2 of The Secure Networks Act.** U.S. Federal Communications Commission · 16 October 2026
www.fcc.gov/supplychain/coveredlist
39. A **Broadcom, annual report on Form 10-K for the fiscal year ended 2 November 2025.** U.S. Securities and Exchange Commission (filing by Broadcom) · 18 December 2025
www.sec.gov/Archives/edgar/data/1730168/000173016825000121/avgo-20251102.htm
40. A **Marvell Technology, annual report on Form 10-K for the fiscal year ended 31 January 2026.** U.S. Securities and Exchange Commission (filing by Marvell Technology) · 11 March 2026
www.sec.gov/Archives/edgar/data/1835632/000183563226000011/mrvl-20260131.htm
41. A **Marvell Technology, current report on Form 8-K dated 2 December 2024.** U.S. Securities and Exchange Commission (filing by Marvell Technology) · 2 December 2024
www.sec.gov/Archives/edgar/data/1835632/000183563224000193/final2024_12x02xmarvell-.htm
42. A **NVIDIA to Manufacture American-Made AI Supercomputers in US for First Time.** Nvidia · 14 April 2025
blogs.nvidia.com/blog/nvidia-manufacture-american-made-ai-supercomputers-us/
43. A **TTM Technologies, annual report on Form 10-K for the fiscal year ended 29 December 2025.** U.S. Securities and Exchange Commission (filing by TTM Technologies) · 17 February 2026
www.sec.gov/Archives/edgar/data/1116942/000119312526051976/ttmi-20251229.htm
44. A **Nittobo Group Integrated Report 2025.** Nitto Boseki (Nittobo) · 16 September 2025 · p. 7
www.nittobo.co.jp/eng/ir/pdf/Nittobo_Integrated-Report_2025.pdf#page=7



01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Data Centers and Power

SemiAnalysis forecast in October 2026 that 50 GW of data center capacity would be added in 2027, about as much as the world had built through 2024. The large transformers that connect such sites to the grid commonly took three years to arrive in 2024.

Specimen 14 · Data Centers and Power

A liquid-cooled rack of 72 GPUs, Nvidia's GB200 NVL72, drawn to scale. It is 2.24 m tall and 600 mm wide, taller than a door. It weighs about 1.36 metric tons, more than a small car, and draws about 120 kW. The newer GB300 NVL72 draws up to 142 kW. The gray steel power shelves and the copper busbar they feed are picked out.

In plain terms

A data center feeds electricity to the machines inside it and carries away the heat they give off. One rack of AI chips, a cabinet taller than a door, can draw 142 kilowatts¹. Every watt of it comes back out as heat, and liquid piped through the rack carries the heat away¹. A large training site already holds more than a hundred thousand chips². The newest sites are planned in gigawatts³. One gigawatt is the whole output of a large power station, and Epoch AI projects that OpenAI's seven Stargate sites in the United States will add up to more than nine of them by 2029³. Getting that much electricity to the site is harder than putting up the building. Transformers and heavy switches connect a site to the grid, and turbines make the power. All of them come from a few suppliers and take years to arrive.

In short

Measured by capacity, US factories supplied 29.2 percent of the large power transformers bought in the US in 2023, and imports the rest⁴. GE Vernova's gas equipment backlog and reserved factory slots stood at 116 GW in mid-2026, against planned output of 20 GW a year from the third quarter⁵.

ERCOT, the grid operator for most of Texas, counted 9,456 MW of big power users approved to energize in its overview for September 2026⁶. Judging by

¹ System Hardware & Components. Nvidia, accessed 9 September 2026. docs.nvidia.com

² Colossus 1, AI data centers directory. Epoch AI, accessed 9 September 2026. epoch.ai

³ OpenAI Stargate: where the US sites stand. Epoch AI, 17 April 2026. epoch.ai

⁴ Large Power Transformers from South Korea, Investigation No. 731-TA-1189... U.S. International Trade Commission, August 2024, p. 90. usitc.gov

⁵ GE Vernova, current report on Form 8-K dated 22 July 2026. U.S. Securities and Exchange Commission, 22 July 2026. sec.gov

⁶ Electric Reliability Council of Texas, ERCOT Monthly Operational Overview... Electric Reliability Council of Texas, 16 October 2026, p. 9. ercot.com

peak monthly use in September, it believed 4,132 MW of that was operating⁶. On 3 August 2026 Governor Greg Abbott ordered an audit of every data center seeking a connection before any data center project moves forward⁷. In September 2026 ERCOT said it had paused approvals to energize data centers of 75 MW or more until the audit and a review of their impact on local communities are complete⁸.

A wafer passes through a leading-edge fab in months, but in 2024 a large power transformer commonly took three years to arrive⁹. Before the pandemic, the same order took under a year¹⁰.

Chokepoint card		Data Centers and Power			
<div>Concentration</div> <div> High</div> <div>Four to six firms could supply this stage today, and the top two take most of the revenue.</div>		<div>Substitutability</div> <div>Moderate</div> <div>Nvidia named nine data center power system providers in October 2025 for its 800-volt designs for gigawatt-scale data centers¹¹.</div>		<div>Price or market size</div> <div>\$580 billion</div> <div>of data center investment expected worldwide in 2025, in the International Energy Agency's November 2025 outlook¹²</div>	
Who leads	US	GE Vernova	Gas equipment, transformers and switchgear, including through Prolec GE ¹³		
	CH	Hitachi Energy	Power transformers and switchgear ¹³		
	DE	Siemens Energy	Grid technologies, transformers, turbines ¹³		
	JP	Mitsubishi Power	Power generation equipment, including gas turbines ¹³		
	US	Vertiv	Data center power systems ¹¹		
	FR	Schneider Electric	Cooling, through its Motivair division ¹⁴		
Where it is made	US	United States	The largest data center operators, and GE Vernova turbines and grid equipment		
	CH	Switzerland	Hitachi Energy transformers and switchgear, and ABB switchgear		
	DE	Germany	Siemens Energy grid technologies and turbines		
	JP	Japan	Mitsubishi Power equipment, including gas turbines		
Why substitution is possible	Buyers of grid equipment can choose among suppliers, and GE Vernova's 2025 annual report names Hitachi Energy, Siemens Energy, Schneider Electric and ABB among its key competitors ¹³ . But in the United States in 2024 the longest large power transformer lead times reached 60 months ⁹ . An International Energy Agency survey published in 2025 found waits of up to four years worldwide ¹⁵ .				

6 Electric Reliability Council of Texas, ERCOT Monthly Operational Overview... Electric Reliability Council of Texas, 16 October 2026, p. 9. [ercot.com](#)

7 Governor Abbott Directs Comprehensive Data Center Audit. Office of the Texas Governor, 3 August 2026. [gov.texas.gov](#)

8 Electric Reliability Council of Texas, Item 14: Batch Zero Update, Board of... Electric Reliability Council of Texas, 11 September 2026. [ercot.com](#)

9 U.S. Department of Energy Large Power Transformer Resilience Report to... U.S. Department of Energy, 10 July 2024, p. 8. [energy.gov](#)

10 U.S. Department of Energy Large Power Transformer Resilience Report to... U.S. Department of Energy, 10 July 2024, p. 18. [energy.gov](#)

11 NVIDIA, Partners Drive Next-Gen Efficient Gigawatt AI Factories in Buildup for... Nvidia, 13 October 2025. [blogs.nvidia.com](#)

12 Executive summary – World Energy Outlook 2025. International Energy Agency, 12 November 2025. [iea.org](#)

13 GE Vernova, annual report on Form 10-K for the fiscal year ended 31 December... U.S. Securities and Exchange Commission, 29 January 2026. [sec.gov](#)

14 Hotter Than a Hot Tub: The 45°C Breakthrough to Cool AI's Biggest Machines. Nvidia, 22 June 2026. [blogs.nvidia.com](#)

15 Executive summary – Building the Future Transmission Grid. International Energy Agency, 2025. [iea.org](#)

Where China stands

China used 25 percent of the world's data center electricity in 2024, second to the United States, by the International Energy Agency's estimate¹⁶. Data centers made up around 3 percent of the growth in China's electricity demand from 2022 to 2024¹⁷.

Where the US stands

US factories supplied 29.2 percent of the large power transformers bought in the United States in 2023, measured by capacity⁴. Constellation said in August 2026 that it expects to restart the Crane nuclear plant in 2027¹⁸. Microsoft has agreed to buy the plant's power¹⁹.

01

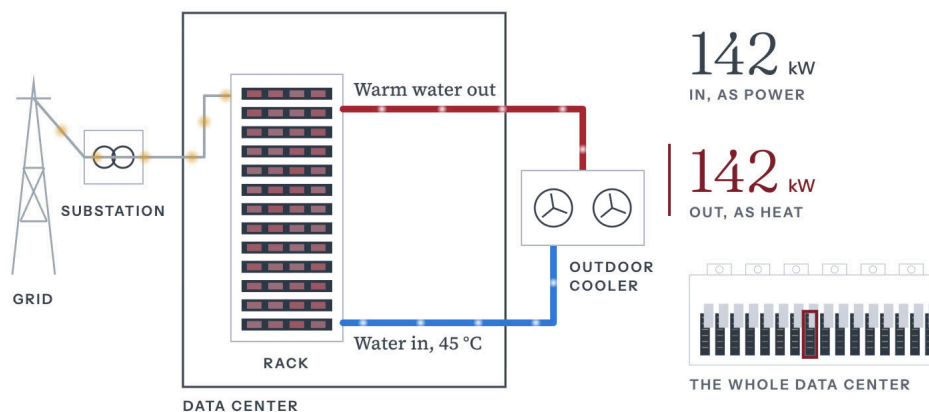
How AI data centers are powered and cooled

Figure 14.1 · Explainer, 21 seconds

Power in, heat out

Water carries the heat away

Nvidia plans racks of a megawatt from 2027



- The site.** Data centers are where AI chips go to work. A large training site holds a hundred thousand of them, in rows of racks.
- Power in.** Power comes in from the grid, stepped down by a substation, and runs through the data center to every rack. One rack of AI chips can draw 142 kilowatts.
- Heat.** Every watt of it comes back out as heat, more than air can carry away.
- Water out.** So water runs through plates on the chips, carries the heat to coolers outdoors and comes back. Nvidia plans for racks of a megawatt each from 2027, so the power coming in and the heat going out keep growing.

Note: Simplified diagram, with illustrative sizes. An Nvidia GB300 NVL72 rack draws at most 142 kW. Nvidia gives 45 °C as the supply-water temperature for its Vera Rubin racks. The megawatt racks from 2027 are Nvidia's plan.

The rack is the basic unit of AI compute. Nvidia's GB300 NVL72 rack draws up to 142 kW through eight 33 kW power shelves, the rack's own power supplies¹. Large sites hold

¹ System Hardware & Components. Nvidia, accessed 9 September 2026. docs.nvidia.com

⁴ Large Power Transformers from South Korea, Investigation No. 731-TA-1189... U.S. International Trade Commission, August 2024, p. 90. usitc.gov

¹⁶ Executive summary – Energy and AI. International Energy Agency, 10 April 2025. iea.org

¹⁷ Executive summary – Electricity 2025. International Energy Agency, 14 February 2025. iea.org

¹⁸ Constellation Reports Second Quarter 2026 Results. Constellation Energy, 6 August 2026. constellationenergy.com

¹⁹ Constellation Ahead of Schedule for Launch of Crane Clean Energy Center. Constellation Energy, 19 February 2025. constellationenergy.com

many such racks. Colossus 1, an AI data center in Memphis, Tennessee, held an estimated 230,000 Nvidia GPUs by July 2025².

Power reaches the rack through a chain of heavy equipment, and each piece has its own lead time, the wait between order and delivery. Between the grid and the rack, a substation steps the high voltage down with transformers. Switchgear, the building's heavy circuit breakers, can cut any part of the site off in a fault. Battery-backed supplies keep the racks running for the seconds it takes backup generators to start. Distribution boards split the feed among the rows of racks.

At the back of each rack, a busbar carries the current down to the server trays. It is a solid copper bar, because an ordinary cable would overheat at that current.

Heat leaves in water. Cold plates, metal blocks with coolant running through them, sit on the GPU packages and pass the heat to the building's water loop, which releases it outdoors¹⁴. Nvidia's Rubin racks run coolant at up to 45 °C, warm enough that in many climates the loop can release its heat without turning on chillers, the refrigeration machines that cool water¹⁴.

Nvidia is also moving the power that feeds its racks to 800 volts of direct current. Raising the voltage cuts the current needed for the same power, and the heat in copper comes from current. Nvidia said in October 2025 that at 800 volts the same wire can carry 157 percent more power than at 415 volts of alternating current²⁰. Inside racks such as the GB300 NVL72, power runs at 54 volts, and at that voltage a one-megawatt rack would need up to 200 kg of copper busbar²¹.

02

Cooling and power options

Cooling

- **Air.** Heat exchangers in the rack door work when density, the power each rack draws, is moderate, but Nvidia's GB300 NVL72 rack is liquid cooled¹.
- **Direct-to-chip liquid.** Nvidia's Rubin platform is 100 percent liquid cooled, and Nvidia says every cloud provider and data center operator building for it is moving to liquid¹⁴.
- **Immersion.** The servers sit in a bath of fluid, which makes them hard to service.

Nvidia says the cooling supply chain is keeping pace with the move to liquid¹⁴. Motivair, Schneider Electric's cooling division, has worked with Nvidia for nearly a decade, following Nvidia's product roadmap¹⁴.

Rack power

Nvidia's 800-volt DC architecture is designed for racks from 100 kW to more than a megawatt, with megawatt racks from 2027²¹. Nvidia is making the change because the

¹ System Hardware & Components. Nvidia, accessed 9 September 2026. docs.nvidia.com

² Colossus 1, AI data centers directory. Epoch AI, accessed 9 September 2026. epoch.ai

¹⁴ Hotter Than a Hot Tub: The 45°C Breakthrough to Cool AI's Biggest Machines. Nvidia, 22 June 2026. blogs.nvidia.com

²⁰ Building the 800 VDC Ecosystem for Efficient, Scalable AI Factories. Nvidia, 13 October 2025. developer.nvidia.com

²¹ NVIDIA 800 VDC Architecture Will Power the Next Generation of AI Factories. Nvidia, 20 May 2025. developer.nvidia.com

54-volt distribution in existing racks begins to hit physical limits once racks exceed 200 kW²¹.

Nvidia names nine data center power system providers for its 800-volt designs for gigawatt-scale data centers, among them ABB, Eaton, Hitachi Energy, Mitsubishi Electric, Schneider Electric, Siemens and Vertiv¹¹.

A megawatt rack changes the busbar, the floor loading, the coolant flow, the leak detection and the energy stored in the rack. Nvidia's Vera Rubin NVL72 rack design adds energy storage to keep power steady¹¹.

Where the electrons come from

- **Grid interconnection.** The slow path in the United States, where the queues to connect are long³.
- **Behind-the-meter gas,** generation on the site itself. The fast path, which at least three of OpenAI's seven US Stargate sites will use to avoid grid queues³.
- **Nuclear.** Existing plants already sell power to data centers²². Talen Energy supplies Amazon's data center campus next to the Susquehanna nuclear plant in Pennsylvania under a June 2025 contract expected to reach 1,920 MW no later than 2032²². Restarts and new reactors are still to come. Constellation signed a power purchase agreement with Microsoft to restart Three Mile Island Unit 1 as the 835 MW Crane Clean Energy Center¹⁹. The plant shut in 2019²³. A \$1 billion federal loan that closed in November 2025 partly finances its restart, which is subject to licensing approvals from the US Nuclear Regulatory Commission²³.

03

Data center spending and power equipment makers

The largest data center operators pay for the buildout. Capital spending by Alphabet, Amazon, Meta, Microsoft and Oracle came to \$448.2 billion in 2025, the sum of quarterly figures compiled by Epoch AI, a research group²⁴. If the trend continues, it will reach \$770 billion in 2026²⁴. The International Energy Agency expected worldwide investment in data centers to reach \$580 billion in 2025¹².

³ OpenAI Stargate: where the US sites stand. Epoch AI, 17 April 2026. epoch.ai

¹¹ NVIDIA, Partners Drive Next-Gen Efficient Gigawatt AI Factories in Buildup for... Nvidia, 13 October 2025. blogs.nvidia.com

¹² Executive summary – World Energy Outlook 2025. International Energy Agency, 12 November 2025. iea.org

¹⁹ Constellation Ahead of Schedule for Launch of Crane Clean Energy Center. Constellation Energy, 19 February 2025. constellationenergy.com

²¹ NVIDIA 800 VDC Architecture Will Power the Next Generation of AI Factories. Nvidia, 20 May 2025. developer.nvidia.com

²² Talen Energy, current report on Form 8-K dated 11 June 2025. U.S. Securities and Exchange Commission, 11 June 2025. sec.gov

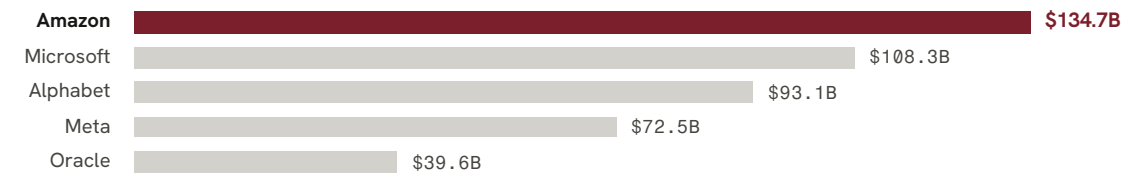
²³ Energy Department Closes Loan to Restart Nuclear Power Plant in Pennsylvania. U.S. Department of Energy, 17 November 2025. energy.gov

²⁴ Hyperscaler capex has quadrupled since GPT-4's release. Epoch AI, 26 February 2026. epoch.ai

Figure 14.2

Amazon spent the most of five large operators, \$134.7 billion in 2025

Capital spending by five large US data center operators, 2025



Source: Epoch AI, hyperscaler capex trend, February 2026, quarterly figures from company filings summed for 2025 [24]

Epoch AI also projects that OpenAI's seven US Stargate sites will exceed 9 GW by 2029³. It expects the site in Abilene, Texas, to grow from an estimated 0.3 GW in April 2026 to 1.2 GW in the fourth quarter of 2026³.

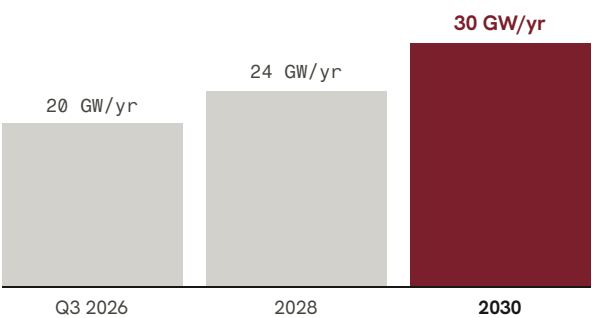
A few large firms make the turbines, transformers and switchgear. GE Vernova builds large gas turbines, and its 2025 annual report names Siemens Energy and Mitsubishi Power among the key competitors of its power generation business¹³. Its electrification business makes power transformers and switchgear, and the report names Hitachi Energy, Siemens Energy, Schneider Electric and ABB among that business's key competitors¹³.

Equipment makers limit how fast the buildout can go. GE Vernova's gas equipment backlog and reserved factory slots grew from 100 GW to 116 GW in the second quarter of 2026⁵. In the first half of 2026, data center orders for its electrification business, which makes grid equipment, passed \$5 billion, more than double that business's data center orders for all of 2025⁵. GE Vernova bought the remaining half of Prolec GE, a transformer maker, in the first half of 2026⁵.

Figure 14.3

GE Vernova plans 30 GW of annual gas turbine output in 2030

GE Vernova's planned annual gas turbine output



Source: GE Vernova second-quarter 2026 results, July 2026 [5]

³ OpenAI Stargate: where the US sites stand. Epoch AI, 17 April 2026. epoch.ai

⁵ GE Vernova, current report on Form 8-K dated 22 July 2026. U.S. Securities and Exchange Commission, 22 July 2026. sec.gov

¹³ GE Vernova, annual report on Form 10-K for the fiscal year ended 31 December... U.S. Securities and Exchange Commission, 29 January 2026. sec.gov

²⁴ Hyperscaler capex has quadrupled since GPT-4's release. Epoch AI, 26 February 2026. epoch.ai

Data center electricity demand forecasts

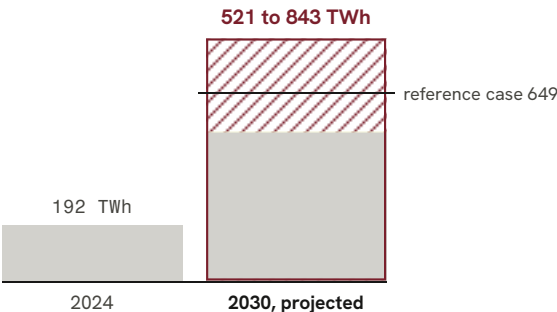
US data center electricity use is projected to rise steeply by 2030. US data centers used 192 TWh in 2024, 4.7 percent of national electricity, according to a June 2026 estimate by Lawrence Berkeley National Laboratory that leaves out cryptocurrency mining²⁵. The lab's reference case, its main scenario, projects 464 TWh in 2028 and 649 TWh in 2030, which would be 11.8 percent of forecast US electricity use²⁵. Its scenarios for 2030 range from 521 to 843 TWh, or 9.5 percent to 15.3 percent²⁶.

The US Energy Information Administration expects electricity demand to keep rising, but in September 2026 it cut its 2027 forecast for the region that includes Texas. In its October 2026 Short-Term Energy Outlook, it expects US electricity sales of 4,152.0 TWh in 2026 and 4,216.6 TWh in 2027²⁷. It expects electricity demand from the commercial sector, which includes data centers, to grow 2.8 percent in 2027 and demand from industry to grow 2.7 percent²⁸. Its September outlook had lowered the 2027 electricity sales forecast for the region that includes Texas by 4.7 percent from August²⁹. That outlook noted that Texas had paused connecting new data centers to the grid while the state audits proposed projects³⁰. The pause, set by the grid operator for most of Texas, covers data centers and crypto mining sites of 75 MW or more⁸.

Figure 14.4

US data centers' projected 2030 use ranges from 521 to 843 TWh

US data center electricity use, 2024 and 2030 projection range



Source: Lawrence Berkeley National Laboratory, June 2026 [26]

By the International Energy Agency's estimate, China accounted for 25 percent of the world's data center electricity use in 2024, second to the United States at 45 percent¹⁶. Data centers made up around 3 percent of the growth in China's electricity demand from 2022 to 2024, the agency found¹⁷.

8 Electric Reliability Council of Texas, Item 14: Batch Zero Update, Board of... Electric Reliability Council of Texas, 11 September 2026. ercot.com

16 Executive summary – Energy and AI. International Energy Agency, 10 April 2025. iea.org

17 Executive summary – Electricity 2025. International Energy Agency, 14 February 2025. iea.org

25 United States Data Center Energy Usage Report: 2025 Update. Lawrence Berkeley National Laboratory, 18 June 2026, p. 10. energy.gov

26 United States Data Center Energy Usage Report: 2025 Update. Lawrence Berkeley National Laboratory, 18 June 2026, p. 11. energy.gov

27 Short-Term Energy Outlook, October 2026. U.S. Energy Information Administration, 6 October 2026, p. 46. eia.gov

28 Short-Term Energy Outlook, October 2026. U.S. Energy Information Administration, 6 October 2026, p. 12. eia.gov

29 Short-Term Energy Outlook, September 2026. U.S. Energy Information Administration, 8 September 2026, p. 4. eia.gov

30 Short-Term Energy Outlook, September 2026. U.S. Energy Information Administration, 8 September 2026, p. 10. eia.gov

SemiAnalysis, a research firm, forecast in October 2026 that 50 GW of data center capacity would be added in 2027, which it said was about as much as the world's data center market had built in total through 2024³¹. Just 40 campuses in an advanced stage of construction held more than 24 GW, most of it to be delivered in 2027, it found³¹.

Better chips do not by themselves cut total energy use. Google says its Ironwood TPU, an AI chip, delivers twice the performance per watt of Trillium, the TPU before it³². A token is the chunk of text a model reads or writes. Energy per token can fall while total energy use still rises, if the number of tokens rises faster.

05

Long waits for grid power and equipment

On the Texas grid, big power users have asked for far more electricity than is connected and running. ERCOT, the grid operator for most of Texas, was tracking about 474 GW of large loads (big power users) seeking a connection in June 2026, roughly 90 percent of it data centers³³. In its operational overview for September 2026, ERCOT counted 9,456 MW of large loads approved to energize, that is, cleared to switch on⁶. Judging by peak monthly use in September, it believed only 4,132 MW of it was operating⁶.

Before a big user can connect, engineers must study whether the nearby grid can carry its load. In a preliminary review in July 2026, ERCOT found that about 205 GW of the requests already had such a study, which made them eligible for Batch Zero, the first batch of requests it studies together³⁴. In September 2026 ERCOT conditionally classed 66.4 GW of Batch Zero projects as base load and 127.9 GW as studied load, pending final decisions in December⁸. Under ERCOT's Batch Zero rules, base load is demand from projects already running or far enough along to be counted without further study³⁵. Studied load is demand that ERCOT will study before giving each project a share of the grid's capacity³⁵.

Texas has paused new connections for large data centers while it audits them. On 3 August 2026 Texas Governor Greg Abbott ordered the state's Public Utility Commission and ERCOT to audit every data center waiting to connect to the grid before any data center project moves forward⁷. ERCOT then paused approvals to energize data centers and crypto mining sites of 75 MW or more until the audit and a review of their impact on local communities are complete⁸. It will report on the audit and the community review to the Public Utility Commission by 10 December 2026⁸.

Projects in that queue also wait on equipment.

⁶ Electric Reliability Council of Texas, ERCOT Monthly Operational Overview... Electric Reliability Council of Texas, 16 October 2026, p. 9. ercot.com

⁷ Governor Abbott Directs Comprehensive Data Center Audit. Office of the Texas Governor, 3 August 2026. gov.texas.gov

⁸ Electric Reliability Council of Texas, Item 14: Batch Zero Update, Board of... Electric Reliability Council of Texas, 11 September 2026. ercot.com

³¹ Datacenters 2027: The Year of Acceleration, +50GW in a Single Year. SemiAnalysis, 19 October 2026. newsletter.semianalysis.com

³² Inside the Ironwood TPU codigned AI stack. Google Cloud, 6 November 2025. cloud.google.com

³³ Electric Reliability Council of Texas, ERCOT update to the Senate Committee on... Electric Reliability Council of Texas, 29 July 2026, p. 6. ercot.com

³⁴ Electric Reliability Council of Texas, ERCOT update to the Senate Committee on... Electric Reliability Council of Texas, 29 July 2026, p. 10. ercot.com

³⁵ ercot.com

- **Large power transformers.** In the United States in 2024, lead times of 36 months were commonly quoted and the longest reached 60 months, against under a year before the pandemic⁹. By a US Commerce Department estimate, 82 percent of the units put into US service in 2019 were imported³⁶. In an industry survey published in 2025, the International Energy Agency found that large power transformers took up to four years to secure worldwide¹⁵. It also found that their average lead times had almost doubled since 2021¹⁵. A transformer's size is given as a power rating in megavolt-amperes (MVA)⁹. Measured by capacity, US factories supplied 29.2 percent of the transformers rated 60 MVA and above bought in the US in 2023, and imports supplied the rest⁴.
- **Gas turbines.** GE Vernova's gas equipment backlog and reserved factory slots stood at 116 GW in mid-2026⁵. In July 2026 it expected to build gas turbines at a yearly rate of 20 GW in the third quarter of 2026, 24 GW in 2028 and 30 GW in 2030⁵.
- **Firm generation,** the kind that runs whatever the weather. The Nuclear Regulatory Commission has approved a fuel license amendment for the Crane plant¹⁸. Constellation called the approval a major milestone toward restarting the plant in 2027¹⁸.

Memory chips are also in short supply. Micron's quarterly report for the period ended 28 May 2026 says AI-driven growth in demand for memory and storage is outpacing industry supply³⁷. The memory shortage and the wait for power equipment both limit how much of the 2026 capital spending turns into working compute.

Four questions to answer from memory

1. What does a data center do for AI chips? see [How it works](#)
 2. Why are AI racks cooled with liquid? see [How it works](#)
 3. How big are the newest AI data centers? see [How it works](#)
 4. What slows down building an AI data center?
-

Four things to remember

- One AI rack can draw 142 kilowatts, too much heat for air, so racks are cooled with liquid.
- The newest AI sites are planned in gigawatts, and each gigawatt is the output of a large power station.
- Power equipment is one of the slow parts of building a data center. In 2024 lead times of 36 months were commonly quoted for a large transformer.
- The United States used 45 percent of the world's data center electricity in 2024 and China 25 percent, by the International Energy Agency's estimate.

⁴ Large Power Transformers from South Korea, Investigation No. 731-TA-1189... U.S. International Trade Commission, August 2024, p. 90. [usitc.gov](#)

⁵ GE Vernova, current report on Form 8-K dated 22 July 2026. U.S. Securities and Exchange Commission, 22 July 2026. [sec.gov](#)

⁹ U.S. Department of Energy Large Power Transformer Resilience Report to... U.S. Department of Energy, 10 July 2024, p. 8. [energy.gov](#)

¹⁵ Executive summary – Building the Future Transmission Grid. International Energy Agency, 2025. [iea.org](#)

¹⁸ Constellation Reports Second Quarter 2026 Results. Constellation Energy, 6 August 2026. [constellationenergy.com](#)

³⁶ U.S. Department of Energy Large Power Transformer Resilience Report to... U.S. Department of Energy, 10 July 2024, p. 20. [energy.gov](#)

³⁷ Micron Technology, quarterly report on Form 10-Q for the quarter ended 28 May... U.S. Securities and Exchange Commission, 25 June 2026. [sec.gov](#)

Sources (37)

1. A **System Hardware & Components**. Nvidia · Accessed 9 September 2026
docs.nvidia.com/enterprise-reference-architectures/nv172-ai-factory/latest/components.html
2. A **Colossus 1, AI data centers directory**. Epoch AI · Accessed 9 September 2026
epoch.ai/data/ai-data-centers/directory/colossus-1
3. A **OpenAI Stargate: where the US sites stand**. Epoch AI · 17 April 2026
epoch.ai/publications/openai-stargate-where-the-us-sites-stand
4. A **Large Power Transformers from South Korea, Investigation No. 731-TA-1189 (Second Review), Publication 5531**. U.S. International Trade Commission · August 2024 · p. 90
www.usitc.gov/publications/701_731/pub5531.pdf#page=90
5. A **GE Vernova, current report on Form 8-K dated 22 July 2026**. U.S. Securities and Exchange Commission (filing by GE Vernova) · 22 July 2026
www.sec.gov/Archives/edgar/data/1996810/000199681026000147/gevpressrelease2q26.htm
6. A **Electric Reliability Council of Texas, ERCOT Monthly Operational Overview (September 2026)**. Electric Reliability Council of Texas · 16 October 2026 · p. 9
www.ercot.com/files/docs/2026/10/16/ERCOT-Monthly-Operational-Overview-September.pdf#page=9
7. A **Governor Abbott Directs Comprehensive Data Center Audit**. Office of the Texas Governor · 3 August 2026
gov.texas.gov/news/post/governor-abbott-directs-comprehensive-data-center-audit
8. A **Electric Reliability Council of Texas, Item 14: Batch Zero Update, Board of Directors meeting, 14-15 September 2026**. Electric Reliability Council of Texas · 11 September 2026
www.ercot.com/files/docs/2026/09/11/14-Batch-Zero-Update.pdf
9. A **U.S. Department of Energy Large Power Transformer Resilience Report to Congress, July 2024**. U.S. Department of Energy · 10 July 2024 · p. 8
www.energy.gov/sites/default/files/2024-10/EXEC-2022-001242%20-%20Large%20Power%20Transformer%20Resilience%20Report%20signed%20by%20Secretary%20Granholm%20on%207-10-24.pdf#page=8
10. A **U.S. Department of Energy Large Power Transformer Resilience Report to Congress, July 2024**. U.S. Department of Energy · 10 July 2024 · p. 18
www.energy.gov/sites/default/files/2024-10/EXEC-2022-001242%20-%20Large%20Power%20Transformer%20Resilience%20Report%20signed%20by%20Secretary%20Granholm%20on%207-10-24.pdf#page=18
11. A **NVIDIA, Partners Drive Next-Gen Efficient Gigawatt AI Factories in Buildup for Vera Rubin**. Nvidia · 13 October 2025
blogs.nvidia.com/blog/gigawatt-ai-factories-ocp-vera-rubin
12. A **Executive summary – World Energy Outlook 2025**. International Energy Agency · 12 November 2025
www.iea.org/reports/world-energy-outlook-2025/executive-summary
13. A **GE Vernova, annual report on Form 10-K for the fiscal year ended 31 December 2025**. U.S. Securities and Exchange Commission (filing by GE Vernova) · 29 January 2026
www.sec.gov/Archives/edgar/data/1996810/000199681026000015/gev-20251231.htm
14. A **Hotter Than a Hot Tub: The 45°C Breakthrough to Cool AI's Biggest Machines**. Nvidia · 22 June 2026
blogs.nvidia.com/blog/liquid-cooling-ai-factories/
15. A **Executive summary – Building the Future Transmission Grid**. International Energy Agency · 2025
www.iea.org/reports/building-the-future-transmission-grid/executive-summary
16. A **Executive summary – Energy and AI**. International Energy Agency · 10 April 2025
www.iea.org/reports/energy-and-ai/executive-summary
17. A **Executive summary – Electricity 2025**. International Energy Agency · 14 February 2025
www.iea.org/reports/electricity-2025/executive-summary
18. A **Constellation Reports Second Quarter 2026 Results**. Constellation Energy · 6 August 2026
www.constellationenergy.com/news/2026/08/constellation-reports-second-quarter-2026-results.html
19. A **Constellation Ahead of Schedule for Launch of Crane Clean Energy Center**. Constellation Energy · 19 February 2025
www.constellationenergy.com/news/2025/constellation-ahead-of-schedule-for-launch-of-crane-clean-energy-center.html
20. A **Building the 800 VDC Ecosystem for Efficient, Scalable AI Factories**. Nvidia · 13 October 2025
developer.nvidia.com/blog/building-the-800-vdc-ecosystem-for-efficient-scalable-ai-factories/
21. A **NVIDIA 800 VDC Architecture Will Power the Next Generation of AI Factories**. Nvidia · 20 May 2025
developer.nvidia.com/blog/nvidia-800-v-hvdc-architecture-will-power-the-next-generation-of-ai-factories/
22. A **Talen Energy, current report on Form 8-K dated 11 June 2025**. U.S. Securities and Exchange Commission (filing by Talen Energy) · 11 June 2025
www.sec.gov/Archives/edgar/data/1622536/000162253625030559/a20250611pressreleasebusin.htm
23. A **Energy Department Closes Loan to Restart Nuclear Power Plant in Pennsylvania**. U.S. Department of Energy · 17 November 2025
www.energy.gov/articles/energy-department-closes-loan-restart-nuclear-power-plant-pennsylvania
24. A **Hyperscaler capex has quadrupled since GPT-4's release**. Epoch AI · 26 February 2026
epoch.ai/data-insights/hyperscaler-capex-trend
25. A **United States Data Center Energy Usage Report: 2025 Update**. Lawrence Berkeley National Laboratory · 18 June 2026 · p. 10
www.energy.gov/documents/united-states-data-center-energy-usage-report-2025-update#page=10
26. A **United States Data Center Energy Usage Report: 2025 Update**. Lawrence Berkeley National Laboratory · 18 June 2026 · p. 11
www.energy.gov/documents/united-states-data-center-energy-usage-report-2025-update#page=11

27. A **Short-Term Energy Outlook, October 2026.** U.S. Energy Information Administration · 6 October 2026 · p. 46
www.eia.gov/outlooks/steo/archives/oct26.pdf#page=46
28. A **Short-Term Energy Outlook, October 2026.** U.S. Energy Information Administration · 6 October 2026 · p. 12
www.eia.gov/outlooks/steo/archives/oct26.pdf#page=12
29. A **Short-Term Energy Outlook, September 2026.** U.S. Energy Information Administration · 8 September 2026 · p. 4
www.eia.gov/outlooks/steo/archives/sep26.pdf#page=4
30. A **Short-Term Energy Outlook, September 2026.** U.S. Energy Information Administration · 8 September 2026 · p. 10
www.eia.gov/outlooks/steo/archives/sep26.pdf#page=10
31. B **Datacenters 2027: The Year of Acceleration, +50GW in a Single Year.** SemiAnalysis · 19 October 2026
newsletter.semianalysis.com/p/datacenters-2027-the-year-of-acceleration
32. A **Inside the Ironwood TPU codesigned AI stack.** Google Cloud · 6 November 2025
cloud.google.com/blog/products/compute/inside-the-ironwood-tpu-codesigned-ai-stack
33. A **Electric Reliability Council of Texas, ERCOT update to the Senate Committee on Business and Commerce, 29 July 2026.** Electric Reliability Council of Texas · 29 July 2026 · p. 6
www.ercot.com/files/docs/2026/07/29/ERCOT-Senate-July-29-Panel-1-Assessing-The-Grid.pdf#page=6
34. A **Electric Reliability Council of Texas, ERCOT update to the Senate Committee on Business and Commerce, 29 July 2026.** Electric Reliability Council of Texas · 29 July 2026 · p. 10
www.ercot.com/files/docs/2026/07/29/ERCOT-Senate-July-29-Panel-1-Assessing-The-Grid.pdf#page=10
35. A **<https://www.ercot.com/mktrules/issues/PGRR145>.** [ercot.com](https://www.ercot.com/mktrules/issues/PGRR145)
www.ercot.com/mktrules/issues/PGRR145
36. A **U.S. Department of Energy Large Power Transformer Resilience Report to Congress, July 2024.** U.S. Department of Energy · 10 July 2024 · p. 20
www.energy.gov/sites/default/files/2024-10/EXEC-2022-001242%20-%20Large%20Power%20Transformer%20Resilience%20Report%20signed%20by%20Secretary%20Granholm%20on%207-10-24.pdf#page=20
37. A **Micron Technology, quarterly report on Form 10-Q for the quarter ended 28 May 2026.** U.S. Securities and Exchange Commission (filing by Micron Technology) · 25 June 2026
www.sec.gov/Archives/edgar/data/723125/000072312526000015/mu-20260528.htm

01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

The Economics of AI Chips

Epoch AI estimated in December 2025 that Nvidia's B200 AI chip cost about \$6,400 to build, mostly for memory and packaging. Its processor silicon cost about \$900.

Specimen 15 · The Economics of AI Chips

Epoch AI's December 2025 estimate of what it cost to build one B200, drawn as a column with each layer as tall as its share of the bill. From the bottom: \$2,900 of memory in garnet, \$1,100 of packaging, \$1,000 of packaging yield loss drawn hollow, \$900 of logic dies, \$480 of power delivery, board and test. The total is about \$6,400, against a selling price of \$30,000 to \$40,000 per chip reported in March 2024.

In plain terms

Most of what it costs to build Nvidia's B200, an AI chip from its Blackwell line, goes to memory and packaging that a few firms supply. A bill of materials is the list of parts inside a product and what each one costs. Epoch AI estimated in December 2025 that the B200 cost about \$6,400 to build¹. The two logic dies, the pieces of silicon that do the calculating, cost about \$900 of that¹. The stacked memory beside them accounted for about half, and the packaging that wires the dies and memory together cost more than the dies¹. Three firms, SK hynix, Samsung and Micron, dominate the world market for that memory². One Taiwanese firm, TSMC, does that packaging¹.

In short

Epoch AI says Nvidia's margin on Blackwell may be lower than the gap between the B200's build cost and its selling price suggests¹. It cites reports from March 2024 that put the B200's selling price at \$30,000 to \$40,000 per chip¹. Epoch AI notes that most Blackwell revenue comes from servers and rack-scale systems, which may carry lower margins¹.

In 2026 Micron's gross margin, the share of sales left after production costs, passed Nvidia's. Micron's rose from 39.8 percent for the year to August 2025 to 80.7 percent for the year to September 2026³. It reached 86.8 percent in the last quarter of that year³. Nvidia's was 75.0 percent in

¹ NVIDIA's B200 costs around \$6,400 to produce. Epoch AI, 10 December 2025. epoch.ai

² Understanding the Biden Administration's Updated Export Controls. Center for Strategic and International Studies, 11 December 2024. csis.org

³ Micron Technology, Inc. Reports Record Fiscal Fourth-Quarter and Full-Year 2026... Micron Technology, 30 September 2026. investors.micron.com

the quarter to July 2026⁴. Epoch AI's estimate priced memory at \$14 to \$17 per gigabyte, before the 2026 rise in memory makers' sales and margins⁵.

A B200, one of Nvidia's Blackwell AI chips, sells for far more than it costs to build. In December 2025 Epoch AI estimated that building one cost about \$6,400¹. Epoch AI cites reports from March 2024 that put its selling price at \$30,000 to \$40,000 per chip¹. Most B200s are sold inside Nvidia's GB200 rack systems⁶. Epoch AI's chip sales model, with data through October 2025, puts what Nvidia earns per GPU for the computing hardware in those racks at \$33,000 to \$42,000⁶. That figure leaves out the networking gear in the racks⁶.

01

What an Nvidia B200 costs to build

Three numbers set the cost of a die, the finished rectangle of circuitry cut out of a wafer.

- **Wafer price.** TSMC does not publish it. TSMC makes Nvidia's Blackwell chips on a custom-built process called 4NP⁷. Epoch AI estimates \$17,000 for a 12-inch (300 mm) wafer on that process¹.
- **Dies per wafer.** A wafer is a circle and dies are rectangles, so the edge of the wafer goes to waste. The bigger the die, the fewer fit. Each of the two logic dies in a B200 is about 800 mm²¹. Nvidia calls them reticle-limited, meaning they are near the largest size a scanner can print in one shot⁷.
- **Yield.** Yield is the share of dies that work. Defects land at random, so a bigger die is more likely to catch one. Epoch AI models Blackwell die yield at 40 to 70 percent, centered on 60¹.

Together, those three numbers put the two dies inside a B200 at about \$900¹. Epoch AI's estimate for the whole B200 counts only variable costs, which rise with each chip made¹. It leaves out fixed costs such as research and development¹.

02

The B200's parts and rack costs

Memory is the largest line

The largest line on the bill is the 192 GB of high-bandwidth memory beside those dies, a generation called HBM3E¹. At \$14 to \$17 per gigabyte it comes to about \$2,900, which Epoch AI counts as half of the build cost¹. Epoch AI says HBM prices are negotiated deal by deal and can vary significantly with volume and contract length¹. The \$14 to \$17 range dates from December 2025, before the 2026 rise in memory makers' sales and margins described below⁵. SK hynix said DRAM and NAND flash prices rose

¹ NVIDIA's B200 costs around \$6,400 to produce. Epoch AI, 10 December 2025. epoch.ai

⁴ NVIDIA Announces Financial Results for Second Quarter Fiscal 2027. Nvidia, 26 August 2026. nvidianews.nvidia.com

⁵ SK hynix Announces 2Q26 Financial Results. SK hynix, 29 July 2026. news.skhynix.com

⁶ AI chip sales documentation. Epoch AI, 8 January 2026. epoch.ai

⁷ NVIDIA Blackwell Architecture. Nvidia, 18 December 2025. nvidia.com

significantly in the second quarter of 2026 from the quarter before, led by high-performance products for AI servers⁵.

Few firms make this memory, and one of them says demand has outrun its supply. SK hynix, Samsung and Micron dominate the world market for it². SK hynix said in July 2026 that demand for its products had exceeded its available supply in recent quarters⁸.

Packaging, substrate and test

CoWoS-L, the TSMC process that mounts dies and memory on one carrier and wires them together, adds about \$1,100, more than the logic dies it carries¹. Epoch AI models packaging yield at 65 to 95 percent¹. A package that fails testing loses its logic dies and memory stacks¹. Spreading that loss over the good units adds about \$1,000 to each B200¹. Power delivery hardware, the circuit board, and final assembly and testing add \$480¹. See Advanced packaging for how tight packaging capacity has been.

The B200 bill of materials

Line	Estimate	Range
HBM3E, 192 GB	\$2,900	\$2,800–3,100
CoWoS-L packaging	\$1,100	\$1,000–1,200
Packaging yield loss	\$1,000	\$430–1,700
Logic die, two on TSMC 4NP	\$900	\$720–1,200
Power delivery, board, assembly and test	\$480	\$370–600
Manufacturing cost	~\$6,400	\$5,700–7,300
Reported selling price per chip, March 2024	\$30,000–40,000	
Nvidia compute revenue per GPU in GB200 racks, data to October 2025	\$33,000–42,000	

Epoch AI models each line as a range, deriving the packaging line from TSMC's advanced packaging revenue and Nvidia's share of CoWoS capacity¹.

Epoch AI says Nvidia's actual margin on Blackwell may be lower than the gap between the B200's build cost and its reported chip price suggests¹. The estimate covers the accelerator module only and leaves out servers and rack-scale systems¹. Epoch AI notes that most Blackwell revenue comes from those systems, which may carry lower margins¹.

Epoch AI's line-by-line estimate covers the B200, which is no longer Nvidia's newest chip. In its results for the quarter to July 2026, Nvidia said its Vera Rubin platform was ramping into full production⁴. Each Rubin GPU carries up to 288 GB of HBM4, a newer generation of the stacked memory⁹.

¹ NVIDIA's B200 costs around \$6,400 to produce. Epoch AI, 10 December 2025. epoch.ai

² Understanding the Biden Administration's Updated Export Controls. Center for Strategic and International Studies, 11 December 2024. csis.org

⁴ NVIDIA Announces Financial Results for Second Quarter Fiscal 2027. Nvidia, 26 August 2026. nvidianews.nvidia.com

⁵ SK hynix Announces 2Q26 Financial Results. SK hynix, 29 July 2026. news.skhynix.com

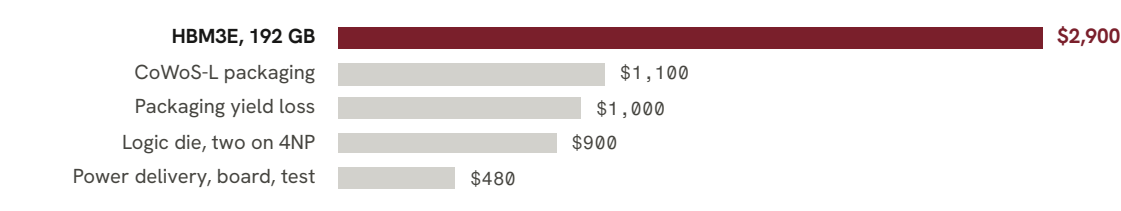
⁸ SK hynix, prospectus on Form 424B4 dated 10 July 2026. U.S. Securities and Exchange Commission, 10 July 2026. sec.gov

⁹ Inside NVIDIA Rubin GPU Architecture: Powering the Era of Agentic AI. Nvidia, 21 July 2026. developer.nvidia.com

Figure 15.1

Memory, \$2,900, is the largest line in Epoch AI's 2025 B200 estimate

Where the ~\$6,400 of B200 manufacturing cost goes, Epoch AI estimate, December 2025



Source: Epoch AI B200 cost model, from a \$17,000 4NP wafer, 40-70% die yield, \$14-17 per GB of memory, and a packaging line derived from TSMC's advanced packaging revenue [1]

From package to rack to cluster

Each new generation of Nvidia rack costs its owner more per hour than the last¹⁰. At rack scale, cost is measured per GPU-hour, one GPU running for one hour. For an operator that owns the machine, SemiAnalysis put a Vera Rubin NVL72 at \$3.57 per GPU-hour in July 2026, against \$1.84 for a GB200 and \$2.36 for a GB300¹⁰.

But SemiAnalysis found Rubin cheaper than GB200 and GB300 per token, a short chunk of text¹⁰. Rubin stayed cheaper at every level of interactivity SemiAnalysis compared, where interactivity is the number of tokens per second each user receives¹⁰. That finding rests on early results from the cloud provider CoreWeave running the DeepSeek R1 model, and SemiAnalysis said it had not verified them¹⁰.

One level up, a cluster needs power and a network as well as servers. SemiAnalysis estimated in June 2024 that a cluster of 100,000 of Nvidia's earlier H100 GPUs cost over \$4 billion in servers¹¹. The cluster needs more than 150 MW of data center capacity and uses 1.59 TWh a year, which costs \$123.9 million at \$0.078 per kWh¹¹. In the network design Nvidia recommended, 98,304 optical transceivers link the cluster's GPUs to the first layer of switches, called leaf switches¹¹.

03

Profit margins along the supply chain

Firm	Stage	Quarter ended	Gross margin
Micron	HBM and DRAM	September 2026	86.8% ³
Nvidia	Accelerator design	July 2026	75.0% ⁴
TSMC	Wafers and CoWoS	September 2026	66.4% ¹²
KLA (non-GAAP)	Inspection	June 2026	62.4% ¹³

1 NVIDIA's B200 costs around \$6,400 to produce. Epoch AI, 10 December 2025. epoch.ai

3 Micron Technology, Inc. Reports Record Fiscal Fourth-Quarter and Full-Year 2026... Micron Technology, 30 September 2026. investors.micron.com

4 NVIDIA Announces Financial Results for Second Quarter Fiscal 2027. Nvidia, 26 August 2026. nvidianews.nvidia.com

10 Vera Rubin NVL72 vs GB200 NVL72? Inference TCO & Architecture Analysis. SemiAnalysis, 23 July 2026. inferencex.semianalysis.com

11 100,000 H100 Clusters: Power, Network Topology, Ethernet vs InfiniBand... SemiAnalysis, 17 June 2024. newsletter.semianalysis.com

12 TSMC Reports Third Quarter EPS of NT\$29.43. U.S. Securities and Exchange Commission, 15 October 2026. sec.gov

13 Letter to Shareholders Q4 Fiscal 2026. KLA Corporation, 28 July 2026, p. 3. d1io3yog0oux5.cloudfront.net

ASML	Lithography	September 2026	57.5% ¹⁴
Lam Research	Etch	June 2026	51.7% ¹⁵
Applied Materials	Deposition	July 2026	50.3% ¹⁶
ASE Technology	Packaging and test segment	June 2026	27.3% ¹⁷
Amkor	OSAT	June 2026	16.8% ¹⁸

Gross margin is highest at the memory maker Micron and lowest in assembly and test. The firms in design, equipment and leading-edge wafers earn gross margins of 50.3 to 75.0 percent, and those in assembly and test 16.8 to 27.3 percent. Micron's gross margin rose from 39.8 percent for the year to August 2025 to 80.7 percent for the year to September 2026³. It reached 86.8 percent in the last quarter of that year³.

Each figure except KLA's comes from the firm's own earnings release. KLA's shareholder letter gives only a non-GAAP gross margin for the quarter, 62.4 percent¹³. KLA's non-GAAP figures adjust its results under US accounting rules, known as GAAP, to leave out items such as acquisition-related charges and restructuring, severance and other charges¹⁹. For ASE the figure is its packaging and test segment¹⁷. The company as a whole had a gross margin of 21.0 percent, because about a third of its revenue came from electronics manufacturing services, which earned 8.9 percent¹⁷.

Two other firms' results give no gross margin. SK hynix's operating margin was 76 percent in the quarter to June 2026, and its revenue was up 257 percent from a year earlier⁵. The substrate maker Ibiden's operating profit was 21.8 percent of net sales in the quarter to June 2026²⁰.

³ Micron Technology, Inc. Reports Record Fiscal Fourth-Quarter and Full-Year 2026... Micron Technology, 30 September 2026. investors.micron.com

⁵ SK hynix Announces 2Q26 Financial Results. SK hynix, 29 July 2026. news.skhynix.com

¹³ Letter to Shareholders Q4 Fiscal 2026. KLA Corporation, 28 July 2026, p. 3. d1io3yog0oux5.cloudfront.net

¹⁴ ASML reports €11.7 billion total net sales and €5.0 billion net income in Q3... U.S. Securities and Exchange Commission, 14 October 2026. sec.gov

¹⁵ Lam Research Corporation Reports Financial Results for the Quarter Ended June... Lam Research, 29 July 2026. newsroom.lamresearch.com

¹⁶ Applied Materials Announces Third Quarter 2026 Results. Applied Materials, 13 August 2026. ir.appliedmaterials.com

¹⁷ ASE Technology Holding Co., Ltd. Reports Its Unaudited Consolidated Financial... PR Newswire, 30 July 2026. prnewswire.com

¹⁸ Amkor Technology, current report on Form 8-K dated 27 July 2026. U.S. Securities and Exchange Commission, 27 July 2026. sec.gov

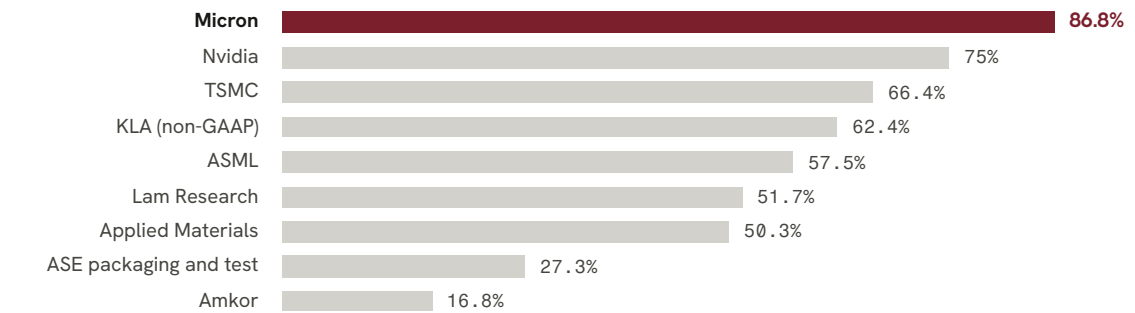
¹⁹ KLA Corporation Reports Fiscal 2026 Fourth Quarter and Full Year Results. KLA Corporation, 28 July 2026. ir.kla.com

²⁰ Outline of Consolidated Financial Results For the First Quarter Ended June 30... Ibiden, 4 August 2026. ibiden.com

Figure 15.2

Micron's gross margin, 86.8 percent, was highest of nine firms in 2026

Gross margin, quarters ended June to September 2026

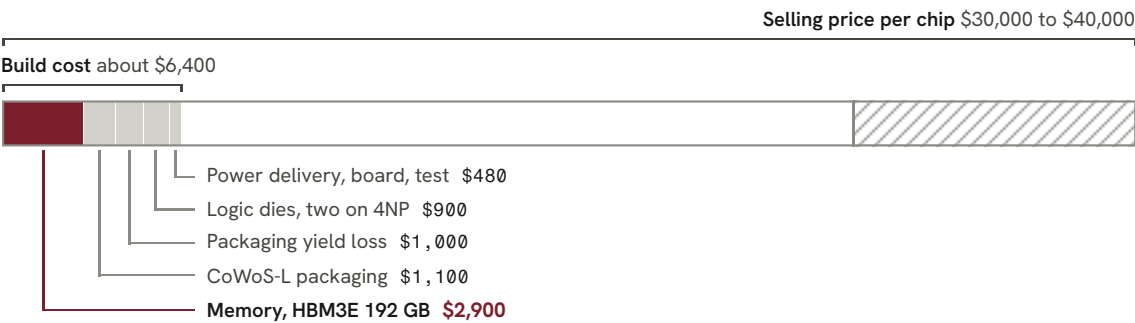


Source: Each firm's own quarterly earnings release, for quarters ending between June and September 2026 (TSMC's linked). ASE's bar is its packaging and test segment. KLA's bar is the non-GAAP figure from its shareholder letter [12]

Figure 15.3

Memory, \$2,900, is the largest cost of building a B200, which sells for \$30,000 to \$40,000

One B200, drawn to scale. Epoch AI's December 2025 estimate of what it cost to build, inside the selling price reported in March 2024



Source: Epoch AI B200 cost model, December 2025, and the March 2024 reports of its selling price that Epoch AI cites [1]

World chip sales are forecast to jump in 2026, with memory growing far faster than logic. The Semiconductor Industry Association, using monthly data compiled by World Semiconductor Trade Statistics, counted \$791.7 billion of global chip sales in 2025²¹. In its June 2026 forecast, World Semiconductor Trade Statistics put 2025 slightly higher, at \$795.6 billion²². It forecast \$1.51 trillion for 2026, with memory growing about 250 percent and logic 37 percent²².

In 2025 capital spending at five large tech firms far exceeded the world's sales of chipmaking equipment. The industry group SEMI counted \$135.1 billion of semiconductor equipment billings in 2025²³. Capital spending at Alphabet, Amazon,

1 NVIDIA's B200 costs around \$6,400 to produce. Epoch AI, 10 December 2025. epoch.ai

12 TSMC Reports Third Quarter EPS of NT\$29.43. U.S. Securities and Exchange Commission, 15 October 2026. sec.gov

21 Global Annual Semiconductor Sales Increase 25.6% to \$791.7 Billion in 2025. Semiconductor Industry Association, 6 February 2026. semiconductors.org

22 Global Semiconductor Market Surges Beyond USD 1.5 Trillion in 2026 Driven by... World Semiconductor Trade Statistics, 2 June 2026. wsts.org

23 SEMI Reports Global Semiconductor Equipment Billings Reached \$135 Billion in... SEMI, 7 April 2026. semi.org

Meta, Microsoft and Oracle came to \$448.2 billion in 2025, the sum of Epoch AI's quarterly figures²⁴. Epoch AI says that spending would reach \$770 billion in 2026 if the trend continues²⁴. These totals overlap, so they cannot be added together.

04

Which stages stay expensive and which get cheaper

Each stage falls into one of three classes, by whether its cost falls as volume grows. A structurally expensive stage stays costly because the work is hard, capacity is short or one firm sets the price. A stage compressible with scale gets cheaper as volume grows. An already commoditized stage has several competing suppliers. The classes are a judgment drawn from the sources in this chapter and the stage chapters.

Stage	Class	Why
EUV lithography	Structurally expensive	One supplier, ASML. See Lithography.
Masks and pellicles	Structurally expensive	Every design needs its own mask set, and every EUV layer a flawless mask. See Photomasks and pellicles.
Metrology and inspection	Structurally expensive	KLA held 56.8 percent of the market for these tools in 2025, by CSET's analysis of TechInsights data ²⁵ . See Metrology and inspection.
HBM	Structurally expensive	SK hynix says HBM needs more wafer input than ordinary DRAM ⁸ . See Memory and HBM.
Advanced packaging, CoWoS-L	Structurally expensive	Modeled packaging yield is 65 to 95 percent, and a failed package loses its dies and memory.
ABF substrates	Structurally expensive	Investment can add substrate lines, but Ajinomoto said in June 2026 that the insulating film it makes for these substrates has held over 95 percent of its market since launch ²⁶ . See Substrates and PCBs.
Power and cooling plant	Structurally expensive	In the United States, grid connections face long queues, so at least three of OpenAI's seven Stargate sites will use on-site natural gas plants ²⁷ . GE Vernova's backlog of gas power equipment, together with agreements reserving future production slots, grew from 100 GW to 116 GW in the second quarter of 2026 ²⁸ . See Data centers and power.
Optical transceivers	Structurally expensive	In May 2026 Nikkei reported that building AI data centers had caused shortages and price rises for lasers, optical fibers and other optical parts ²⁹ . Nvidia agreed in March 2026 to invest \$2 billion in the laser maker Lumentum, with rights to future capacity ³⁰ . It agreed a similar \$2 billion deal with Coherent ³¹ . See Systems and networking.
Leading-edge logic wafers	Compressible with scale	A very large die yields well only once a process matures. See Foundries and fabs.
Design and EDA	Compressible with scale	A design is paid for once, and its cost is spread across every chip sold. See Chip design, EDA and IP.
Deposition and etch tools	Compressible with scale	Most deposition and etch steps have three or four established tool makers. See Deposition and etch.

⁸ SK hynix, prospectus on Form 424B4 dated 10 July 2026. U.S. Securities and Exchange Commission, 10 July 2026. [sec.gov](#)

²⁴ Hyperscaler capex has quadrupled since GPT-4's release. Epoch AI, 26 February 2026. [epoch.ai](#)

²⁵ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. [chipeexplorer.eto.tech](#)

²⁶ Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026. Ajinomoto, 30 June 2026, p. 3. [ajinomoto.co.jp](#)

²⁷ OpenAI Stargate: where the US sites stand. Epoch AI, 17 April 2026. [epoch.ai](#)

²⁸ GE Vernova, current report on Form 8-K dated 22 July 2026. U.S. Securities and Exchange Commission, 22 July 2026. [sec.gov](#)

²⁹ AI demand strains supplies of lasers, fiber and other optical tech. Nikkei Asia, 27 May 2026. [asia.nikkei.com](#)

³⁰ NVIDIA Announces Strategic Partnership With Lumentum to Develop... Nvidia, 2 March 2026. [nvidianews.nvidia.com](#)

³¹ NVIDIA and Coherent Announce Strategic Partnership to Develop Optics Technology... Nvidia, 2 March 2026. [nvidianews.nvidia.com](#)

Test and assembly (OSAT)	Already commoditized	Gross margins of 16.8 to 27.3 percent at Amkor and ASE's packaging and test segment in the quarter to June 2026.
Wafers and bulk gases	Already commoditized	Several firms make approved 300 mm wafers. By Siltronic's estimate, the five largest wafer makers served around 75 percent of the market in the first three quarters of 2025 ³² . See Silicon and wafers.
Rack integration (ODM)	Already commoditized	In October 2025 Nvidia said more than 50 makers of systems and components were gearing up for the Vera Rubin NVL72 ³³ . See Systems and networking.

Four questions to answer from memory

1. Where does most of the cost of building an Nvidia B200 go? *see How it works*
2. What is the most expensive part of a B200? *see Memory is the largest line*
3. How does a B200's price compare with its cost to build?
4. Which three numbers set the cost of a die? *see How it works*

Three things to remember

- Epoch AI estimated in December 2025 that a B200 cost about \$6,400 to build, against a selling price of \$30,000 to \$40,000 per chip reported in March 2024.
- The stacked memory is the most expensive part, about half of the cost.
- Packaging costs more than the logic chips, and each package that fails wastes the chips and memory inside it.

Sources (33)

1. A **NVIDIA's B200 costs around \$6,400 to produce.** Epoch AI · 10 December 2025
epoch.ai/data-insights/b200-cost-breakdown
2. A **Understanding the Biden Administration's Updated Export Controls.** Center for Strategic and International Studies · 11 December 2024
www.csis.org/analysis/understanding-biden-administrations-updated-export-controls
3. A **Micron Technology, Inc. Reports Record Fiscal Fourth-Quarter and Full-Year 2026 Results.** Micron Technology · 30 September 2026
investors.micron.com/news/press-release/2026/Micron-Technology-Inc--Reports-Record-Fiscal-Fourth-Quarter-and-Full-Year-2026-Results/default.aspx
4. A **NVIDIA Announces Financial Results for Second Quarter Fiscal 2027.** Nvidia · 26 August 2026
nvidianews.nvidia.com/news/nvidia-announces-financial-results-for-second-quarter-fiscal-2027
5. A **SK hynix Announces 2Q26 Financial Results.** SK hynix · 29 July 2026
news.skhynix.com/en/q2-2026-business-results/
6. A **AI chip sales documentation.** Epoch AI · 8 January 2026
epoch.ai/data/ai-chip-sales-documentation/methodology#nvidia
7. A **NVIDIA Blackwell Architecture.** Nvidia · 18 December 2025
www.nvidia.com/en-us/data-center/technologies/blackwell-architecture/
8. A **SK hynix, prospectus on Form 424B4 dated 10 July 2026.** U.S. Securities and Exchange Commission (filing by SK hynix) · 10 July 2026
www.sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm
9. A **Inside NVIDIA Rubin GPU Architecture: Powering the Era of Agentic AI.** Nvidia · 21 July 2026
developer.nvidia.com/blog/inside-nvidia-rubin-gpu-architecture-powering-the-era-of-agentic-ai/
10. B **Vera Rubin NVL72 vs GB200 NVL72? Inference TCO & Architecture Analysis.** SemiAnalysis · 23 July 2026
inferencex.semianalysis.com/blog/vera-rubin-nvl72-vs-gb200-nvl72-inference
11. B **100,000 H100 Clusters: Power, Network Topology, Ethernet vs InfiniBand, Reliability, Failures, Checkpointing.** SemiAnalysis · 17 June 2024
newsletter.semianalysis.com/p/100000-h100-clusters-power-network
12. A **TSMC Reports Third Quarter EPS of NT\$29.43.** U.S. Securities and Exchange Commission (filing by TSMC) · 15 October 2026
www.sec.gov/Archives/edgar/data/1046179/000104617926000726/a3q26e_withguidancexfinal.htm

³² Investor Presentation: Foundation of Digital Life. Siltronic, April 2026, p. 6. siltronic.com

³³ NVIDIA, Partners Drive Next-Gen Efficient Gigawatt AI Factories in Buildup for... Nvidia, 13 October 2025. blogs.nvidia.com

13. A **Letter to Shareholders Q4 Fiscal 2026.** KLA Corporation · 28 July 2026 · p. 3
d1io3yog0oux5.cloudfront.net/_b9ee755a5f60dd0fb3f9e27967aed6af/klatencor/db/1117/10668/letter_to_shareholders/KLA+Earnings+Shareholder+Letter+-+Q4+FY26.pdf#page=3
14. A **ASML reports €11.7 billion total net sales and €5.0 billion net income in Q3 2026.** U.S. Securities and Exchange Commission (filing by ASML Holding) · 14 October 2026
www.sec.gov/Archives/edgar/data/937966/000162828026065813/pressreleasefinancialresul.htm
15. A **Lam Research Corporation Reports Financial Results for the Quarter Ended June 28, 2026.** Lam Research · 29 July 2026
newsroom.lamresearch.com/2026-07-29-Lam-Research-Corporation-Reports-Financial-Results-for-the-Quarter-Ended-June-28,-2026
16. A **Applied Materials Announces Third Quarter 2026 Results.** Applied Materials · 13 August 2026
ir.appliedmaterials.com/news-releases/news-release-details/applied-materials-announces-third-quarter-2026-results
17. A **ASE Technology Holding Co., Ltd. Reports Its Unaudited Consolidated Financial Results for the Second Quarter of 2026.** PR Newswire · 30 July 2026
www.prnewswire.com/news-releases/ase-technology-holding-co-ltd-reports-its-unaudited-consolidated-financial-results-for-the-second-quarter-of-2026-302838714.html
18. A **Amkor Technology, current report on Form 8-K dated 27 July 2026.** U.S. Securities and Exchange Commission (filing by Amkor Technology) · 27 July 2026
www.sec.gov/Archives/edgar/data/0001047127/000104712726000043/amkr6302026erex-991.htm
19. A **KLA Corporation Reports Fiscal 2026 Fourth Quarter and Full Year Results.** KLA Corporation · 28 July 2026
ir.kla.com/news-events/press-releases/detail/518/kla-corporation-reports-fiscal-2026-fourth-quarter-and-full
20. A **Outline of Consolidated Financial Results For the First Quarter Ended June 30, 2026.** Ibidem · 4 August 2026
www.ibiden.com/ir/items/outline2026Q1.pdf
21. A **Global Annual Semiconductor Sales Increase 25.6% to \$791.7 Billion in 2025.** Semiconductor Industry Association · 6 February 2026
www.semiconductors.org/global-annual-semiconductor-sales-increase-25-6-to-791-7-billion-in-2025/
22. A **Global Semiconductor Market Surges Beyond USD 1.5 Trillion in 2026 Driven by Extraordinary Memory Expansion.** World Semiconductor Trade Statistics · 2 June 2026
www.wsts.org/esraCMS/extension/media/f/WST/7618/WSTS_FC-Release-2026-May.pdf
23. A **SEMI Reports Global Semiconductor Equipment Billings Reached \$135 Billion in 2025, Up 15% Year-on-Year.** SEMI · 7 April 2026
www.semi.org/en/SEMI-Reports-Global-Semiconductor-Equipment-Billings-Reached-135-Billion-in-2025
24. A **Hyperscaler capex has quadrupled since GPT-4's release.** Epoch AI · 26 February 2026
epoch.ai/data-insights/hyperscaler-capex-trend
25. A **Supply Chain Explorer: Advanced Chips.** Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N118&selectedNode=N60
26. A **Ajinomoto, Growth Strategy for the Electronic Materials Business, 30 June 2026.** Ajinomoto · 30 June 2026 · p. 3
www.ajinomoto.co.jp/company/en/ir/event/business_briefing/main/011117/teaserItems1/01/linkList/03/link/20260630_presentation_E.pdf#page=3
27. A **OpenAI Stargate: where the US sites stand.** Epoch AI · 17 April 2026
epoch.ai/publications/openai-stargate-where-the-us-sites-stand
28. A **GE Vernova, current report on Form 8-K dated 22 July 2026.** U.S. Securities and Exchange Commission (filing by GE Vernova) · 22 July 2026
www.sec.gov/Archives/edgar/data/1996810/000199681026000147/gevpressrelease2q26.htm
29. B **AI demand strains supplies of lasers, fiber and other optical tech.** Nikkei Asia · 27 May 2026
asia.nikkei.com/business/technology/tech-asia/ai-demand-strains-supplies-of-lasers-fiber-and-other-optical-tech
30. A **NVIDIA Announces Strategic Partnership With Lumentum to Develop State-of-the-Art Optics Technology.** Nvidia · 2 March 2026
nvidianews.nvidia.com/news/nvidia-announces-strategic-partnership-with-lumentum-to-develop-state-of-the-art-optics-technology
31. A **NVIDIA and Coherent Announce Strategic Partnership to Develop Optics Technology to Scale Next-Generation Data Center Architecture.** Nvidia · 2 March 2026
nvidianews.nvidia.com/news/nvidia-and-coherent-announce-strategic-partnership-to-develop-optics-technology-to-scale-next-generation-data-center-architecture
32. A **Investor Presentation: Foundation of Digital Life.** Siltronic · April 2026 · p. 6
www.siltronic.com/fileadmin/investorrelations/2026/Q1/20260429_Siltronic_InvestorPresentation__.pdf#page=6
33. A **NVIDIA, Partners Drive Next-Gen Efficient Gigawatt AI Factories in Buildup for Vera Rubin.** Nvidia · 13 October 2025
blogs.nvidia.com/blog/gigawatt-ai-factories-ocp-vera-rubin

01	Chip Design, EDA and IP	
02	Silicon and Wafers	
03	Chemicals, Gases and Photoresist	
04	Lithography	
05	Photomasks and Pellicles	
06	Deposition and Etch	
07	Metrology and Inspection	
08	Foundries and Fabs	
09	Memory and HBM	
10	Advanced Packaging	
11	Substrates and PCBs	
12	Test and Assembly	
13	Systems and Networking	
14	Data Centers and Power	
15	The Economics of AI Chips	
16	Who Controls the Chain	

Who Controls the Chain

Since 2018 the United States has used export controls to limit China's access to advanced chips and chipmaking tools, and China has been learning to make both.

Specimen 16 · Who Controls the Chain

The world, with nineteen chokepoint towns pinned in garnet. Five towns building alternatives to those chokepoints are pinned in ink: Beijing, Wuhan, Shenzhen, Hefei and Dresden. The taller the garnet pin, the tighter the chokepoint at that town's stage of the chain. The pins are not to scale. If the globe were the size of the Earth, the tallest pin would stand about 1,000 km high.

In plain terms

Export controls work only when a country's own firms sell something the buyer cannot get elsewhere, so few governments can use them to much effect. An export control is a rule that requires the government's permission for a sale. The government names an item and a country or a buyer. From then on its own companies must hold a license before they ship that item to that country or buyer. The American government extends some of these rules to goods made abroad with American technology. The machines, software and chemicals used to make an advanced chip come from a short list of firms in the United States, the Netherlands and Japan, so those three governments can control who gets them.

In short

Japan and the Netherlands have aligned their own export controls with the American rules on chipmaking equipment¹. China has answered by building its own tools and by restricting sales of US chips in China. Chinese toolmakers supplied 35 percent of China's own chipmaking equipment market in 2025, up from 10 to 15 percent before 2022². Nvidia says the Chinese government restricted the sales of its H200 chip that the United States licensed in February 2026³.

The most advanced chips come mainly from Taiwan. It held 69 percent of the world's capacity for logic chips below 10 nanometers in 2022, by the

¹ Where the Chips Fall: U.S. Export Controls Under the Biden Administration from... Center for Strategic and International Studies, 12 December 2024. [csis.org](https://www.csis.org/analysis/where-the-chips-fall-us-export-controls-under-the-biden-administration)

² China's Localization Drive in Semiconductors Gains Impetus from Allied Chip... Center for Strategic and International Studies, 24 March 2026. [csis.org](https://www.csis.org/analysis/china-localization-drive-semiconductors-gains-impetus-allied-chip)

³ Nvidia, quarterly report on Form 10-Q for the quarter ended 26 July 2026. U.S. Securities and Exchange Commission, 26 August 2026. [sec.gov](https://www.sec.gov)

count of the Semiconductor Industry Association and Boston Consulting Group⁴.

01

How chip export controls work

China cannot yet make the most advanced lithography machines, which print a chip's finest circuits⁵. China's leading lithography maker, SMEE, produces only older, less precise machines, among them some deep-ultraviolet types⁵. China has also yet to show it can make high-bandwidth memory, the stacked memory beside an AI chip, in volume.

In September 2022 US National Security Advisor Jake Sullivan said the United States had previously aimed to stay "only a couple of generations ahead" in some key technologies⁶. He said it must now keep "as large of a lead as possible" in foundational technologies such as advanced logic and memory chips⁶. The export rules of October 2022 were the first to apply his doctrine of a small yard with a high fence, meaning strict controls on a narrow set of technologies¹. The Center for Strategic and International Studies (CSIS), a research institute in Washington, judged that those rules went beyond the old aim of staying two technology nodes ahead of China and tried to push China's capability back below the level it had already reached⁷.

US license rules can target a single buyer or a whole country, and in 2022 the rules on advanced AI chips and the tools for advanced fabs began to cover all of China. In October 2018, for example, the Bureau of Industry and Security (BIS), the US Commerce Department's export control office, put the Chinese chip company Fujian Jinhua Integrated Circuit on its Entity List⁸. From then on any item under US export rules needed a license to reach the company⁸. The 2022 rules went further and required a license for any advanced AI chip, and any tool for an advanced fab, bound for China⁹. BIS reviewed most applications under a presumption of denial, meaning it would normally refuse them⁹. It reviewed applications for equipment bound for the China fabs of firms headquartered in the United States or allied and partner countries case by case⁹.

02

Which countries lead each segment

Segment	Leader	Share	Basis
EUV lithography	Netherlands	100.0%	revenue, 2025

1 Where the Chips Fall: U.S. Export Controls Under the Biden Administration from... Center for Strategic and International Studies, 12 December 2024. [csis.org](#)

4 Emerging Resilience in the Semiconductor Supply Chain. Boston Consulting Group and Semiconductor Industry..., May 2024, p. 14. [semiconductors.org](#)

5 Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements. Center for Strategic and International Studies, 24 September 2025. [csis.org](#)

6 Remarks by National Security Advisor Jake Sullivan at the Special Competitive... The White House, 16 September 2022. [bidenwhitehouse.archives.gov](#)

7 Choking off China's Access to the Future of AI. Center for Strategic and International Studies, 11 October 2022. [csis.org](#)

8 Addition of an Entity to the Entity List. Federal Register, 30 October 2018. [federalregister.gov](#)

9 Implementation of Additional Export Controls: Certain Advanced Computing and... Federal Register, 13 October 2022. [federalregister.gov](#)

Immersion DUV lithography	Netherlands	99.3%	revenue, 2025
Metrology and inspection	United States	71.7%	revenue, 2025
Deposition	United States	60.3%	revenue, 2025
Etch and clean	United States	52.6%	revenue, 2025
Photoresist	Japan	78%	revenue, 2023
Silicon wafers	Japan	53%	revenue, 2023
Leading-edge logic, below 10 nm	Taiwan	69%	capacity, 2022
Foundry, all nodes	Taiwan	81.9%	market share, 2025
HBM	South Korea	82.5%	revenue, 2025: SK hynix 63.2, Samsung 19.3, Micron 17.4
Logic chip design	United States	65%	sales, 2022
Mature logic, 28 nm and above	China	33%	capacity, 2022

No country leads every segment. The United States leads four of the table's segments. The Netherlands, Japan and Taiwan lead two each, and South Korea and China one each.

- **Equipment.** TechInsights 2025 revenue by parent-company headquarters, from CSET's ETO Supply Chain Explorer¹⁰.
- **Materials.** Fuji Keizai's survey by parent-company headquarters, as Japan's Ministry of Economy, Trade and Industry published it in December 2025¹¹.
- **Memory.** Figures from the market research firm IDC, as SK hynix's US listing prospectus relays them¹².
- **Logic capacity.** The Semiconductor Industry Association and Boston Consulting Group's 2022 measurement of logic capacity, below 10 nm for Taiwan and at 28 nm and above for China⁴.

Advanced packaging is missing from the table because no public source splits its capacity by country. The Taiwanese chipmaker TSMC does not publish one either.

03

How US chip export controls have changed

US chip controls grew tighter from 2020 to 2024. In August 2020 BIS widened its Foreign Direct Product Rule to require a license for any foreign-made item produced with US technology and bound for Huawei¹³. In 2022 BIS blocked China's access to the most advanced AI chips and to the tools to make them¹. It tightened those rules in 2023 and 2024¹. But in August 2025 the US government began licensing some sales of Nvidia's H20 chip to China¹⁴. In February 2026 it began licensing small amounts of the H200¹⁴.

¹ Where the Chips Fall: U.S. Export Controls Under the Biden Administration from... Center for Strategic and International Studies, 12 December 2024. csis.org

⁴ Emerging Resilience in the Semiconductor Supply Chain. Boston Consulting Group and Semiconductor Industry..., May 2024, p. 14. semiconductors.org

¹⁰ Documentation: Semiconductor Supply Chain Dataset. Emerging Technology Observatory (ETO), accessed 9 September 2026. eto.tech

¹¹ METI, Semiconductor and digital industry strategy: future direction... Ministry of Economy, Trade and Industry (Japan), 23 December 2025, p. 8. meti.go.jp

¹² SK hynix, prospectus on Form 424B4 dated 10 July 2026. U.S. Securities and Exchange Commission, 10 July 2026. sec.gov

¹³ Addition of Huawei Non-U.S. Affiliates to the Entity List, the Removal of... Federal Register, 20 August 2020. federalregister.gov

¹⁴ Nvidia, annual report on Form 10-K for the fiscal year ended 25 January 2026. U.S. Securities and Exchange Commission, 25 February 2026. sec.gov

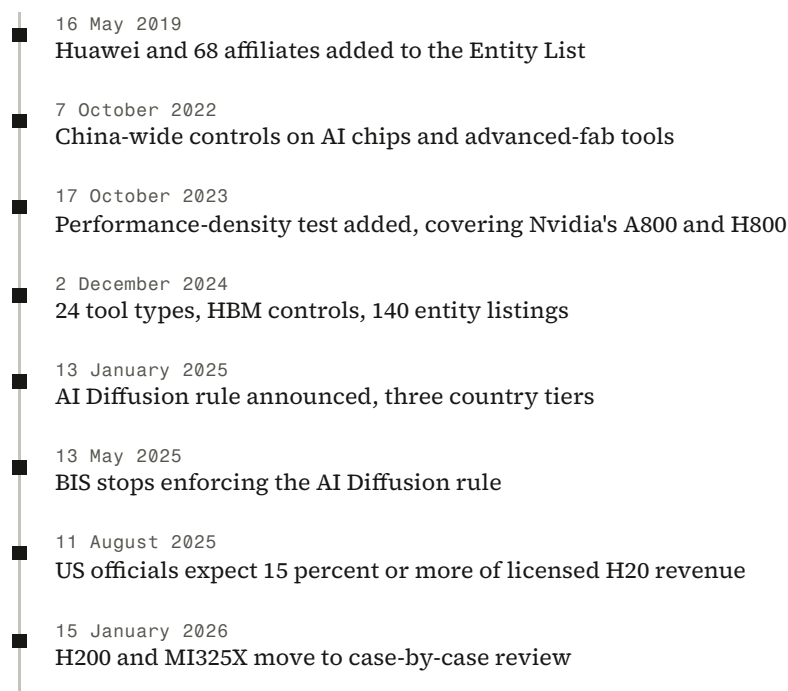
The United States has also approved large AI chip sales in the Gulf. In November 2025 Commerce authorized G42 of the United Arab Emirates and HUMAIN of Saudi Arabia to buy the equivalent of up to 35,000 Nvidia GB300 chips each under security and reporting conditions¹⁵. On 10 July 2026 BIS moved the United Arab Emirates into Country Group A:5, the export-control group that holds close US allies¹⁶. It named the Emirati government, G42 and eight US-headquartered AI companies as recipients that need no license for controlled AI chips and systems¹⁶.

The Export Controls page has the full timeline, with the legal citation for each rule.

Figure 16.1

US chip export controls tightened through January 2025, then partly eased

Eight US actions that shaped chip export controls



Source: Federal Register rules, BIS press releases and Nvidia filings, cited for each entry on the Export Controls timeline

04

Renting compute abroad and chip smuggling

Firms can use controlled chips without any chip crossing a border, because renting out time on a chip does not count as exporting it¹⁷. A Singapore data center selling time on an H200 already installed there, for example, moves nothing across a border¹⁷. The AI Diffusion rule of January 2025 required a license for advanced AI chips bound anywhere in the world¹⁸. For the data centers it approved, it said that API access to a model, and rented capacity for inference, "are not prohibited"¹⁸. On 13 May 2025 the

15 Statement on UAE and Saudi Chip Exports. U.S. Department of Commerce, November 2025. [commerce.gov](https://www.commerce.gov)

16 Enhanced Favorable Treatment for the United Arab Emirates Under the Export... Federal Register, 14 July 2026. [federalregister.gov](https://www.federalregister.gov)

17 15 CFR 734.13 -- Export. Electronic Code of Federal Regulations, 3 June 2016. [ecfr.gov](https://www.ecfr.gov)

18 Framework for Artificial Intelligence Diffusion. Federal Register, 15 January 2025. [federalregister.gov](https://www.federalregister.gov)

Commerce Department said it would rescind the rule and told BIS officials not to enforce it¹⁹.

The American rules reach that trade through the firms holding the chips. A license under the 15 January 2026 rule for H200-class chips bound for China or Macau requires the applicant to obtain a description of the recipient's know-your-customer procedures²⁰. These are the recipient's checks on who its customers are. The applicant must also obtain the recipient's list of customers renting computing power in China and seven other places, among them Russia and Iran²⁰. The recipient must also promise that no algorithm trained on the chips is served to blacklisted or military end users²⁰.

Smugglers route chips past the controls through Southeast Asia. Since 14 July 2025 Malaysia has required a permit to export, transship or transit any high-performance US-origin AI chip²¹. On 25 March 2026 the Justice Department announced charges against three people accused of using Thai companies' names to order servers with export-controlled chips for China²². The orders included one for \$170 million that was never completed²².

In July 2025 the US House of Representatives' select committee on China cited estimates that a median of 140,000 chips were smuggled to China in 2024²³. A bill in Congress, the Chip Security Act, would require location verification on controlled chips within 180 days of enactment²⁴. The House Foreign Affairs Committee approved the House version 42-0 on 26 March 2026²⁵.

05

The Netherlands, Japan, Korea and Europe

US tool controls alone would only shift the sales to Dutch and Japanese suppliers, so US controls depend on those two governments. Both have aligned their own controls on chipmaking equipment with the American rules¹.

- **The Netherlands.** The Dutch government began requiring export licenses for advanced deep-ultraviolet tools on 1 September 2023 and widened the controls in September 2024²⁶. On 1 April 2025 it extended them to measurement and inspection tools²⁷.

¹ Where the Chips Fall: U.S. Export Controls Under the Biden Administration from... Center for Strategic and International Studies, 12 December 2024. [csis.org](https://www.csis.org)

¹⁹ Department of Commerce Announces Rescission of Biden-Era Artificial... U.S. Bureau of Industry and Security, 13 May 2025. [bis.gov](https://www.bis.gov)

²⁰ Revision to License Review Policy for Advanced Computing Commodities. U.S. Government Publishing Office, 15 January 2026. [govinfo.gov](https://www.govinfo.gov)

²¹ Export, transshipment and transit of high-performance AI chips of US origin now... Ministry of Investment, Trade and Industry, 14 July 2025. miti.gov.my

²² Chinese National and Two U.S. Citizens Charged with Conspiring to Smuggle... U.S. Department of Justice, 25 March 2026. [justice.gov](https://www.justice.gov)

²³ Protecting U.S. Tech: China Committee and Bipartisan, Bicameral Leaders Unite... U.S. House Select Committee on the Chinese Communist Party, 7 July 2025. chinaselectcommittee.house.gov

²⁴ S.1705 – Chip Security Act, 119th Congress (2025-2026), bill text. U.S. Congress, 8 May 2025. [congress.gov](https://www.congress.gov)

²⁵ UNANIMOUS: Bipartisan Huizenga Legislation to Curb AI Chip Smuggling Passes... U.S. House of Representatives, 26 March 2026. huizenga.house.gov

²⁶ The Netherlands expands export control measure for advanced semiconductor... Government of the Netherlands, 6 September 2024. [government.nl](https://www.government.nl)

²⁷ Klever: export controls on advanced semiconductor manufacturing equipment to be... Government of the Netherlands, 15 January 2025. [government.nl](https://www.government.nl)

- **Japan.** Japan's controls on advanced manufacturing equipment took effect on 23 July 2023, apply to all destinations and name no country²⁸.
- **US rules for South Korean fabs in China.** BIS revoked the Validated End-User status that let Samsung's and SK hynix's China subsidiaries and Intel Semiconductor (Dalian) receive US equipment without individual licenses, effective 31 December 2025²⁹. BIS said it would license those fabs to keep running, but not to expand capacity or upgrade technology³⁰. SK hynix, which bought the Dalian fab from Intel, received an annual BIS license in December 2025 to ship approved US equipment to its China fabs during 2026³¹.

A BIS rule effective 29 September 2025 extended Entity List restrictions to any company at least 50 percent owned by one or more listed firms³². The rule reached Nexperia, a Nijmegen chipmaker that supplies Europe's car industry, and the Dutch government said it worked to secure an exemption for the company³³. On 30 September the Dutch economy minister invoked the Goods Availability Act against Nexperia³⁴. He cited governance failures that risked moving technology out of Europe³⁴. The order aimed to keep Nexperia's production capabilities available to Europe in an emergency³³.

On 4 October the Chinese authorities imposed an export control on Nexperia's operations in China, so deliveries from those operations to customers needed an export license³⁵. The Dutch government said uncertainty over licensing and long processing times caused chip shortages among Nexperia's customers and stopped production at some companies³⁵.

Both the US rule and the Dutch order were suspended in November. On 10 November BIS suspended its rule until 9 November 2026³⁶. The minister suspended his order on 19 November³³. He cited constructive meetings with the Chinese authorities and the measures they had taken to ensure the supply of chips to Europe and the rest of the world³³. Europe holds a chokepoint in leading-edge lithography, but none in the mature-node chips its car industry uses.

A bill in the US Congress would push allies to match US limits on chipmaking tools sold to China. The MATCH Act, a bill introduced on 8 April 2026, would ban sales of immersion deep-ultraviolet scanners to China³⁷. It would also restrict exports to, and servicing of, every chipmaking plant run by five Chinese companies, CXMT, Hua Hong, Huawei, SMIC and YMTC³⁷. It would give allies 150 days to match those limits before the United States extends its own controls to foreign-made items that use US software, technology or components³⁷.

28 CSIS Translation: Updated Japanese Export Controls on High-Performance... Center for Strategic and International Studies, 18 July 2023. [csis.org](https://www.csis.org)

29 Revocation of Validated End-User Authorizations in the People's Republic of... Federal Register, 2 September 2025. [federalregister.gov](https://www.federalregister.gov)

30 Department of Commerce Closes Export Controls Loophole for Foreign-Owned... U.S. Bureau of Industry and Security, 29 August 2025. [bis.gov](https://www.bis.gov)

31 SK hynix, prospectus on Form 424B4 dated 10 July 2026. U.S. Securities and Exchange Commission, 10 July 2026. [sec.gov](https://www.sec.gov)

32 Expansion of End-User Controls To Cover Affiliates of Certain Listed Entities. Federal Register, 30 September 2025. [federalregister.gov](https://www.federalregister.gov)

33 Update on invoking Goods Availability Act - 19 november 2025. Government of the Netherlands, 19 November 2025. [government.nl](https://www.government.nl)

34 Minister of Economic Affairs invokes Goods Availability Act. Government of the Netherlands, 12 October 2025. [government.nl](https://www.government.nl)

35 Developments concerning Nexperia, letter to the House of Representatives. Government of the Netherlands, 19 November 2025. [government.nl](https://www.government.nl)

36 One Year Suspension of Expansion of End-User Controls for Affiliates of Certain... Federal Register, 12 November 2025. [federalregister.gov](https://www.federalregister.gov)

37 Risch, Ricketts, Kim Introduce MATCH Act; Level the Global Playing Field for... U.S. Senate Committee on Foreign Relations, 8 April 2026. [foreign.senate.gov](https://www.foreign.senate.gov)

06

China's response to the chip controls

China has answered by replacing foreign chips at home, restricting some American suppliers, limiting its exports of minerals and building its own chipmaking tools. In 2024 China's Ministry of Industry and Information Technology reportedly told Chinese telecom operators to strip foreign chips out of their networks by 2027².

China has also taken measures against American suppliers. On 21 May 2023 the Cyberspace Administration of China (CAC) said that products sold in China by Micron, the American memory maker, had failed a cybersecurity review³⁸. It said operators of critical information infrastructure in China should stop buying them³⁸. In September 2025 the CAC reportedly told firms including ByteDance and Alibaba to cancel Nvidia orders³⁹. Nvidia says the Chinese government restricted the H200 sales that the United States licensed in February 2026³. It says China had earlier restricted licensed H20 sales too³.

China's Ministry of Commerce (MOFCOM) has also restricted exports of minerals.

- **3 December 2024.** MOFCOM banned exports of gallium, germanium, antimony and superhard materials to the United States, one day after the American chip rules⁴⁰.
- **4 April 2025.** It required export licenses for seven medium and heavy rare earths⁴¹.
- **9 October 2025.** It announced that from 1 December 2025 foreign firms would need its license to export listed goods made abroad with Chinese rare earths worth 0.1 percent or more of their value⁴². MOFCOM suspended that rule on 7 November 2025 until 10 November 2026⁴³.
- **9 November 2025.** MOFCOM suspended its ban on exports of gallium, germanium, antimony and superhard materials to the United States until 27 November 2026⁴⁴. It acted after Donald Trump and Xi Jinping met at the Asia-Pacific summit in October 2025⁴⁵.

China's suspension of its October 2025 controls did not cover the April 2025 licensing rules for seven rare earths⁴³.

² China's Localization Drive in Semiconductors Gains Impetus from Allied Chip... Center for Strategic and International Studies, 24 March 2026. csis.org

³ Nvidia, quarterly report on Form 10-Q for the quarter ended 26 July 2026. U.S. Securities and Exchange Commission, 26 August 2026. sec.gov

³⁸ Cyberspace Administration of China, notice on the cybersecurity review of... Cyberspace Administration of China, 21 May 2023. cac.gov.cn

³⁹ Beijing blocks Nvidia sales in vote of confidence for Chinese chipmakers, the... Center for Security and Emerging Technology, 18 September 2025. cset.georgetown.edu

⁴⁰ Ministry of Commerce Notice 2024 No. 46: Notice Concerning Strengthening... Center for Security and Emerging Technology, 3 December 2024. cset.georgetown.edu

⁴¹ Announcement No.18 of 2025 of The Ministry of Commerce and The General... Ministry of Commerce of the People's Republic of China, 4 April 2025. english.mofcom.gov.cn

⁴² Ministry of Commerce Notice 2025 No. 61: Announcement of the Decision to... Center for Security and Emerging Technology, 9 October 2025. cset.georgetown.edu

⁴³ MOFCOM and GAC Announcement 2025 No. 70, suspending the October 2025... Ministry of Commerce of the People's Republic of China, 7 November 2025. mofcom.gov.cn

⁴⁴ 商务部公告2025年第72号 公布调整实施商务部公告2024年第46号的决定. Ministry of Commerce of the People's Republic of China, 9 November 2025. mofcom.gov.cn

⁴⁵ The U.S.-China Trade Truce Has Not Solved the Gallium Problem. Center for Strategic and International Studies, 11 May 2026. csis.org

Chinese toolmakers are winning a growing share of their home market. They held 10 to 15 percent of it before 2022, 25 percent in 2024 and 35 percent in 2025². In March 2026 CSIS put their share of the Chinese market for etch and deposition tools at 40 percent². But in September 2025 CSIS judged that making its own extreme-ultraviolet machines remained firmly out of China's reach despite massive state investment⁵.

Chinese chipmakers remain behind at the leading edge, where TSMC makes 2 nm chips⁴⁶. SMIC's most advanced process, N+3, reaches the transistor density of TSMC's 6 nm-class process without extreme-ultraviolet scanners⁴⁷. It prints its tightest layers in several passes on deep-ultraviolet tools (see figure 04.2)⁴⁷.

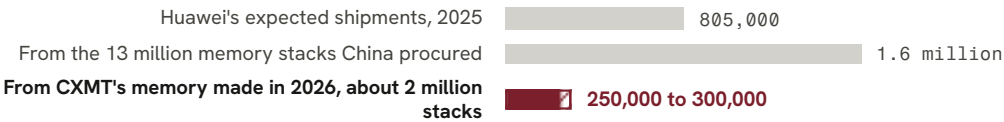
In September 2025 the research firm SemiAnalysis conservatively put SMIC's capacity at 7 nm and below at 45,000 wafers a month by the end of 2025⁴⁸. It expected 60,000 in 2026 and 80,000 in 2027⁴⁸. Those figures count wafers, and how many working chips they give depends on yield, the share of chips on a wafer that work.

SemiAnalysis judged that memory would limit China's output of AI chips before logic wafers did⁴⁸. It expected Huawei to ship about 805,000 of its Ascend AI chips in 2025, with dies made by both TSMC and SMIC⁴⁸. SemiAnalysis says Huawei got Ascend dies made at TSMC, in violation of export controls, while SMIC ramped up its own production⁴⁸. By its count, China had procured roughly 13 million memory stacks, enough for about 1.6 million Ascend 910C packages⁴⁸. It expected CXMT, China's own memory maker, to make only about 2 million stacks in 2026, enough for 250,000 to 300,000 more packages⁴⁸.

Figure 16.2

China's own memory could fill only 250,000 to 300,000 more Ascend packages in 2026

Huawei's Ascend AI chip packages, shipped in 2025 and possible from China's memory, as SemiAnalysis estimated in September 2025



SemiAnalysis expected CXMT, China's own memory maker, to make only about 2 million stacks in 2026, enough for 250,000 to 300,000 more packages.

Source: Huawei Ascend Production Ramp: Die Banks, TSMC Continued Production, HBM is The Bottleneck [48]

Huawei said in September 2025 that its Ascend 950 chips, due in 2026, would carry high-bandwidth memory of its own design⁴⁹. It gave no figure for how much of that memory it would make⁴⁹.

2 China's Localization Drive in Semiconductors Gains Impetus from Allied Chip... Center for Strategic and International Studies, 24 March 2026. csis.org

5 Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements. Center for Strategic and International Studies, 24 September 2025. csis.org

46 Why Taiwan Fears 'America First' Risks Eroding Its 'Silicon Shield'. Stimson Center, 10 October 2025. stimson.org

47 Is SMIC N+3's Metal Pitch Smaller than Intel 18A's? SemiAnalysis, 14 June 2026. newsletter.semianalysis.com

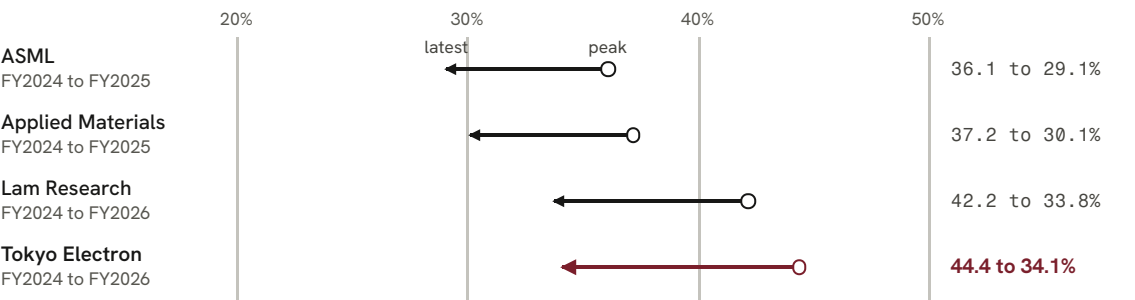
48 Huawei Ascend Production Ramp: Die Banks, TSMC Continued Production, HBM is The... SemiAnalysis, 8 September 2025. newsletter.semianalysis.com

49 Groundbreaking SuperPoD Interconnect: Leading a New Paradigm for AI... Huawei, 18 September 2025. huawei.com

Figure 16.3

China's revenue share fell at all four largest toolmakers after fiscal 2024

China's share of revenue at the four largest chip-tool makers, peak fiscal year and latest



Source: ASML 2025 Form 20-F (total net sales), Applied Materials and Lam Research 10-K filings and Tokyo Electron FY2024 and FY2026 consolidated financial statements, each China share computed from the filing's sales by region [50]

07

CHIPS Act, Big Fund, Rapidus and other subsidies

The US government helps pay for new chip plants with grants and a tax credit. The CHIPS and Science Act authorized about \$52.7 billion for manufacturing incentives, research and workforce support². By July 2025 Commerce had awarded \$30.9 billion of direct funding to 19 companies for 40 projects⁵¹. The grants covered a median 14.2 percent of each project's capital cost⁵¹. Commerce took a federal tax credit, the Advanced Manufacturing Investment Credit, into account when it set the size of those grants⁵¹. Since the One Big Beautiful Bill Act of 2025, the credit covers 35 percent of qualified investment in an advanced chip plant placed in service after 2025, up from 25 percent⁵¹.

On 22 August 2025 the US government agreed to take a 9.9 percent stake in Intel by buying \$8.9 billion of its stock⁵². Of that sum, \$5.7 billion was to come from CHIPS Act grants that Intel had been awarded but not yet paid⁵². The other \$3.2 billion was to come from Intel's award under Secure Enclave, a program to supply trusted and secure chips to the US Department of Defense⁵².

The United States has also used tariffs to draw chip investment. In January 2026 the American Institute in Taiwan and the Taipei Economic and Cultural Representative Office in the United States signed a memorandum on investment⁵³. Under it, Taiwanese chip and technology firms are to invest \$250 billion in US semiconductor, energy and AI production⁵³. In the same memorandum the United States agreed to cap some of its national-security tariffs on Taiwanese goods at 15 percent⁵³. On 16 July 2026

2 China's Localization Drive in Semiconductors Gains Impetus from Allied Chip... Center for Strategic and International Studies, 24 March 2026. csis.org

50 ASML Holding, annual report on Form 20-F for the fiscal year ended 31 December... U.S. Securities and Exchange Commission, 25 February 2026. sec.gov

51 GAO-26-107882, SEMICONDUCTORS: Information on Projects Funded to Strengthen... U.S. Government Accountability Office, 11 December 2025. files.gao.gov

52 Intel and Trump Administration Reach Historic Agreement to Accelerate American... Intel, 22 August 2025. intc.com

53 Implementing Certain Tariff-Related Elements of a Trade and Security Agreement... Federal Register, 28 May 2026. federalregister.gov

TSMC announced another \$100 billion for four more Arizona fabs, bringing its total Arizona investment to \$265 billion⁵⁴.

The European Commission says the EU still depends on other countries for advanced chip manufacturing⁵⁵. On 3 June 2026 the Commission proposed a Chips Act 2.0 to support advanced chip production in the EU⁵⁵.

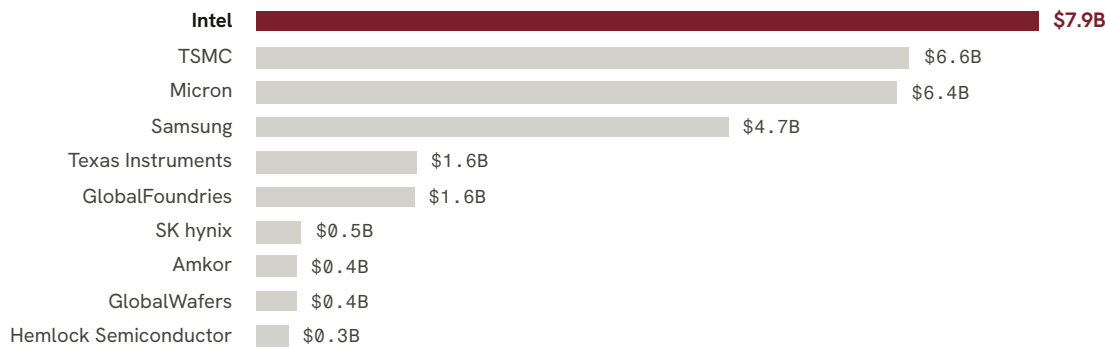
Japan backs a homegrown chipmaker, Rapidus. Rapidus began prototyping 2 nm gate-all-around transistors at its IIM-1 plant in July 2025⁵⁶. In February 2026 it raised another 267.6 billion yen, about \$1.7 billion, from Japan's Information-Technology Promotion Agency (IPA) and 32 companies, aiming for 2 nm mass production by 2027⁵⁷. By June 2026 it had raised 424.95 billion yen in equity in all, after a further 150 billion yen from the IPA⁵⁸.

CSIS puts China's cumulative state funding for chips since 2014 at an estimated \$150 billion and calls the CHIPS Act substantially smaller in scale². The latest round of China's National Integrated Circuit Industry Investment Fund, the Big Fund, reached \$47 billion⁵⁹. That round, the fund's third, was set up in May 2024⁶⁰.

Figure 16.4

Intel led CHIPS Act direct funding with \$7.865 billion by July 2025

CHIPS Act direct funding awarded, by firm, as of July 2025



Source: GAO-26-107882, Semiconductors: Information on Projects Funded to Strengthen U.S. Supply Chain [51]

08

Taiwan, TSMC and the silicon shield

The world relies on Taiwan for most of its advanced chips. Taiwan's foundries held 81.9 percent of the world's contract chipmaking market in 2025, according to the Taiwan

2 China's Localization Drive in Semiconductors Gains Impetus from Allied Chip... Center for Strategic and International Studies, 24 March 2026. csis.org

51 GAO-26-107882, SEMICONDUCTORS: Information on Projects Funded to Strengthen... U.S. Government Accountability Office, 11 December 2025. files.gao.gov

54 TSMC Announces Additional \$100 Billion Investment In Arizona. City of Phoenix, 16 July 2026. phoenix.gov

55 Proposal for the Chips Act 2.0. European Commission, 3 June 2026. digital-strategy.ec.europa.eu

56 Rapidus Achieves Significant Milestone at its State-of-the-Art Foundry with... Rapidus, 18 July 2025. rapidus.inc

57 Rapidus Secures 267.6 Billion Yen in Funding from Japan Government and Private... Rapidus, 27 February 2026. rapidus.inc

58 Rapidus Completes 150 Billion Yen Funding Round from Japan Government. Rapidus, 5 June 2026. rapidus.inc

59 China's Evolving Industrial Policy for AI. RAND Corporation, 26 June 2025. rand.org

60 Six banks to invest in big way in IC fund. The State Council of the People's Republic of China, 29 May 2024. english.www.gov.cn

Semiconductor Industry Association's August 2026 report⁶¹. TSMC makes its 2 nm chips only in Taiwan⁴⁶. Taiwan held 69 percent of the world's logic capacity below 10 nm in 2022⁴.

TSMC's advanced packaging capacity could not keep up with demand. Asked in October 2025 how much CoWoS packaging capacity he would add, TSMC's chairman said only that the company was "working very hard to narrow the gap between the demand and supply"⁶². He called wafer and packaging capacity both "very tight"⁶².

The silicon shield argument holds that this concentration deters an attack on Taiwan, because so many countries rely on its chips⁴⁶. The Stimson Center calls that open to debate, though many Taiwanese believe it⁴⁶.

With an eye to that shield, Taiwan's rules keep TSMC's newest process at home first⁴⁶. As a result, TSMC's Arizona fabs have run a generation behind its fabs in Taiwan⁴⁶. The Stimson Center expected 2 nm production in Arizona in 2028 at the earliest⁴⁶. TSMC said in October 2025 that it was "preparing to upgrade our technologies faster to N2 and more advanced process technologies in Arizona"⁶³. The four Arizona fabs it announced in July 2026 are to run at 2 nm or more advanced⁵⁴.

TSMC has also announced two advanced packaging fabs for Arizona⁶⁴. But TSMC's work in Taiwan rests on a local supply chain of more than 300 firms, which the Stimson Center judged extremely difficult to copy in the United States⁴⁶. The US push for chip plants at home has raised fears in Taiwan that the shield could weaken⁴⁶.

09

What each country gains and loses

- **Taiwan and Korea.** Fabs built abroad add capacity without taking any away from Taiwan and Korea. TSMC makes its 2 nm chips only in Taiwan⁴⁶. Korean firms took 82.5 percent of the world's high-bandwidth memory revenue in 2025, by the market research firm IDC's count¹².
- **The Netherlands and Japan.** Their toolmakers build the controlled machines, so the two governments gain a say in who gets them. China accounts for a falling share of the firms' sales. At ASML, China's share of net system sales fell from 41 percent in 2024 to 33 percent in 2025⁶⁵. That measure leaves out ASML's service and field option sales, which come from servicing and upgrading machines already installed⁶⁶. Against total net sales, the measure in the chart, it fell from 36.1 percent to 29.1

4 Emerging Resilience in the Semiconductor Supply Chain. Boston Consulting Group and Semiconductor Industry..., May 2024, p. 14. semiconductors.org

12 SK hynix, prospectus on Form 424B4 dated 10 July 2026. U.S. Securities and Exchange Commission, 10 July 2026. sec.gov

46 Why Taiwan Fears 'America First' Risks Eroding Its 'Silicon Shield'. Stimson Center, 10 October 2025. stimson.org

54 TSMC Announces Additional \$100 Billion Investment In Arizona. City of Phoenix, 16 July 2026. phoenix.gov

61 Overview on Taiwan Semiconductor Industry (2026 Edition). Taiwan Semiconductor Industry Association, 7 August 2026, p. 9. tsia.org.tw

62 Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese... Refinitiv StreetEvents, 16 October 2025, p. 7. investor.tsmc.com

63 Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese... Refinitiv StreetEvents, 16 October 2025, p. 5. investor.tsmc.com

64 Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese... Refinitiv StreetEvents, 16 October 2025, p. 13. investor.tsmc.com

65 ASML 2025 fourth-quarter and full-year results (investor presentation). ASML, 28 January 2026, p. 9. ourbrand.asml.com

66 ASML Holding, 2025 annual report, filed on Form 6-K. U.S. Securities and Exchange Commission, 25 February 2026. sec.gov

percent⁵⁰. At Tokyo Electron, China's share of sales fell from 44.4 percent in the year to March 2024 to 34.1 percent in the year to March 2026⁶⁷. The company said China's share of its sales dropped to 26.8 percent in the quarter to March 2026 because spending on leading-edge nodes grew faster than spending on mature nodes⁶⁸.

- **The United States.** The Semiconductor Industry Association, using data from World Semiconductor Trade Statistics, Gartner and Omdia, put US firms' share of all chip sales in 2025 at 53.4 percent, the highest since 1984⁶⁹. US firms also took 65 percent of the world's logic chip sales in 2022⁷⁰. Commerce expects the CHIPS-funded projects to lift the US share of global leading-edge logic chip manufacturing from 0 percent in 2022 to 20 percent by 2030⁵¹.
- **China.** Chinese suppliers are replacing foreign ones at home, most visibly in mature-node and commodity chips². In September 2025 SemiAnalysis expected China to make fewer Ascend chips in 2026 than in 2025 unless memory was smuggled in, because its own memory maker could supply too little⁴⁸.

Five questions to answer from memory

1. What does a country need for its export controls to work? see The shape of the contest
2. Which countries can control who gets the tools to make advanced chips?
see The shape of the contest
3. How do US export controls reach goods made in other countries?
see US export controls, 2018 to today
4. Where are most leading-edge chips made? see Taiwan
5. What did SemiAnalysis expect to limit China's output of AI chips first?
see China's response

Five things to remember

- An export control works only when a country's firms sell something the buyer cannot get elsewhere.
- US controls also cover some foreign goods made with American technology.
- Chinese toolmakers' share of China's own chipmaking equipment market rose from 10 to 15 percent before 2022 to 35 percent in 2025.
- China's share of ASML's and Tokyo Electron's sales has fallen since 2024.
- Taiwan held 69 percent of the world's logic capacity below 10 nm in 2022, and TSMC makes its 2 nm chips only there.

² China's Localization Drive in Semiconductors Gains Impetus from Allied Chip... Center for Strategic and International Studies, 24 March 2026. csis.org

⁴⁸ Huawei Ascend Production Ramp: Die Banks, TSMC Continued Production, HBM is The... SemiAnalysis, 8 September 2025. newsletter.semianalysis.com

⁵⁰ ASML Holding, annual report on Form 20-F for the fiscal year ended 31 December... U.S. Securities and Exchange Commission, 25 February 2026. sec.gov

⁵¹ GAO-26-107882, SEMICONDUCTORS: Information on Projects Funded to Strengthen... U.S. Government Accountability Office, 11 December 2025. files.gao.gov

⁶⁷ FY2026 (April 2025-March 2026) Financial Announcement, transcript. Tokyo Electron, 30 April 2026, p. 27. tel.com

⁶⁸ FY2026 (April 2025-March 2026) Financial Announcement, transcript. Tokyo Electron, 30 April 2026, p. 5. tel.com

⁶⁹ 2026 State of the U.S. Semiconductor Industry. Semiconductor Industry Association, 2 July 2026, p. 7. semiconductors.org

⁷⁰ Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO), accessed 9 September 2026. chipexplorer.eto.tech

Sources (70)

1. A **Where the Chips Fall: U.S. Export Controls Under the Biden Administration from 2022 to 2024.** Center for Strategic and International Studies · 12 December 2024
www.csis.org/analysis/where-chips-fall-us-export-controls-under-biden-administration-2022-2024
2. A **China's Localization Drive in Semiconductors Gains Impetus from Allied Chip Export Controls.** Center for Strategic and International Studies · 24 March 2026
www.csis.org/analysis/chinas-localization-drive-semiconductors-gains-impetus-allied-chip-export-controls
3. A **Nvidia, quarterly report on Form 10-Q for the quarter ended 26 July 2026.** U.S. Securities and Exchange Commission (filing by Nvidia) · 26 August 2026
www.sec.gov/Archives/edgar/data/1045810/000104581026000075/nvda-20260726.htm
4. A **Emerging Resilience in the Semiconductor Supply Chain.** Boston Consulting Group and Semiconductor Industry Association · May 2024 · p. 14
www.semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconductor-Supply-Chain.pdf#page=14
5. A **Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements.** Center for Strategic and International Studies · 24 September 2025
www.csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chinese-lithography
6. A **Remarks by National Security Advisor Jake Sullivan at the Special Competitive Studies Project Global Emerging Technologies Summit.** The White House · 16 September 2022
[bidenwhitehouse.archives.gov/briefing-room/speeches-remarks/2022/09/16/remarks-by-national-security-advisor-jake-sullivan-at-the-special-competitive-studies-project-global-emerging-technologies-summit/](https://www.bidenwhitehouse.archives.gov/briefing-room/speeches-remarks/2022/09/16/remarks-by-national-security-advisor-jake-sullivan-at-the-special-competitive-studies-project-global-emerging-technologies-summit/)
7. A **Choking off China's Access to the Future of AI.** Center for Strategic and International Studies · 11 October 2022
www.csis.org/analysis/choking-chinas-access-future-ai
8. A **Addition of an Entity to the Entity List.** Federal Register (Commerce Department; Industry and Security Bureau) · 30 October 2018
www.federalregister.gov/documents/2018/10/30/2018-23693/addition-of-an-entity-to-the-entity-list
9. A **Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification.** Federal Register (Commerce Department; Industry and Security Bureau) · 13 October 2022
www.federalregister.gov/documents/2022/10/13/2022-21658/implementation-of-additional-export-controls-certain-advanced-computing-and-semiconductor
10. A **Documentation: Semiconductor Supply Chain Dataset.** Emerging Technology Observatory (ETO) · Accessed 9 September 2026
eto.tech/dataset-docs/chipexplorer
11. A **METI, Semiconductor and digital industry strategy: future direction (半導体・デジタル産業戦略の今後の方向性),** 23 December 2025. Ministry of Economy, Trade and Industry (Japan) · 23 December 2025 · p. 8
www.meti.go.jp/policy/mono_info_service/joho/conference/semicon_digital/0014/handejii14-4.pdf#page=8
12. A **SK hynix, prospectus on Form 424B4 dated 10 July 2026.** U.S. Securities and Exchange Commission (filing by SK hynix) · 10 July 2026
www.sec.gov/Archives/edgar/data/0002120882/000119312526299963/d32785d424b4.htm
13. A **Addition of Huawei Non-U.S. Affiliates to the Entity List, the Removal of Temporary General License, and Amendments to General Prohibition Three (Foreign-Produced Direct Product Rule).** Federal Register (Commerce Department; Industry and Security Bureau) · 20 August 2020
www.federalregister.gov/documents/2020/08/20/2020-18213/addition-of-huawei-non-us-affiliates-to-the-entity-list-the-removal-of-temporary-general-license-and
14. A **Nvidia, annual report on Form 10-K for the fiscal year ended 25 January 2026.** U.S. Securities and Exchange Commission (filing by Nvidia) · 25 February 2026
www.sec.gov/Archives/edgar/data/1045810/000104581026000021/nvda-20260125.htm
15. A **Statement on UAE and Saudi Chip Exports.** U.S. Department of Commerce · November 2025
www.commerce.gov/news/press-releases/2025/11/statement-uae-and-saudi-chip-exports
16. A **Enhanced Favorable Treatment for the United Arab Emirates Under the Export Administration Regulations.** Federal Register (Commerce Department; Industry and Security Bureau) · 14 July 2026
www.federalregister.gov/documents/2026/07/14/2026-14132/enhanced-favorable-treatment-for-the-united-arab-emirates-under-the-export-administration
17. A **15 CFR 734.13 -- Export..** Electronic Code of Federal Regulations · 3 June 2016
www.ecfr.gov/current/title-15/subtitle-B/chapter-VII/subchapter-C/part-734/section-734.13
18. A **Framework for Artificial Intelligence Diffusion.** Federal Register (Commerce Department; Industry and Security Bureau) · 15 January 2025
www.federalregister.gov/documents/2025/01/15/2025-00636/framework-for-artificial-intelligence-diffusion
19. A **Department of Commerce Announces Rescission of Biden-Era Artificial Intelligence Diffusion Rule, Strengthens Chip-Related Export Controls.** U.S. Bureau of Industry and Security · 13 May 2025
www.bis.gov/press-release/department-commerce-rescinds-biden-era-artificial-intelligence-diffusion-rule-strengthens-chip-related
20. A **Revision to License Review Policy for Advanced Computing Commodities.** U.S. Government Publishing Office (Federal Register) · 15 January 2026
www.govinfo.gov/content/pkg/FR-2026-01-15/html/2026-00789.htm

21. A **Export, transshipment and transit of high-performance AI chips of US origin now subject to a Strategic Trade Permit.** Ministry of Investment, Trade and Industry (MITI), Malaysia · 14 July 2025
www.miti.gov.my/miti/resources/Media%20Release/%5BFINAL%5D_MITI_Press_Stmt_Malaysia_Regulates_Trade_of_US_AI_Chips_2025-07-14.pdf
22. A **Chinese National and Two U.S. Citizens Charged with Conspiring to Smuggle Artificial Intelligence Technology to China.** U.S. Department of Justice · 25 March 2026
www.justice.gov/opa/pr/chinese-national-and-two-us-citizens-charged-conspiring-smuggle-artificial-intelligence
23. A **Protecting U.S. Tech: China Committee and Bipartisan, Bicameral Leaders Unite to Stop CCP AI Chip Smuggling.** U.S. House Select Committee on the Chinese Communist Party · 7 July 2025
chineselectcommittee.house.gov/media/press-releases/protecting-us-tech-china-committee-and-bipartisan-bicameral-leaders-unite-to-stop-ccp-ai-chip-smuggling
24. A **S.1705 – Chip Security Act, 119th Congress (2025-2026), bill text.** U.S. Congress (Congress.gov, Library of Congress) · 8 May 2025
www.congress.gov/bill/119th-congress/senate-bill/1705/text
25. A **UNANIMOUS: Bipartisan Huizenga Legislation to Curb AI Chip Smuggling Passes Committee.** U.S. House of Representatives (Office of Rep. Bill Huizenga) · 26 March 2026
huizenga.house.gov/news/documentsingle.aspx?DocumentID=404259
26. A **The Netherlands expands export control measure for advanced semiconductor manufacturing equipment.** Government of the Netherlands · 6 September 2024
www.government.nl/latest/news/2024/09/06/the-netherlands-expands-export-control-measure-advanced-semiconductor-manufacturing-equipment
27. A **Klever: export controls on advanced semiconductor manufacturing equipment to be tightened.** Government of the Netherlands · 15 January 2025
www.government.nl/latest/news/2025/01/15/klever-export-controls-on-advanced-semiconductor-manufacturing-equipment-to-be-tightened
28. A **CSIS Translation: Updated Japanese Export Controls on High-Performance Semiconductor Manufacturing Equipment.** Center for Strategic and International Studies · 18 July 2023
www.csis.org/analysis/csis-translation-updated-japanese-export-controls-high-performance-semiconductor
29. A **Revocation of Validated End-User Authorizations in the People's Republic of China.** Federal Register (Commerce Department; Industry and Security Bureau) · 2 September 2025
www.federalregister.gov/documents/2025/09/02/2025-16735/revocation-of-validated-end-user-authorizations-in-the-peoples-republic-of-china
30. A **Department of Commerce Closes Export Controls Loophole for Foreign-Owned Semiconductor Fabs in China.** U.S. Bureau of Industry and Security · 29 August 2025
www.bis.gov/press-release/department-commerce-closes-export-controls-loophole-foreign-owned-semiconductor-fabs-china
31. A **SK hynix, prospectus on Form 424B4 dated 10 July 2026.** U.S. Securities and Exchange Commission (filing by SK hynix) · 10 July 2026
www.sec.gov/Archives/edgar/data/2120882/000119312526299963/d32785d424b4.htm
32. A **Expansion of End-User Controls To Cover Affiliates of Certain Listed Entities.** Federal Register (Commerce Department; Industry and Security Bureau) · 30 September 2025
www.federalregister.gov/documents/2025/09/30/2025-19001/expansion-of-end-user-controls-to-cover-affiliates-of-certain-listed-entities
33. A **Update on invoking Goods Availability Act - 19 november 2025.** Government of the Netherlands · 19 November 2025
www.government.nl/site/binaries/site-content/collections/documents/2025/11/19/update-on-invoking-goods-availability-act/Update+on+invoking+Goods+Availability+Act++19+november+2025.pdf
34. A **Minister of Economic Affairs invokes Goods Availability Act.** Government of the Netherlands · 12 October 2025
www.government.nl/latest/news/2025/10/12/minister-of-economic-affairs-invokes-goods-availability-act
35. A **Developments concerning Nexperia, letter to the House of Representatives.** Government of the Netherlands (Ministry of Economic Affairs) · 19 November 2025
www.government.nl/site/binaries/site-content/collections/documents/2025/11/19/letter-to-the-parliament-on-the-latest-developments-concerning-nexperia/102176837+Developments+concerning+Nexperia.pdf
36. A **One Year Suspension of Expansion of End-User Controls for Affiliates of Certain Listed Entities.** Federal Register (Commerce Department; Industry and Security Bureau) · 12 November 2025
www.federalregister.gov/documents/2025/11/12/2025-19846/one-year-suspension-of-expansion-of-end-user-controls-for-affiliates-of-certain-listed-entities
37. A **Risch, Ricketts, Kim Introduce MATCH Act; Level the Global Playing Field for U.S. Tech.** U.S. Senate Committee on Foreign Relations · 8 April 2026
www.foreign.senate.gov/press/rep/release/risch-ricketts-kim-introduce-match-act-level-the-global-playing-field-for-us-tech
38. A **Cyberspace Administration of China, notice on the cybersecurity review of Micron products (美光公司在华销售的产品未通过网络安全审查), 21 May 2023.** Cyberspace Administration of China · 21 May 2023
www.cac.gov.cn/2023-05/21/c_1686348043518073.htm
39. A **Beijing blocks Nvidia sales in vote of confidence for Chinese chipmakers, the White House strikes a deal for 10 percent of Intel, and Commerce voids a \$7.4B CHIPS Act grant.** Center for Security and Emerging Technology (CSET) · 18 September 2025
cset.georgetown.edu/newsletter/september-18-2025/

40. A **Ministry of Commerce Notice 2024 No. 46: Notice Concerning Strengthening Controls on Exports of Relevant Dual-Use Items to the United States.** Center for Security and Emerging Technology (CSET) · 3 December 2024
cset.georgetown.edu/publication/china-rare-earth-export-ban/
41. A **Announcement No.18 of 2025 of The Ministry of Commerce and The General Administration of Customs of The People's Republic of China Announcing the decision to implement export control on some medium and heavy rare earth related items.** Ministry of Commerce of the People's Republic of China · 4 April 2025
english.mofcom.gov.cn/Policies/AnnouncementsOrders/art/2025/art_0dd87cbee7b045bf93fab6ab2faceee.html
42. A **Ministry of Commerce Notice 2025 No. 61: Announcement of the Decision to Implement Controls on Exports of Rare Earth-Related Items to Foreign Countries (translation).** Center for Security and Emerging Technology (CSET) · 9 October 2025
cset.georgetown.edu/wp-content/uploads/t0656_china_rare_earth_controls_2025_61_EN.pdf
43. A **MOFCOM and GAC Announcement 2025 No. 70, suspending the October 2025 export-control measures, Announcements Nos. 55 to 58, 61 and 62 (商务部、海关总署公告2025年第70号).** Ministry of Commerce of the People's Republic of China · 7 November 2025
www.mofcom.gov.cn/zwgk/zcfb/art/2025/art_b1ec77dd3f0d4762952904df7cdaadec.html
44. A **商务部公告2025年第72号 公布调整实施商务部公告2024年第46号的决定.** Ministry of Commerce of the People's Republic of China · 9 November 2025
www.mofcom.gov.cn/zwgk/zcfb/art/2025/art_5c68985a6b1a46778e2e8dbff1bb1601.html
45. A **The U.S.-China Trade Truce Has Not Solved the Gallium Problem.** Center for Strategic and International Studies · 11 May 2026
www.csis.org/analysis/us-china-trade-truce-has-not-solved-gallium-problem
46. A **Why Taiwan Fears 'America First' Risks Eroding Its 'Silicon Shield'.** Stimson Center · 10 October 2025
www.stimson.org/2025/why-taiwan-fears-america-first-risks-eroding-its-silicon-shield/
47. B **Is SMIC N+3's Metal Pitch Smaller than Intel 18A's?.** SemiAnalysis · 14 June 2026
newsletter.semianalysis.com/p/steel-smic-n3-teardown
48. B **Huawei Ascend Production Ramp: Die Banks, TSMC Continued Production, HBM is The Bottleneck.** SemiAnalysis · 8 September 2025
newsletter.semianalysis.com/p/huawei-ascend-production-ramp
49. A **Groundbreaking SuperPoD Interconnect: Leading a New Paradigm for AI Infrastructure.** Huawei · 18 September 2025
www.huawei.com/en/news/2025/9/hc-xu-keynote-speech
50. A **ASML Holding, annual report on Form 20-F for the fiscal year ended 31 December 2025, financial statement table.** U.S. Securities and Exchange Commission (filing by ASML Holding) · 25 February 2026
www.sec.gov/Archives/edgar/data/937966/000162828026011378/R71.htm
51. A **GAO-26-107882, SEMICONDUCTORS: Information on Projects Funded to Strengthen U.S. Supply Chain.** U.S. Government Accountability Office · 11 December 2025
files.gao.gov/reports/GAO-26-107882/index.html
52. A **Intel and Trump Administration Reach Historic Agreement to Accelerate American Technology and Manufacturing Leadership.** Intel · 22 August 2025
www.intel.com/news-events/press-releases/detail/1748/intel-and-trump-administration-reach-historic-agreement-to
53. A **Implementing Certain Tariff-Related Elements of a Trade and Security Agreement Between the American Institute in Taiwan and the Taipei Economic and Cultural Representative Office in the United States.** Federal Register (Commerce Department; International Trade Administration; Trade Representative, Office of United States) · 28 May 2026
www.federalregister.gov/documents/2026/05/28/2026-10571/implementing-certain-tariff-related-elements-of-a-trade-and-security-agreement-between-the-american
54. A **TSMC Announces Additional \$100 Billion Investment In Arizona.** City of Phoenix · 16 July 2026
www.phoenix.gov/newsroom/ced-news/tsmc-announces-additional--100-billion-investment-in-arizona.html
55. A **Proposal for the Chips Act 2.0.** European Commission · 3 June 2026
digital-strategy.ec.europa.eu/en/library/proposal-chips-act-20
56. A **Rapidus Achieves Significant Milestone at its State-of-the-Art Foundry with Prototyping of Leading-Edge 2nm GAA Transistors.** Rapidus · 18 July 2025
www.rapidus.inc/en/news_topics/information/rapidus-achieves-significant-milestone-at-its-state-of-the-art-foundry-with-prototyping-of-leading-edge-2nm-gaa-transistors/
57. A **Rapidus Secures 267.6 Billion Yen in Funding from Japan Government and Private Sector Companies.** Rapidus · 27 February 2026
www.rapidus.inc/en/news_topics/information/rapidus-secures-267-6-billion-yen-in-funding-from-japan-government-and-private-sector-companies/
58. A **Rapidus Completes 150 Billion Yen Funding Round from Japan Government.** Rapidus · 5 June 2026
www.rapidus.inc/en/news_topics/information/20260605-2/
59. A **China's Evolving Industrial Policy for AI.** RAND Corporation · 26 June 2025
www.rand.org/pubs/perspectives/PEA4012-1.html
60. A **Six banks to invest in big way in IC fund.** The State Council of the People's Republic of China · 29 May 2024
english.www.gov.cn/news/202405/29/content_WS66569746c6d0868f4e8e7987.html
61. A **Overview on Taiwan Semiconductor Industry (2026 Edition).** Taiwan Semiconductor Industry Association · 7 August 2026 · p. 9
www.tsia.org.tw/api/DownloadOverview?ID=36&page=9

62. A Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 October 2025 · p. 7
investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2025-10/6860312f04fd291d0f26b46c1234f84e6332717e/TSMC%203Q25%20Transcript.pdf#page=7
63. A Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 October 2025 · p. 5
investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2025-10/6860312f04fd291d0f26b46c1234f84e6332717e/TSMC%203Q25%20Transcript.pdf#page=5
64. A Q3 2025 Taiwan Semiconductor Manufacturing Co Ltd Earnings Call (Chinese, English) — edited transcript. Refinitiv StreetEvents (transcript of a TSMC earnings call), via TSMC · 16 October 2025 · p. 13
investor.tsmc.com/english/encrypt/files/encrypt_file/reports/2025-10/6860312f04fd291d0f26b46c1234f84e6332717e/TSMC%203Q25%20Transcript.pdf#page=13
65. A ASML 2025 fourth-quarter and full-year results (investor presentation). ASML · 28 January 2026 · p. 9
ourbrand.asml.com/m/3136300aa4999bc1/original/2026_01_28_Presentation-Investor-Relations-Q4-2025.pdf#page=9
66. A ASML Holding, 2025 annual report, filed on Form 6-K. U.S. Securities and Exchange Commission (filing by ASML Holding) · 25 February 2026
www.sec.gov/Archives/edgar/data/937966/000162828026011377/asml-2025xannualxreportx.htm
67. A FY2026 (April 2025-March 2026) Financial Announcement, transcript. Tokyo Electron · 30 April 2026 · p. 27
www.tel.com/ir/library/report/pjuomj00000000tf-att/fy26q4transcript-e.pdf#page=27
68. A FY2026 (April 2025-March 2026) Financial Announcement, transcript. Tokyo Electron · 30 April 2026 · p. 5
www.tel.com/ir/library/report/pjuomj00000000tf-att/fy26q4transcript-e.pdf#page=5
69. A 2026 State of the U.S. Semiconductor Industry. Semiconductor Industry Association · 2 July 2026 · p. 7
www.semiconductors.org/wp-content/uploads/2026/07/SIA_2026_State-of-the-Semiconductor-Industry.pdf#page=7
70. A Supply Chain Explorer: Advanced Chips. Emerging Technology Observatory (ETO) · Accessed 9 September 2026
chipexplorer.eto.tech/?parentNode=N0&selectedNode=N6

Made by Yashvardhan Sharma. Corrections and questions:
contact@chipsupplychain.org.

A company filings, governments, standards bodies, universities and research institutions; B SemiAnalysis, Reuters, the Financial Times and Nikkei Asia.

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