

Chapter 8: Transistors and the Front End

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CHAPTER

08

STAGE 8 OF 15

Transistors and the Front End

Only TSMC, Intel and Samsung make 2 nm-class transistors in volume. TSMC plans its A14 process for 2028, with more than 20 percent higher logic density than N2.

IN PLAIN TERMS

The front end of a chip factory is the part that builds the transistors, the billions of tiny switches in every chip. Each switch works like a valve. Current runs along a narrow strip of silicon called the channel, and a small voltage on a gate above the strip opens or shuts the flow. For decades chipmakers made the strips shorter, so they switched faster and more of them fit on a chip. But once the strip gets short enough, the valve stops sealing. Current leaks through even when the gate is off, and the chip burns power doing nothing. The newest kind of transistor, called gate-all-around, cuts this leak by wrapping the gate around all four sides of the strip. Building them takes a long sequence of steps that have to run in exact order. Only three companies, TSMC, Intel and Samsung, make these switches in volume. In 2024 the United States put a worldwide license requirement on the know-how for building them, with an exception for countries that impose matching controls.

IN SHORT

Intel's 18A process shipped gate-all-around transistors together with backside power, a second power network built underneath them ¹¹. TSMC says its A14 process will give up to 15 percent more speed or up to 30 percent less power than N2 ²². Rapidus, a state-backed newcomer in Japan, said in July 2025 that it would begin 2 nm mass production in 2027 ⁷.

China's SMIC makes 7 nm-class chips without extreme-ultraviolet (EUV) lithography, the most advanced way to print chip patterns ⁶. China has announced \$43 billion to develop its own EUV ³⁴. In September 2025 the Center for Strategic and International Studies judged that EUV remains firmly out of reach ³⁴.

¹¹ Intel Foundry Details Process Milestones and Future Innovation at VLSI Symposium. Intel · 16 June 2026 ^[A] www.intel.com/news-events/press-releases/detail/1772/intel-foundry-details-process-milestones-and-future

²² TSMC Unveils Next-Generation A14 Process at North America Technology Symposium. TSMC · 24 April 2025 ^[A] pr.tsmc.com/english/news/3228

⁷ Rapidus Achieves Significant Milestone at its State-of-the-Art Foundry with Prototyping of Leading-Edge 2nm GAA Transistors. Rapidus · 18 July 2025 ^[A] www.rapidus.inc/en/news_topics/information/rapidus-achieves-significant-milestone-at-its-state-of-the-art-foundry-with-prototyping-of-leading-edge-2nm-gaa-transistors/

⁶ Is SMIC N+3's Metal Pitch Smaller than Intel 18A's?. SemiAnalysis · 14 June 2026 ^[B] newsletter.semianalysis.com/p/steel-smic-n3-teardown

³⁴ Breakthroughs or Boasts? Assessing Recent Chinese Lithography Advancements. Center for Strategic and International Studies · 24 September 2025 ^[A] www.csis.org/blogs/strategic-technologies-blog/breakthroughs-or-boasts-assessing-recent-chinese-lithography

CHOKEPOINT CARD		EXTREME CONCENTRATION	HARD TO SUBSTITUTE
CONCENTRATION	SUBSTITUTABILITY		PRICE OR MARKET SIZE
Extreme	Hard		\$17,000
	TSMC, Intel and Samsung all make chips with gate-all-around transistors, the newest kind ¹ .		per 300 mm wafer on TSMC's 4NP process, Epoch AI's December 2025 estimate ²
WHO LEADS	TW TSMC N2 in volume production since 4Q25, TSMC's first nanosheet node³ US Intel 18A in high-volume production in the United States, as of 2026⁴ KR Samsung Foundry Started initial production of its 3 nm gate-all-around process in June 2022⁵ CN SMIC N+3, a 7 nm-class process made without EUV, SemiAnalysis found in June 2026⁶ JP Rapidus Said in July 2025 it would begin 2 nm mass production in 2027⁷		
WHERE IT IS MADE	TW Taiwan TSMC N2 at Fab 20 Hsinchu and Fab 22 Kaohsiung US United States Intel 18A at Fab 52, Arizona KR South Korea Samsung Hwaseong and Pyeongtaek JP Japan Rapidus Chitose, Hokkaido CN China SMIC Shanghai and Beijing 300 mm lines		
WHY SUBSTITUTION IS SLOW	Rapidus, a newcomer, is building on IBM's 2 nm technology under a December 2022 agreement ⁸ . Since September 2024 the United States has required a license to share the know-how for building these transistors, except with countries that impose matching controls ⁹ .		
WHERE CHINA STANDS		WHERE THE US STANDS	
SMIC ships its N+3 process, which SemiAnalysis measured in June 2026 at 113.4 million transistors per square millimeter ⁶ . It builds its tightest layers in several patterning steps because it cannot buy an extreme-ultraviolet scanner ⁶ .		In August 2025 Intel called itself the only chipmaker that both develops and manufactures leading-edge logic chips in the United States ¹⁰ . It says its 18A process brought gate-all-around transistors and backside power to market together in 2025 ¹¹ .	

1 Intel Panther Lake Teardown. SemiAnalysis · 26 September 2026 [B] newsletter.semianalysis.com/p/intel-panther-lake-teardown

2 NVIDIA's B200 costs around \$6,400 to produce. Epoch AI · 10 December 2025 [A] epoch.ai/data-insights/b200-cost-breakdown

3 2nm Technology. TSMC · Accessed 9 September 2026 [A] www.tsmc.com/english/dedicatedFoundry/technology/logic/l_2nm

4 Intel 18A: See Our Biggest Process Innovation. Intel · Accessed 18 October 2026 [A] www.intel.com/content/www/us/en/foundry/process/18a.html

5 Samsung Begins Chip Production Using 3nm Process Technology With GAA Architecture. Samsung Global Newsroom · 30 June 2022 [A] news.samsung.com/global/samsung-begins-chip-production-using-3nm-process-technology-with-gaa-architecture

6 Is SMIC N+3's Metal Pitch Smaller than Intel 18A's?. SemiAnalysis · 14 June 2026 [B] newsletter.semianalysis.com/p/steel-smic-n3-teardown

7 Rapidus Achieves Significant Milestone at its State-of-the-Art Foundry with Prototyping of Leading-Edge 2nm GAA Transistors. Rapidus · 18 July 2025 [A] www.rapidus.inc/en/news_topics/information/rapidus-achieves-significant-milestone-at-its-state-of-the-art-foundry-with-prototyping-of-leading-edge-2nm-gaa-transistors/

Nvidia's Blackwell GPU holds 208 billion switches on two dies, each die the largest a lithography machine can print in one shot ¹². Every switch has to turn on fully, let almost no current through when off, and keep doing it for years. Making the switches is called the front end of line. Wiring them together is the back end of line.

How it works

The front end builds the transistors in a fixed order, starting with the channel. In a FinFET, the older design, the fab etches the silicon into thin fins that stand up from the wafer. The gate then goes over the top and both sides of each fin, three sides instead of one.

In a gate-all-around transistor, the fab instead grows alternating layers of silicon and silicon-germanium and cuts the stack into narrow bars ¹³. It lays a placeholder, called a dummy gate, across each bar where the real gate will go ¹⁴. On either side of the placeholder it cuts deep trenches where the source and drain, the two ends of the channel, will go ¹⁵. Through those trenches it etches the silicon-germanium layers back a little and fills the gaps with an insulator, the inner spacer, which keeps the gate apart from the source and drain ¹³. Then it grows the source and drain as crystal inside the trenches, a step called epitaxy ¹⁵.

Only then does the fab remove the placeholder and etch away the silicon-germanium, leaving thin silicon sheets that hang between the source and drain like shelves ¹³. The inner spacer shields the source and drain from that etch ¹⁴. The fab coats every sheet with an insulating film a few atoms thick, so the gate can control the channel without touching it. Gate metal then fills the gaps above, below and beside each sheet, covering all four sides ¹⁶. Last come the contacts,

8 IBM and Rapidus Form Strategic Partnership to Build Advanced Semiconductor Technology and Ecosystem in Japan.

Rapidus · 13 December 2022 [A] www.rapidus.inc/en/news_topics/information/ibm-and-rapidus-form-strategic-partnership-to-build-advanced-semiconductor-technology-and-ecosystem-in-japan/

9 Commerce Control List Additions and Revisions; Implementation of Controls on Advanced Technologies Consistent With Controls Implemented by International Partners. Federal Register (Commerce Department; Industry and Security Bureau) · 6 September 2024 [A] www.federalregister.gov/documents/2024/09/06/2024-19633/commerce-control-list-additions-and-revisions-implementation-of-controls-on-advanced-technologies

6 Is SMIC N+3's Metal Pitch Smaller than Intel 18A's?. SemiAnalysis · 14 June 2026 [B] newsletter.semianalysis.com/p/steel-smic-n3-teardown

10 Intel and Trump Administration Reach Historic Agreement to Accelerate American Technology and Manufacturing Leadership. Intel · 22 August 2025 [A] www.intc.com/news-events/press-releases/detail/1748/intel-and-trump-administration-reach-historic-agreement-to

11 Intel Foundry Details Process Milestones and Future Innovation at VLSI Symposium. Intel · 16 June 2026 [A] www.intc.com/news-events/press-releases/detail/1772/intel-foundry-details-process-milestones-and-future

12 NVIDIA Blackwell Architecture. Nvidia · 18 December 2025 [A] www.nvidia.com/en-us/data-center/technologies/blackwell-architecture/

13 Entering the nanosheet transistor era. imec · 11 February 2022 [A] www.imec-int.com/en/articles/entering-nanosheet-transistor-era-0

14 Development of SiGe Indentation Process Control for Gate-All-Around FET Technology Enablement. arXiv · 12 January 2022 [A] arxiv.org/abs/2201.04725

15 Applied Materials Unveils Next-Gen Chipmaking Products to Supercharge AI Performance. Applied Materials · 7 October 2025 [A] ir.appliedmaterials.com/news-releases/news-release-details/applied-materials-unveils-next-gen-chipmaking-products

16 Applied Materials Technologies Enable 2D Scaling with EUV and 3D Gate-All-Around Transistors. Applied Materials · 21 April 2022 [A] ir.appliedmaterials.com/news-releases/news-release-details/applied-materials-technologies-enable-2d-scaling-euv-and-3d-gate

small metal plugs down to the source, the drain and the gate, ready for the wiring layers above.

Each of those steps is a separate deposition, etch or implant. An implant step, called ion implantation, fires atoms of boron or phosphorus into chosen patches of silicon so they conduct the way the design needs. The steps have to run in exact order, because later layers cover earlier ones. Once gate metal surrounds a sheet, the insulator can no longer go between them.

Current leaks in two main ways, straight through the gate insulator and along the channel from end to end while the gate is off. The second grows as the channel gets shorter, and wrapping the gate around the channel reduces it. Three fixes deal with the two leaks:

- **Better insulator.** A thicker hafnium-based film, paired with a metal gate, lets fewer electrons slip straight through yet controls the channel as tightly as before. Intel replaced the silicon dioxide insulator with it at 45 nm in 2007¹⁷. It said the new film cut leakage through the insulator more than tenfold¹⁷. With the metal gate, it could either raise the current a switch carries when on by more than 20 percent or cut leakage along the channel more than fivefold¹⁷.
- **More gate.** Fins and nanosheets wrap gate metal around more sides of the channel.
- **Thinner channel.** The fab thins the silicon until no current can flow where the gate cannot reach it.

Variants and trade-offs

Planar and FinFET

A planar transistor lays the gate on one side of a flat channel. As the channel shortens, the gate loses control of it. A fin stands the channel on edge so the gate covers three sides. But each fin adds a fixed amount of current, so a designer who needs more current has to add a whole fin.

Gate-all-around nanosheets

A nanosheet transistor lays the channel flat again, stacks two to four thin sheets and wraps gate metal around each one. The sheets can be drawn at different widths, so current can be set in finer steps. TSMC sells this as NanoFlex, which lets designers mix short logic cells for small area with tall cells for performance¹⁸.

TSMC's N2, its first nanosheet node, entered volume production in the fourth quarter of 2025³. TSMC rates the follow-on N2P at 18 percent more speed at the

¹⁷ Intel's Transistor Technology Breakthrough Represents Biggest Change to Computer Chips in 40 Years. Intel · 27 January 2007 [A] www.intel.com/pressroom/archive/releases/2007/20070128comp.htm

¹⁸ TSMC Celebrates 30th North America Technology Symposium with Innovations Powering AI with Silicon Leadership. TSMC · 24 April 2024 [A] pr.tsmc.com/english/news/3136

³ 2nm Technology. TSMC · Accessed 9 September 2026 [A] www.tsmc.com/english/dedicatedFoundry/technology/logic/l_2nm

same power and 36 percent less power at the same speed than its earlier N3E ¹⁹. It gives N2P 1.2 times the logic density of N3E and 1.15 times its chip density, two separate measures ¹⁹.

Intel's version, called RibbonFET, is built into its 18A process, which Intel says is in high-volume production in the United States ⁴. An improved version, 18A-P, adds another 9 percent performance at the same power ¹¹. Samsung got there first, starting initial production of its 3 nm gate-all-around process in June 2022 ⁵. But SemiAnalysis reported in February 2023 that, because of yield problems, high-volume chips on Samsung's 3 nm gate-all-around technology were expected only in 2024 ²⁰.

Those numbers are the foundries' own claims until someone measures the silicon. Each foundry picks its own baseline, and none publishes a density figure that can be compared with a rival's.

TSMC's published chip density gains (a separate measure from the logic density it also quotes), each over the baseline TSMC names, with A16 at its stated maximum %



Source: TSMC advanced technologies, HPC platform

Backside power delivery

In a conventional chip, power and signal share one stack of copper wiring above the transistors, where wide power rails crowd out the signal wires. With backside power, the fab grinds the wafer thin and builds a second network for power underneath it.

Intel's version, PowerVia, is part of 18A, and Intel calls it an industry first ⁴. It cut routed area by 11 percent and dynamic voltage droop tenfold ¹¹. Droop is the sag

¹⁹ HPC Platform – Advanced Technologies. TSMC · Accessed 9 September 2026 [\[A\]](#)
www.tsmc.com/english/dedicatedFoundry/technology/platform_HPC_tech_advancedTech

⁴ Intel 18A: See Our Biggest Process Innovation. Intel · Accessed 18 October 2026 [\[A\]](#)
www.intel.com/content/www/us/en/foundry/process/18a.html

¹¹ Intel Foundry Details Process Milestones and Future Innovation at VLSI Symposium. Intel · 16 June 2026 [\[A\]](#) www.intc.com/news-events/press-releases/detail/1772/intel-foundry-details-process-milestones-and-future

⁵ Samsung Begins Chip Production Using 3nm Process Technology With GAA Architecture. Samsung Global Newsroom · 30 June 2022 [\[A\]](#) news.samsung.com/global/samsung-begins-chip-production-using-3nm-process-technology-with-gaa-architecture

²⁰ The Future of the Transistor. SemiAnalysis · 21 February 2023 [\[B\]](#) newsletter.semianalysis.com/p/the-future-of-the-transistor

in supply voltage when a block of logic switches on at once. TSMC's Super Power Rail connects the backside network directly to each transistor's source and drain, the two ends of its channel ²¹. Against N2P, TSMC rates A16, which uses Super Power Rail, at 8 to 10 percent more speed, 15 to 20 percent less power and up to 1.10 times the chip density ¹⁹.

TSMC plans to start A14 production in 2028, with more than 20 percent higher logic density than N2 ²². It said in April 2026 that two more processes, A13 and A12, are scheduled to enter production in 2029 ²³. A13 is a direct shrink of A14 with 6 percent area savings, and A12 adds Super Power Rail to the A14 platform ²³.

TSMC's logic roadmap beyond N2, from its own announcements

- 2028
N2U, 3-4% faster or 8-10% lower power than N2P
- 2028
A14, the base node for A13 and A12
- 2029
A13, a direct shrink of A14 for 6% area savings
- 2029
A12, the A14 platform with Super Power Rail backside power

Source: TSMC, 2026 North America Technology Symposium

CFET and what comes after

A basic logic circuit needs two transistors that switch on opposite signals, and in production chips the two sit side by side. Complementary field-effect transistors, or CFETs, stack the two on top of each other ²⁴. The research institute imec sees them as an attractive design for logic nodes beyond 1 nm ²⁴.

The back end of line

Wiring has become as hard to make as the transistor. Copper seeps into the insulator around it, so every wire needs a barrier, a liner and a cap ²⁵. As the most critical wiring levels drop below a 20 nm pitch, those extra layers take a large share of the wire's width ²⁵. Pitch is the distance from the center of one wire to the center of the next. Two metals are moving into those narrow levels.

²¹ Clash of the Foundries: Gate All Around + Backside Power at 2nm. SemiAnalysis · 1 October 2024 [\[B\]](https://newsletter.semianalysis.com/p/clash-of-the-foundries)
newsletter.semianalysis.com/p/clash-of-the-foundries

¹⁹ HPC Platform – Advanced Technologies. TSMC · Accessed 9 September 2026 [\[A\]](https://www.tsmc.com/english/dedicatedFoundry/technology/platform_HPC_tech_advancedTech)
www.tsmc.com/english/dedicatedFoundry/technology/platform_HPC_tech_advancedTech

²² TSMC Unveils Next-Generation A14 Process at North America Technology Symposium. TSMC · 24 April 2025 [\[A\]](https://pr.tsmc.com/english/news/3228)
pr.tsmc.com/english/news/3228

²³ TSMC Debuts A13 Technology at 2026 North America Technology Symposium. TSMC · 23 April 2026 [\[A\]](https://pr.tsmc.com/english/news/3302)
pr.tsmc.com/english/news/3302

²⁴ CFET (complementary FET). imec · 16 June 2022 [\[A\]](https://www.imec-int.com/en/articles/imec-puts-complementary-fet-cfet-logic-technology-roadmap) www.imec-int.com/en/articles/imec-puts-complementary-fet-cfet-logic-technology-roadmap

²⁵ Semi-damascene metallization. imec · 31 October 2024 [\[A\]](https://www.imec-int.com/en/articles/semi-damascene-metallization-inflection-point-back-end-line-processing) www.imec-int.com/en/articles/semi-damascene-metallization-inflection-point-back-end-line-processing

- **Ruthenium** shows promise for use without a barrier, which would keep the wire's resistance low ²⁵. imec has demonstrated ruthenium lines at a 16 nm pitch ²⁶.
- **Molybdenum** conducts worse than copper in bulk, with a resistivity of 5.3 microhm-cm against copper's 1.68 ²⁷. But in a thin film it has up to 30 percent lower resistivity than tungsten and needs no barrier either, so chipmakers are putting it into some contacts and local wiring layers ²⁷.

Who makes it

TSMC, Intel and Samsung build gate-all-around nodes with extreme-ultraviolet (EUV) lithography. China's SMIC builds 7 nm-class nodes without it ⁶.

SemiAnalysis reported in September 2026 that Intel's Panther Lake, Samsung's Exynos 2600 and Apple's A20 Pro, made on TSMC's N2, all use gate-all-around transistors ¹. In August 2025 Intel called itself the only semiconductor company that both develops and manufactures leading-edge logic chips in the United States ¹⁰.

In July 2025 Rapidus, a state-backed newcomer in Japan, said it had started making 2 nm prototypes at its plant in Chitose, Hokkaido, and would begin mass production in 2027 ⁷. Its process builds on IBM's 2 nm technology, which the two firms agreed in December 2022 to develop further for production at Rapidus's plant in Japan ⁸. By June 2026 Rapidus had raised 424.95 billion yen in equity, the latest 150 billion yen from a state agency ²⁸. It has also received government research subsidies since fiscal 2022 ²⁸.

25 Semi-damascene metallization. imec · 31 October 2024 [\[A\]](https://www.imec-int.com/en/articles/semi-damascene-metallization-inflection-point-back-end-line-processing) www.imec-int.com/en/articles/semi-damascene-metallization-inflection-point-back-end-line-processing

26 16nm Ru lines using semi-damascene integration approach. imec · 3 June 2025 [\[A\]](https://www.imec-int.com/en/press/imec-demonstrates-16nm-pitch-ru-lines-record-low-resistance-obtained-using-semi-damascene) www.imec-int.com/en/press/imec-demonstrates-16nm-pitch-ru-lines-record-low-resistance-obtained-using-semi-damascene

27 Molybdenum's Role in Ultra-Fast Computing: The Metal Behind the Speed. Entegris · 18 May 2026 [\[A\]](https://blog.entegris.com/molybdenums-role-in-ultra-fast-computing-the-metal-behind-the-speed) blog.entegris.com/molybdenums-role-in-ultra-fast-computing-the-metal-behind-the-speed

6 Is SMIC N+3's Metal Pitch Smaller than Intel 18A's?. SemiAnalysis · 14 June 2026 [\[B\]](https://newsletter.semianalysis.com/p/steel-smic-n3-teardown) newsletter.semianalysis.com/p/steel-smic-n3-teardown

1 Intel Panther Lake Teardown. SemiAnalysis · 26 September 2026 [\[B\]](https://newsletter.semianalysis.com/p/intel-panther-lake-teardown) newsletter.semianalysis.com/p/intel-panther-lake-teardown

10 Intel and Trump Administration Reach Historic Agreement to Accelerate American Technology and Manufacturing Leadership. Intel · 22 August 2025 [\[A\]](https://www.intel.com/news-events/press-releases/detail/1748/intel-and-trump-administration-reach-historic-agreement-to) www.intel.com/news-events/press-releases/detail/1748/intel-and-trump-administration-reach-historic-agreement-to

7 Rapidus Achieves Significant Milestone at its State-of-the-Art Foundry with Prototyping of Leading-Edge 2nm GAA Transistors. Rapidus · 18 July 2025 [\[A\]](https://www.rapidus.inc/en/news_topics/information/rapidus-achieves-significant-milestone-at-its-state-of-the-art-foundry-with-prototyping-of-leading-edge-2nm-gaa-transistors/) www.rapidus.inc/en/news_topics/information/rapidus-achieves-significant-milestone-at-its-state-of-the-art-foundry-with-prototyping-of-leading-edge-2nm-gaa-transistors/

8 IBM and Rapidus Form Strategic Partnership to Build Advanced Semiconductor Technology and Ecosystem in Japan. Rapidus · 13 December 2022 [\[A\]](https://www.rapidus.inc/en/news_topics/information/ibm-and-rapidus-form-strategic-partnership-to-build-advanced-semiconductor-technology-and-ecosystem-in-japan/) www.rapidus.inc/en/news_topics/information/ibm-and-rapidus-form-strategic-partnership-to-build-advanced-semiconductor-technology-and-ecosystem-in-japan/

28 Rapidus Completes 150 Billion Yen Funding Round from Japan Government. Rapidus · 5 June 2026 [\[A\]](https://www.rapidus.inc/en/news_topics/information/20260605-2/) www.rapidus.inc/en/news_topics/information/20260605-2/

A node's name, such as 7 nm, does not measure any feature on the chip. Applied Materials, a toolmaker, said in 2022 that chipmakers raise density in two ways, by printing smaller features and by laying out each logic cell more tightly ¹⁶. SMIC's N+3, its third-generation 7 nm process, sets its narrowest wires 32.5 nm apart, tighter than the 36 nm in Intel's Panther Lake chips on 18A ⁶. But 18A allows 32 nm, and SemiAnalysis called the comparison an incomplete, cherry-picked metric ⁶. N+3 packs 113.4 million transistors per square millimeter, against 107.7 for TSMC's N6 ⁶.

AI accelerators have usually trailed the leading edge. A die as large as theirs is more likely to hold a defect ²⁹. So the share of dies that work, called the yield, gets high enough only once a process has run long enough to cut its defect rate.

Blackwell uses a custom TSMC 4NP process ¹². Epoch AI estimated in December 2025 that a 300 mm wafer on that process costs \$17,000 ². AMD's MI455X, launched on 23 July 2026, lists TSMC 2 nm and 3 nm silicon ³⁰. It spreads its compute across eight separate dies ³¹.

SRAM is the fast memory on the logic die. SemiAnalysis reported in 2024 that the cell that holds one bit had barely shrunk since the 5 nm node ²¹. TSMC said in 2025 that its 2 nm SRAM uses a 0.021 square-micrometer cell and gets 1.1 times the density of its previous node by tuning design and process together ³². See Memory and HBM.

The chokepoint

TSMC, Intel and Samsung do not sell their leading-edge process flows, which set the steps, their order and the tools for each. In September 2024 the United States put a worldwide license requirement on the know-how for building gate-all-

¹⁶ Applied Materials Technologies Enable 2D Scaling with EUV and 3D Gate-All-Around Transistors. Applied Materials · 21 April 2022 ^[A] ir.appliedmaterials.com/news-releases/news-release-details/applied-materials-technologies-enable-2d-scaling-euv-and-3d-gate

⁶ Is SMIC N+3's Metal Pitch Smaller than Intel 18A's?. SemiAnalysis · 14 June 2026 ^[B] newsletter.semianalysis.com/p/steel-smic-n3-teardown

²⁹ Behrooz Parhami, Dependable Computing: A Multilevel Approach, part 2. University of California, Santa Barbara · 11 October 2020 · p. 8 ^[A] web.ece.ucsb.edu/~parhami/docs_folder/f33-book-dep-comp-pt2.pdf#page=8

¹² NVIDIA Blackwell Architecture. Nvidia · 18 December 2025 ^[A] www.nvidia.com/en-us/data-center/technologies/blackwell-architecture/

² NVIDIA's B200 costs around \$6,400 to produce. Epoch AI · 10 December 2025 ^[A] epoch.ai/data-insights/b200-cost-breakdown

³⁰ AMD Instinct™ MI455X GPUs. AMD · Accessed 9 September 2026 ^[A] www.amd.com/en/products/accelerators/instinct/mi400/mi455x.html

³¹ AMD Instinct MI455X GPU. AMD · 20 July 2026 ^[A] www.amd.com/content/dam/amd/en/documents/products/accelerators/instinct/amd-instinct-mi455x-brochure.pdf

²¹ Clash of the Foundries: Gate All Around + Backside Power at 2nm. SemiAnalysis · 1 October 2024 ^[B] newsletter.semianalysis.com/p/clash-of-the-foundries

³² A 38.1Mb/mm² SRAM in a 2nm-CMOS-Nanosheet Technology for High-Density and Energy-Efficient Compute. TSMC · 2025 ^[A] research.tsmc.com/page/memory/4.html

around transistors, with an exception for countries that impose matching controls ⁹.

China launched its third National Integrated Circuit Fund in May 2024 with 344 billion yuan, about \$47 billion ³³. But China cannot buy EUV scanners. Its 7 nm chips have been made instead on deep-ultraviolet machines, a generation behind EUV, stockpiled from ASML, the Dutch scanner maker, before export restrictions took effect ³⁴. SMIC gets fine features out of them by building its tightest layers in several patterning steps ⁶.

In July 2026 Reuters reported that a Shanghai state firm had begun making home-grown immersion deep-ultraviolet scanners ³⁵. Citing The Information, it said the firm planned about five that year and roughly 20 in 2027 ³⁵. Reuters's own source said the firm's machine still needed testing and was far from matching ASML's models ³⁵.

Domestic EUV is further off. China has announced \$43 billion to develop it ³⁴. In September 2025 the Center for Strategic and International Studies (CSIS) judged that EUV remains firmly out of reach despite massive state investment ³⁴.

See Lithography and Who Controls the Chain.

FOUR THINGS TO REMEMBER

- The newest transistors wrap the gate around all four sides of the channel to cut the current that leaks when the switch is off.
- Only TSMC, Intel and Samsung make them in volume.
- TSMC, Intel and Samsung do not sell their leading-edge process flows, so a newcomer has to develop its own or build on another firm's, as Rapidus is doing with IBM's.
- China's SMIC makes 7 nm-class chips without EUV by building its tightest layers in several patterning steps.

9 Commerce Control List Additions and Revisions; Implementation of Controls on Advanced Technologies Consistent With Controls Implemented by International Partners. Federal Register (Commerce Department; Industry and Security Bureau) · 6 September 2024 [A] www.federalregister.gov/documents/2024/09/06/2024-19633/commerce-control-list-additions-and-revisions-implementation-of-controls-on-advanced-technologies

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Made by **Yashvardhan Sharma** with Claude. Corrections and questions: contact@chipsupplychain.org.

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A company filings, governments, standards bodies, universities and research institutions; **B** SemiAnalysis, Reuters, the Financial Times and Nikkei Asia.

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